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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

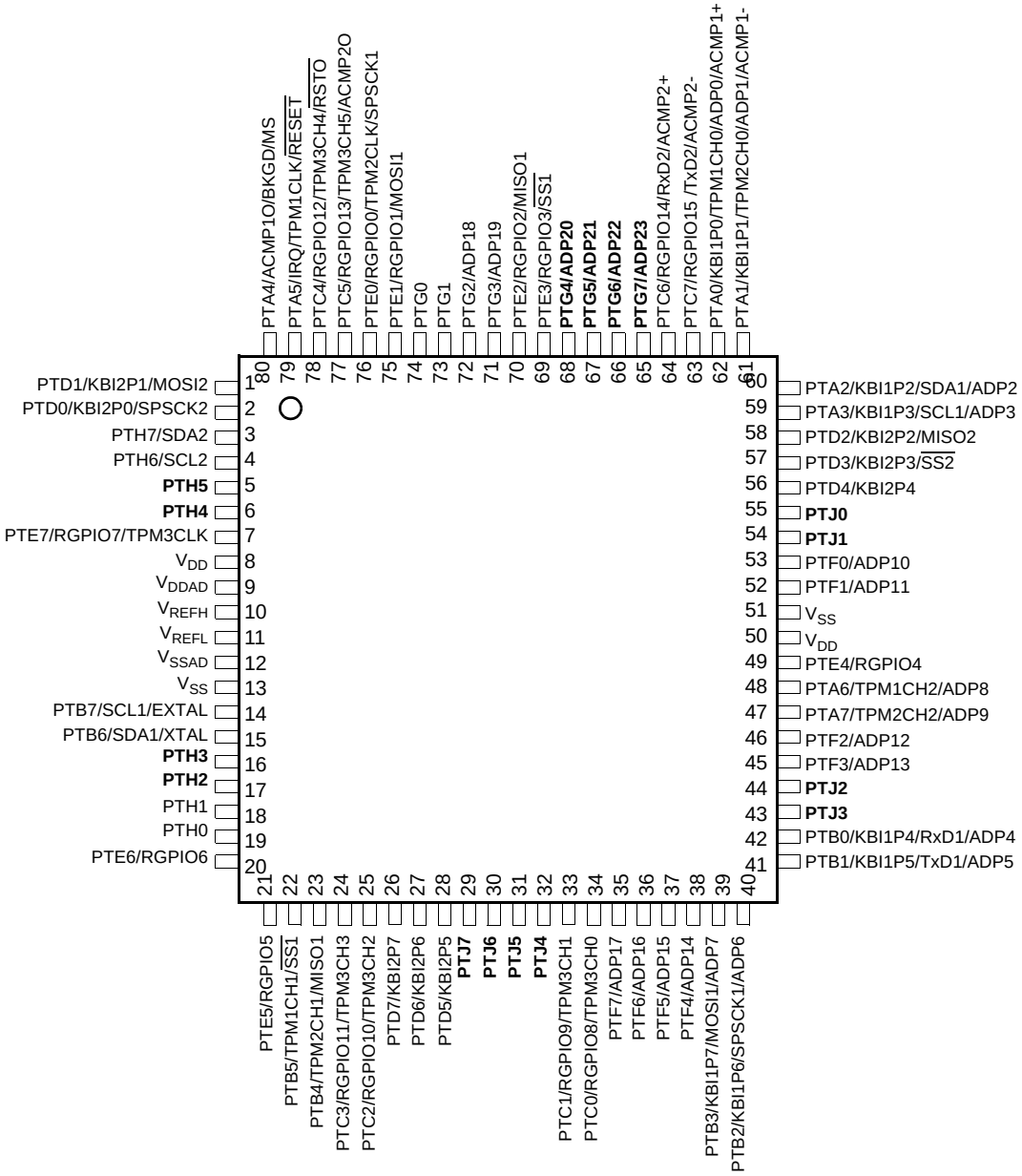
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	54
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51qe32clh

Table of Contents

2 Pin Assignments

This section describes the pin assignments for the available packages. See Table 1 for pin availability by package pin-count.



Pins in **bold** are added from the next smaller package.

Figure 2. Pin Assignments in 80-Pin LQFP

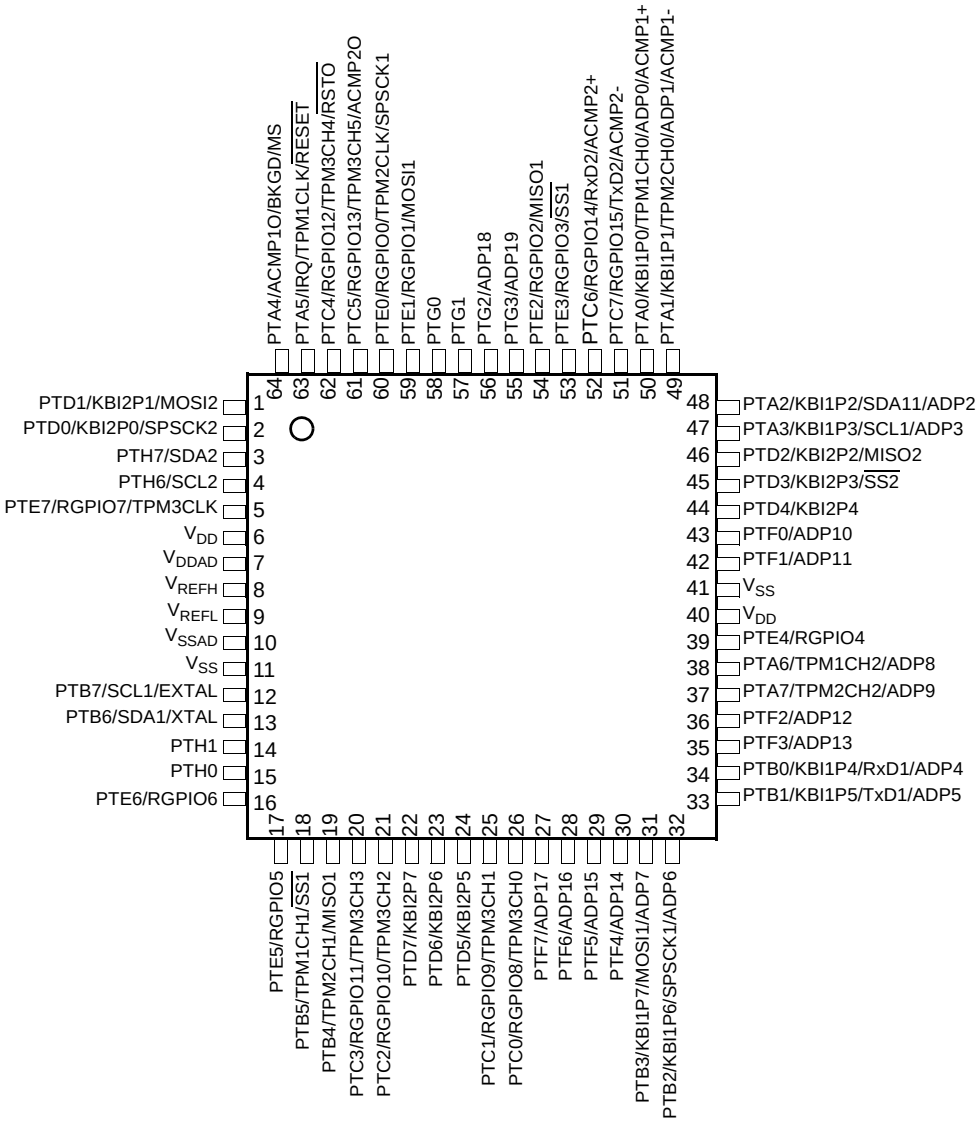


Figure 3. Pin Assignments in 64-Pin LQFP Package

Table 2. MCF51QE128 Series Pin Assignment by Package and Pin Sharing Priority

Pin Number		Lowest	←	Priority	→	Highest
80	**64**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	1	PTD1	KBI2P1	MOSI2		
2	2	PTD0	KBI2P0	SPSCK2		
3	3	PTH7	SDA2			
4	4	PTH6	SCL2			
5	—	PTH5				
6	—	PTH4				
7	5	PTE7	RGPIO7	TPM3CLK		
8	6					V_{DD}
9	7					V_{DDAD}
10	8					V_{REFH}
11	9					V_{REFL}
12	10					V_{SSAD}
13	11					V_{SS}
14	12	PTB7	SCL1			EXTAL
15	13	PTB6	SDA1			XTAL
16	—	PTH3				
17	—	PTH2				
18	14	PTH1				
19	15	PTH0				
20	16	PTE6	RGPIO6			
21	17	PTE5	RGPIO5			
22	18	PTB5	TPM1CH1	$\overline{SS1}$		
23	19	PTB4	TPM2CH1	MISO1		
24	20	PTC3	RGPIO11	TPM3CH3		
25	21	PTC2	RGPIO10	TPM3CH2		
26	22	PTD7	KBI2P7			
27	23	PTD6	KBI2P6			
28	24	PTD5	KBI2P5			
29	—	PTJ7				
30	—	PTJ6				
31	—	PTJ5				
32	—	PTJ4				
33	25	PTC1	RGPIO9	TPM3CH1		
34	26	PTC0	RGPIO8	TPM3CH0		
35	27	PTF7				ADP17
36	28	PTF6				ADP16
37	29	PTF5				ADP15
38	30	PTF4				ADP14
39	31	PTB3	KBI1P7	MOSI1[1]		ADP7
40	32	PTB2	KBI1P6	SPSCK1		ADP6

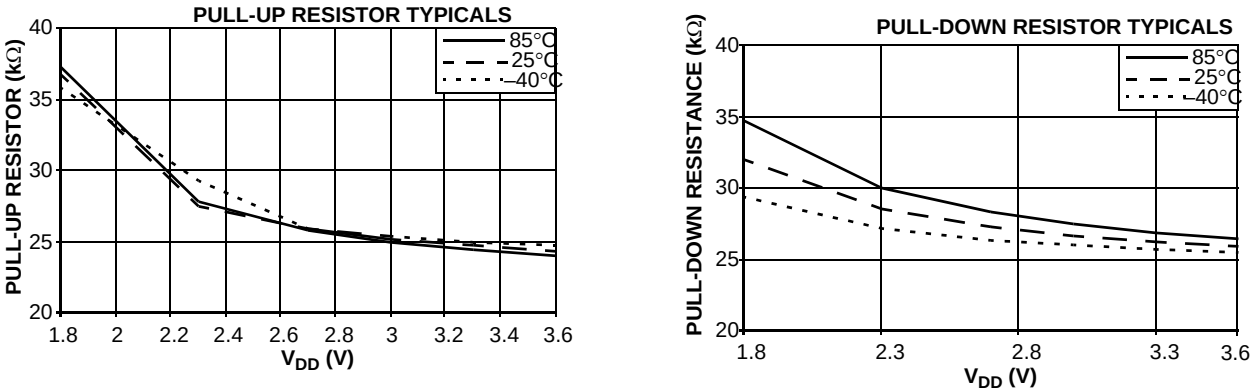


Figure 4. Pull-up and Pull-down Typical Resistor Values

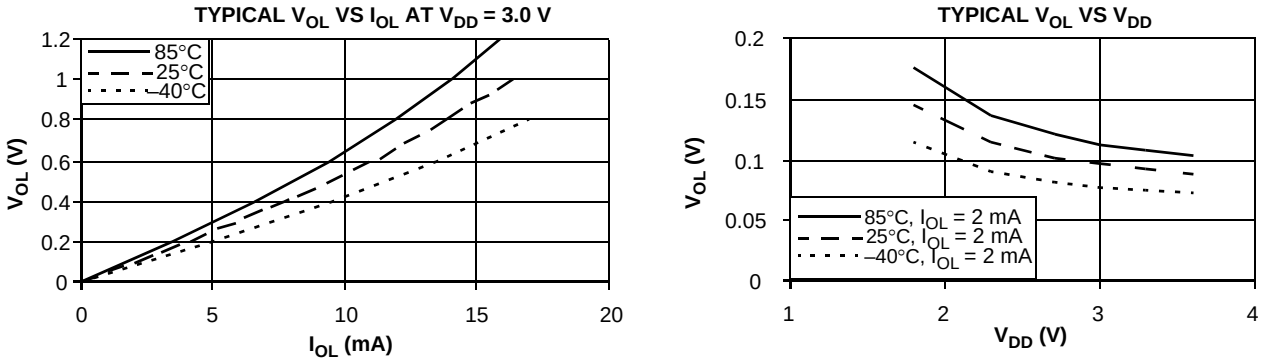


Figure 5. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)

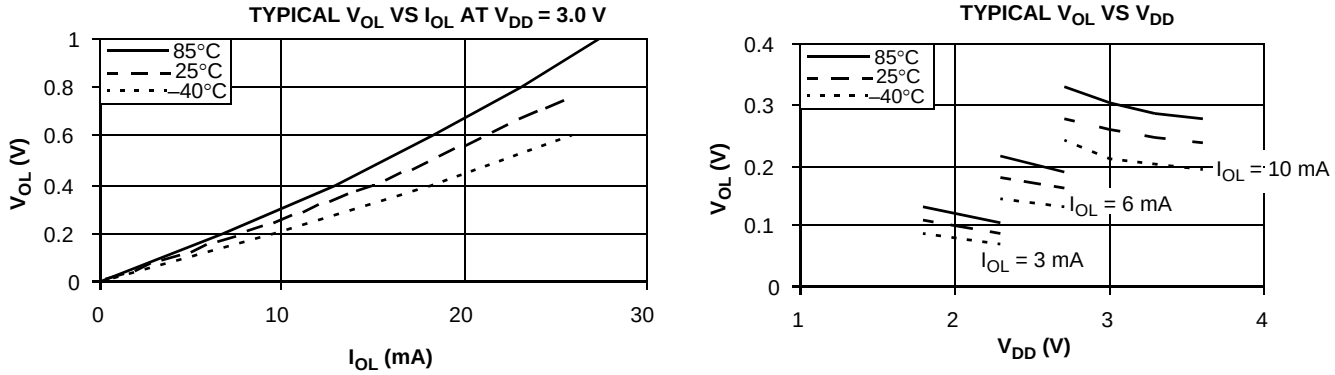


Figure 6. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)

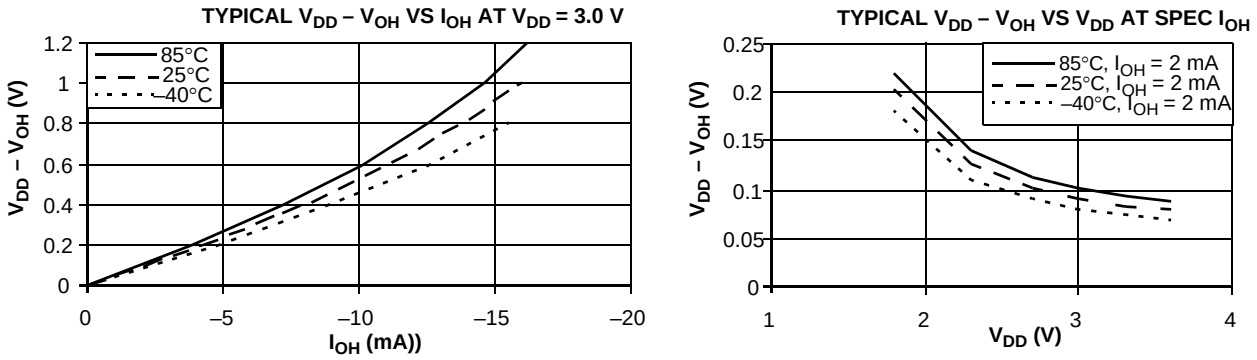


Figure 7. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

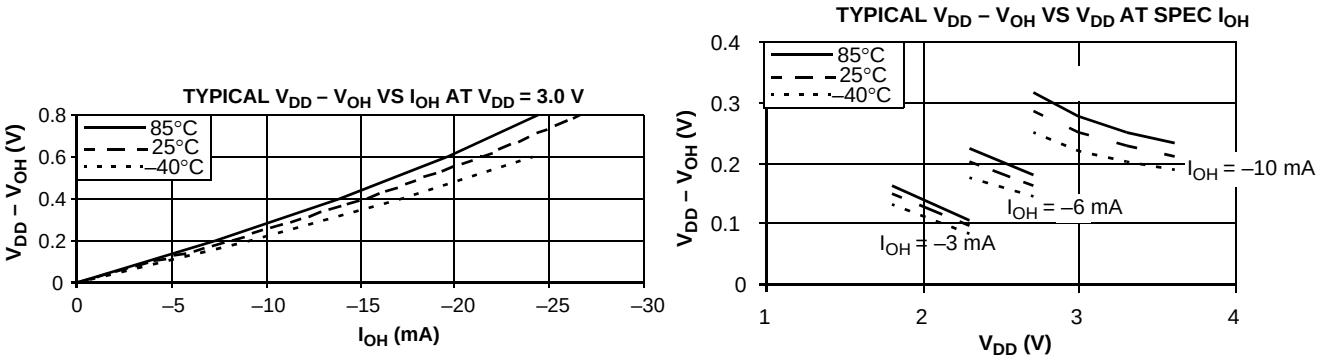


Figure 8. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	RI_{DD}	25.165 MHz	3	32	35	mA	–40 to 25
	P					32	35		85
	T			20 MHz		28.0	—		–40 to 85
	T			8 MHz		13.2	—		
	T			1 MHz		2.4	—		
2	C	Run supply current FEI mode, all modules off	RI_{DD}	25.165 MHz	3	28.1	29.6	mA	–40 to 85
	T			20 MHz		22.9	—		
	T			8 MHz		11.3	—		
	T			1 MHz		2.0	—		

Table 9. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
3	T	Run supply current LPS=0, all modules off	RI_{DD}	16 kHz FBILP	3	203	—	µA	–40 to 85
	T			16 kHz FBELP		154	—		
4	T	Run supply current LPS=1, all modules off, running from Flash	RI_{DD}	16 kHz FBELP	3	50	—	µA	–40 to 85
5	C	Wait mode supply current FEI mode, all modules off	WI_{DD}	25.165 MHz	3	11	13.7	mA	–-40 to 85
	T			20 MHz		4.57	—		
	T			8 MHz		2	—		
	T			1 MHz		0.73	—		
6	P	Stop2 mode supply current	$S2I_{DD}$	n/a	3	0.6	0.8	µA	-40 to 25
	C					3.0	11		70
	P					8.0	20		85
	C				2	0.6	0.8		-40 to 25
	C					2.5	10		70
	C					6.0	12		85
7	P	Stop3 mode supply current No clocks active	$S3I_{DD}$	n/a	3	0.8	1.3	µA	-40 to 25
	C					6.0	18		70
	P					18.0	28		85
	C				2	0.8	1.3		-40 to 25
	C					5.0	16		70
	C					12.0	20		85

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

Table 10. Stop Mode Adders

Num	C	Parameter	Condition	Temperature (°C)				Units
				-40	25	70	85	
1	T	LPO		50	75	100	150	nA
2	T	ERREFSTEN	RANGE = HGO = 0	1000	1000	1100	1500	nA
3	T	IREFSTEN[1]		63	70	77	81	uA
4	T	RTC	does not include clock source current	50	75	100	150	nA
5	T	LVD[1]	LVDSE = 1	90	100	110	115	uA
6	T	ACMP[1]	not using the bandgap (BGBE = 0)	18	20	22	23	uA
7	T	ADC[1]	ADLPC = ADLSMP = 1 not using the bandgap (BGBE = 0)	95	106	114	120	uA

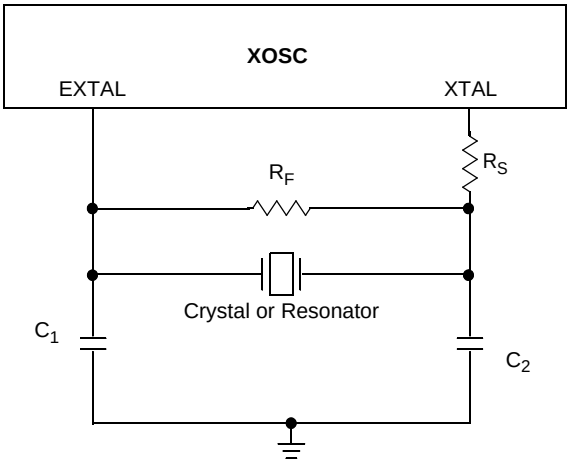


Figure 10. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

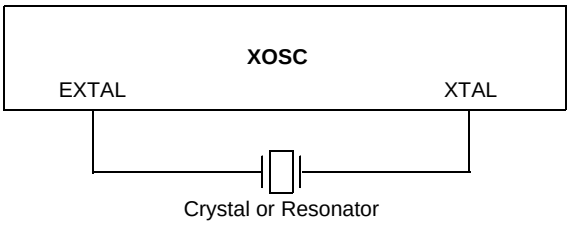


Figure 11. Typical Crystal or Resonator Circuit: Low Range/Low Gain

3.9 Internal Clock Source (ICS) Characteristics

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
1	P	Average internal reference frequency — factory trimmed at V_{DD} = 3.6 V and temperature = 25°C		f_{int_ft}	—	32.768	—	kHz
2	P	Internal reference frequency — user trimmed		f_{int_ut}	31.25	—	39.06	kHz
3	T	Internal reference start-up time		t_{IRST}	—	60	100	µs
4	P	DCO output frequency range — trimmed [2]	Low range (DRS=00)	f_{dco_u}	16	—	20	MHz
	P		Mid range (DRS=01)		32	—	40	
	P		High range (DRS=10)		48	—	60	
5	P	DCO output frequency [2] Reference = 32768 Hz and DMX32 = 1	Low range (DRS=00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DRS=01)		—	39.85	—	
	P		High range (DRS=10)		—	59.77	—	
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	$\%f_{dco}$

Table 12. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
8	C	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	+ 0.5 -1.0	± 2	$\%f_{dco}$
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0°C to 70 °C	Δf_{dco_t}	—	± 0.5	± 1	$\%f_{dco}$
10	C	FLL acquisition time [3]	$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval) [4]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

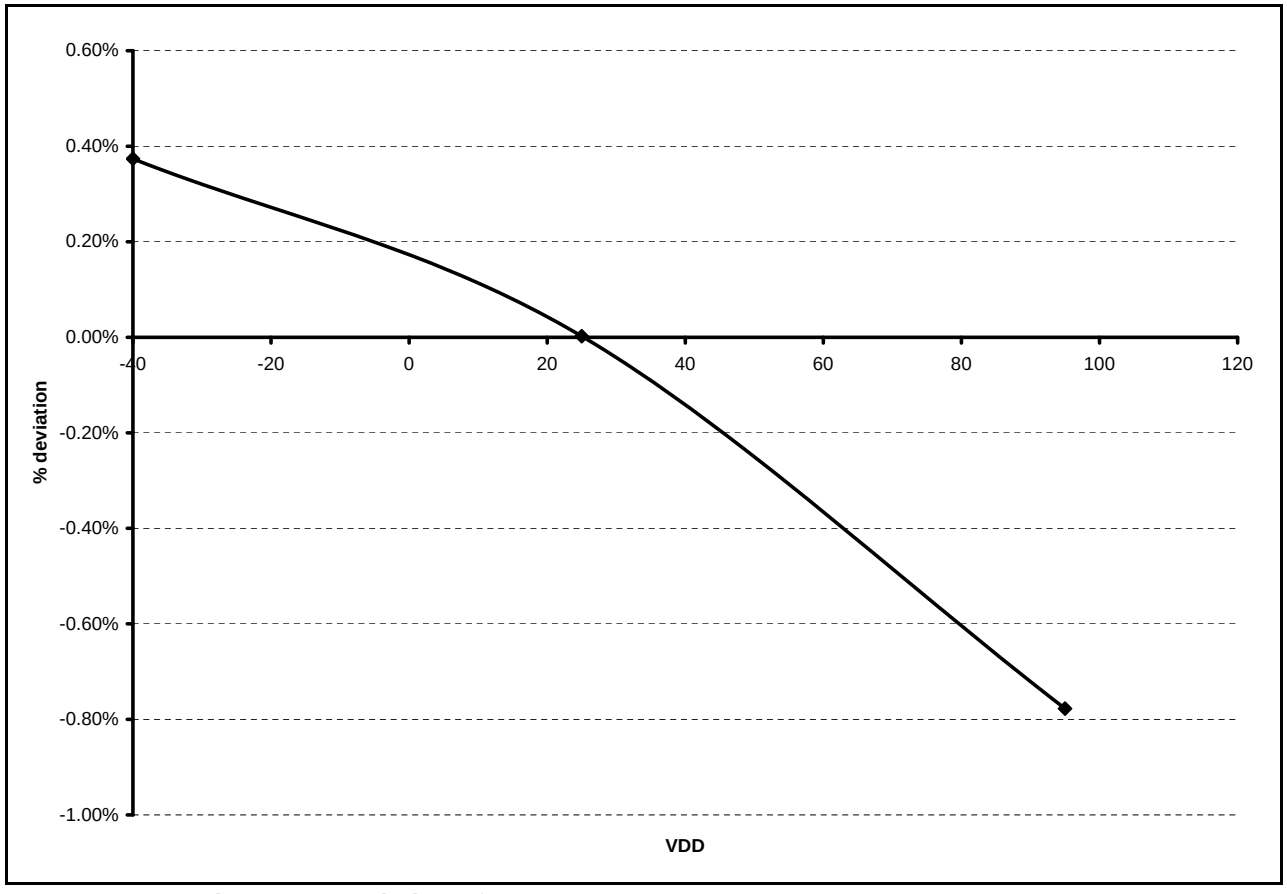


Figure 12. Deviation of DCO Output Across Temperature at V_{DD} = 3.0 V

Table 13. Control Timing (continued)

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 2 x t_{cyc}	— —	— —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 2 x t_{cyc}	— —	— —	ns
9	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	8 31	— —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF) Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	7 24	— —	ns
10		Voltage regulator recovery time	t_{VRR}	—	4	—	µs

1 Typical values are based on characterization data at V_{DD} = 3.0V, 25°C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset or interrupt pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum assertion time in which the interrupt **may** be recognized. The correct protocol is to assert the interrupt request until it is explicitly negated by the interrupt service routine.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

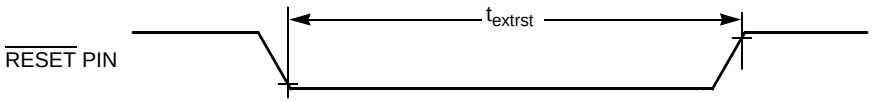


Figure 14. Reset Timing

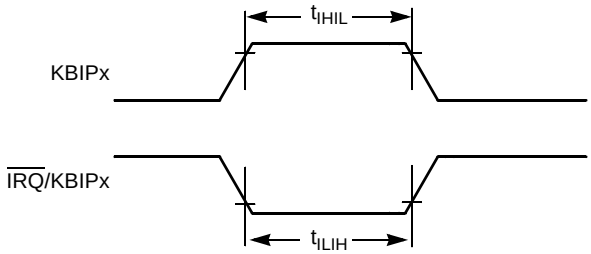


Figure 15. IRQ/KBIPx Timing

3.10.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 14. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

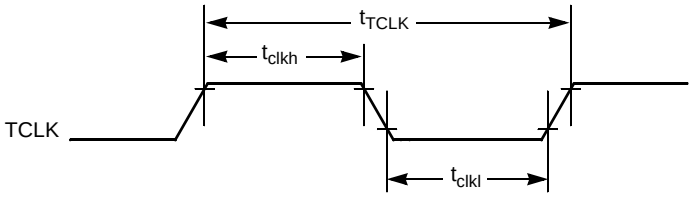


Figure 16. Timer External Clock

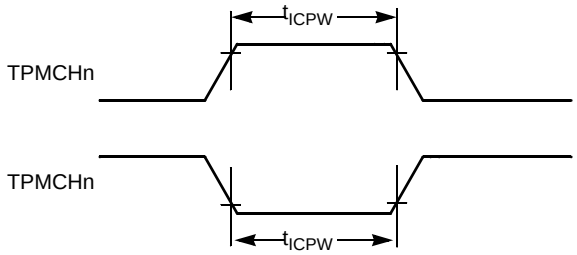
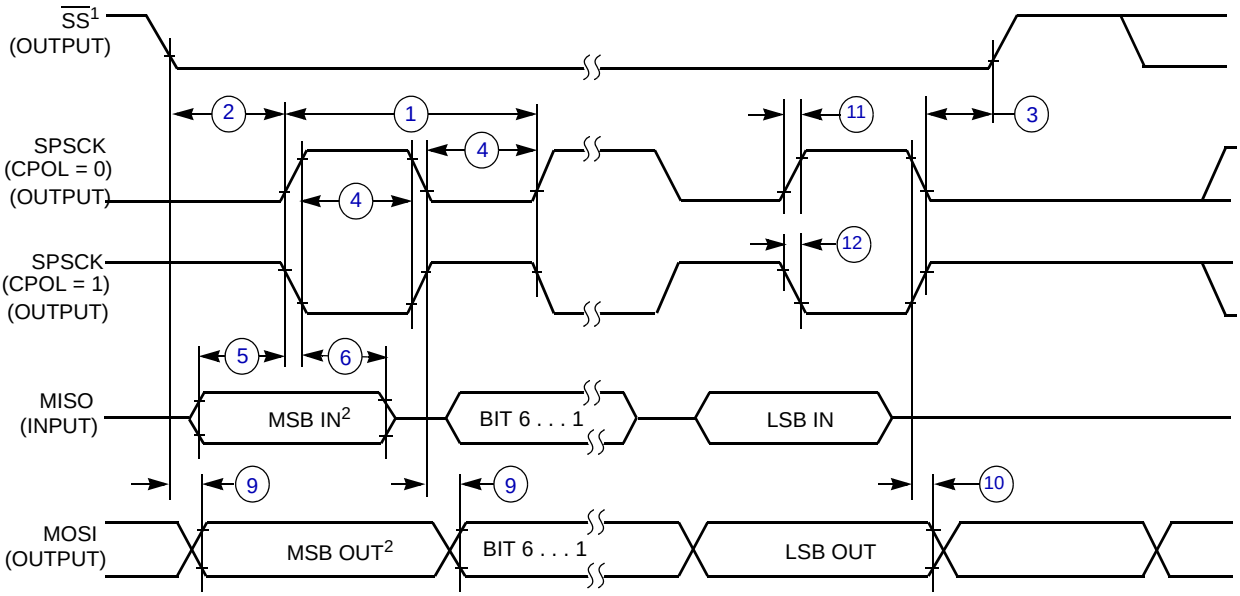
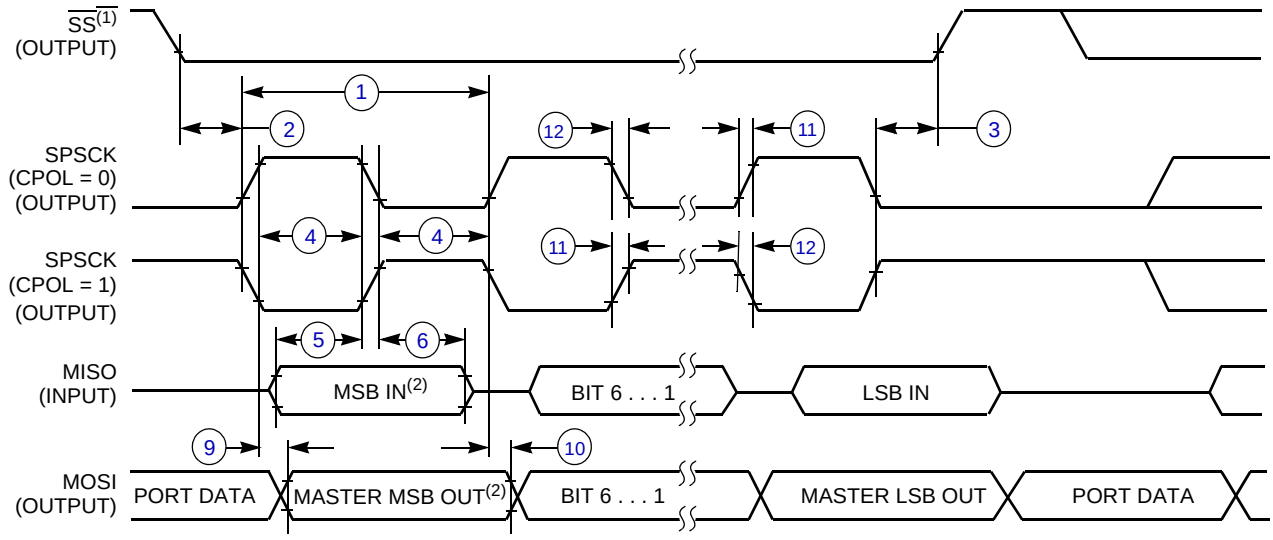


Figure 17. Timer Input Capture Pulse



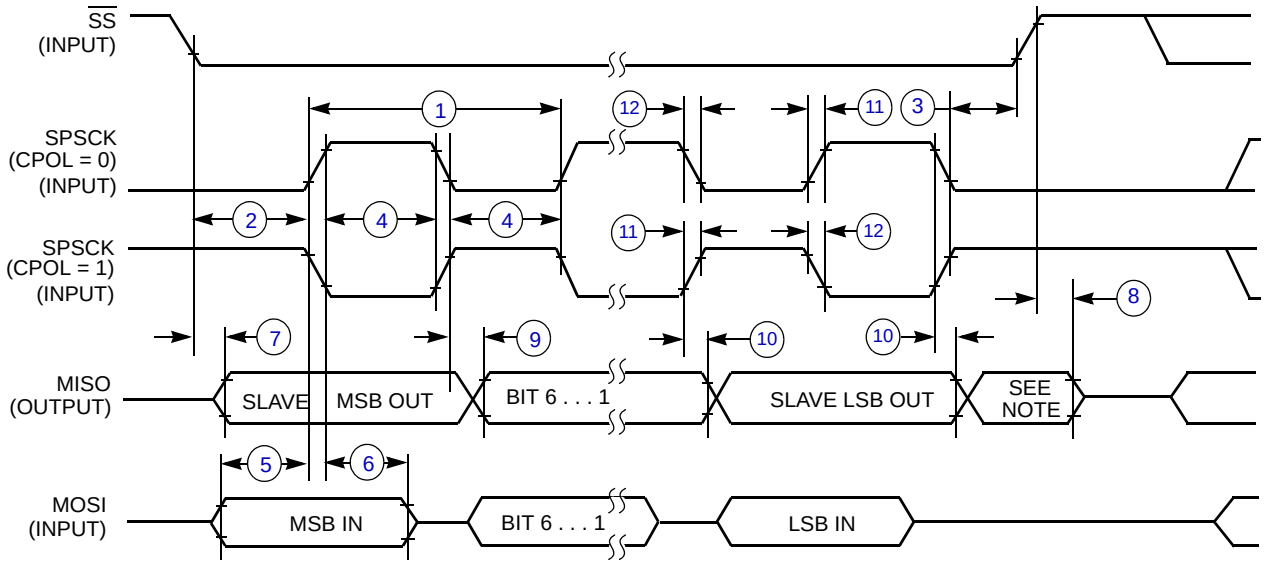
NOTES:
1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

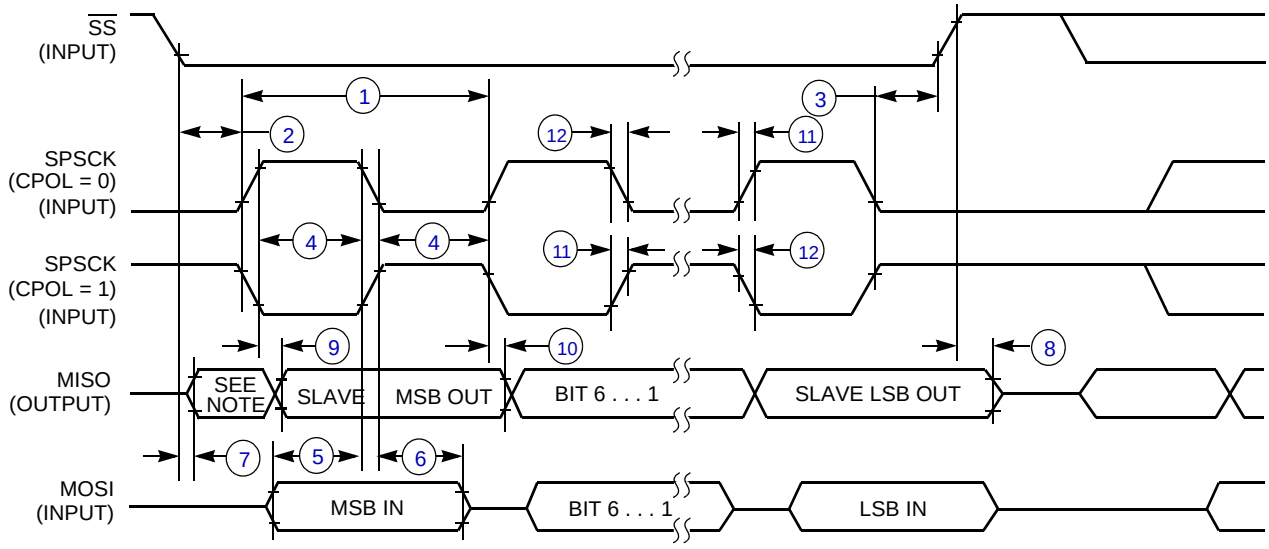
Figure 19. SPI Master Timing (CPHA =1)



NOTE:

1. Not defined but normally MSB of character just received

Figure 20. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 21. SPI Slave Timing (CPHA = 1)

3.11 Analog Comparator (ACMP) Electricals

Table 16. Analog Comparator Electrical Specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DD}	1.80	—	3.6	V
C	Supply current (active)	I_{DDAC}	—	20	35	µA
D	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
C	Analog input offset voltage	V_{AIO}		20	40	mV
C	Analog comparator hysteresis	V_H	3.0	9.0	15.0	mV
P	Analog input leakage current	I_{ALKG}	—	—	1.0	µA
C	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	µs

3.12 ADC Characteristics

Table 17. 12-bit ADC Operating Conditions

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
D	Supply voltage	Absolute	V_{DDAD}	1.8	—	3.6	V	
		Delta to V_{DD} (V_{DD}-V_{DDAD})[2]	ΔV_{DDAD}	-100	0	+100	mV	
D	Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSAD})[2]	ΔV_{SSAD}	-100	0	+100	mV	
D	Ref Voltage High		V_{REFH}	1.8	V_{DDAD}	V_{DDAD}	V	
D	Ref Voltage Low		V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V	
D	Input Voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
C	Input Capacitance		C_{ADIN}	—	4.5	5.5	pF	
C	Input Resistance		R_{ADIN}	—	5	7	kΩ	
C	Analog Source Resistance	12 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
		10 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz		 — —	 — —	 5 10		
		8 bit mode (all valid f_{ADCK})		—	—	10		
D	ADC Conversion Clock Freq.	High Speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
		Low Power (ADLPC=1)		0.4	—	4.0		

1 Typical values assume V_{DDAD} = 3.0V, Temp = 25°C, f_{ADCK}=1.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

Table 18. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
Conversion Time (Including sample time)	Short Sample (ADLSMP=0)	P	t_{ADC}	—	20	—	ADCK cycles	See the ADC chapter in the *MCF51QE128 Reference Manual* for conversion time variances
	Long Sample (ADLSMP=1)	C		—	40	—		
Sample Time	Short Sample (ADLSMP=0)	P	t_{ADS}	—	3.5	—	ADCK cycles	
	Long Sample (ADLSMP=1)	C		—	23.5	—		
Total Unadjusted Error	12 bit mode	T	E_{TUE}	—	±3.0	—	LSB[2]	Includes Quantization
	10 bit mode	P		—	±1	±2.5		
	8 bit mode	T		—	±0.5	±1.0		
Differential Non-Linearity	12 bit mode	T	DNL	—	±1.75	—	LSB[2]	
	10 bit mode[3]	P		—	±0.5	±1.0		
	8 bit mode[3]	T		—	±0.3	±0.5		
Integral Non-Linearity	12 bit mode	T	INL	—	±1.5	—	LSB[2]	
	10 bit mode	T		—	±0.5	±1.0		
	8 bit mode	T		—	±0.3	±0.5		
Zero-Scale Error	12 bit mode	T	E_{ZS}	—	±1.5	—	LSB[2]	V_{ADIN} = V_{SSAD}
	10 bit mode	P		—	±0.5	±1.5		
	8 bit mode	T		—	±0.5	±0.5		
Full-Scale Error	12 bit mode	T	E_{FS}	—	±1.0	—	LSB[2]	V_{ADIN} = V_{DDAD}
	10 bit mode	P		—	±0.5	±1		
	8 bit mode	T		—	±0.5	±0.5		
Quantization Error	12 bit mode	D	E_Q	—	-1 to 0	—	LSB[2]	
	10 bit mode			—	—	±0.5		
	8 bit mode			—	—	±0.5		
Input Leakage Error	12 bit mode	D	E_{IL}	—	±2	—	LSB[2]	Pad leakage[4] * R_{AS}
	10 bit mode			—	±0.2	±4		
	8 bit mode			—	±0.1	±1.2		
Temp Sensor Slope	-40°C to 25°C	D	m	—	1.646	—	mV/°C	
	25°C to 85°C			—	1.769	—		
Temp Sensor Voltage	25°C	D	V_{TEMP25}	—	701.2	—	mV	

1 Typical values assume V_{DDAD} = 3.0V, Temp = 25°C, f_{ADCK}=1.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and No-Missing-Codes guaranteed in 10 bit and 8 bit modes

4 Based on input pad leakage current. Refer to pad electricals.

3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section of the *MCF51QE128 Reference Manual*.

Table 19. Flash Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase -40°C to 85°C	$V_{prog/erase}$	1.8		3.6	V
D	Supply voltage for read operation	V_{Read}	1.8		3.6	V
D	Internal FCLK frequency[1]	f_{FCLK}	150		200	kHz
D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	µs
P	Longword program time (random location)[(2)]	t_{prog}	9			t_{Fcyc}
P	Longword program time (burst mode)[(2)]	t_{Burst}	4			t_{Fcyc}
P	Page erase time[2]	t_{Page}	4000			t_{Fcyc}
P	Mass erase time[(2)]	t_{Mass}	20,000			t_{Fcyc}
	Longword program current[3]	R_{IDDBP}	—	9.7	—	mA
	Page erase current[3]	R_{IDDPE}	—	7.6	—	mA
C	Program/erase endurance[4] T_L to T_H = –40°C to + 85°C T = 25°C		10,000 —	— 100,000	— —	cycles
C	Data retention[5]	t_{D_ret}	15	100	—	years

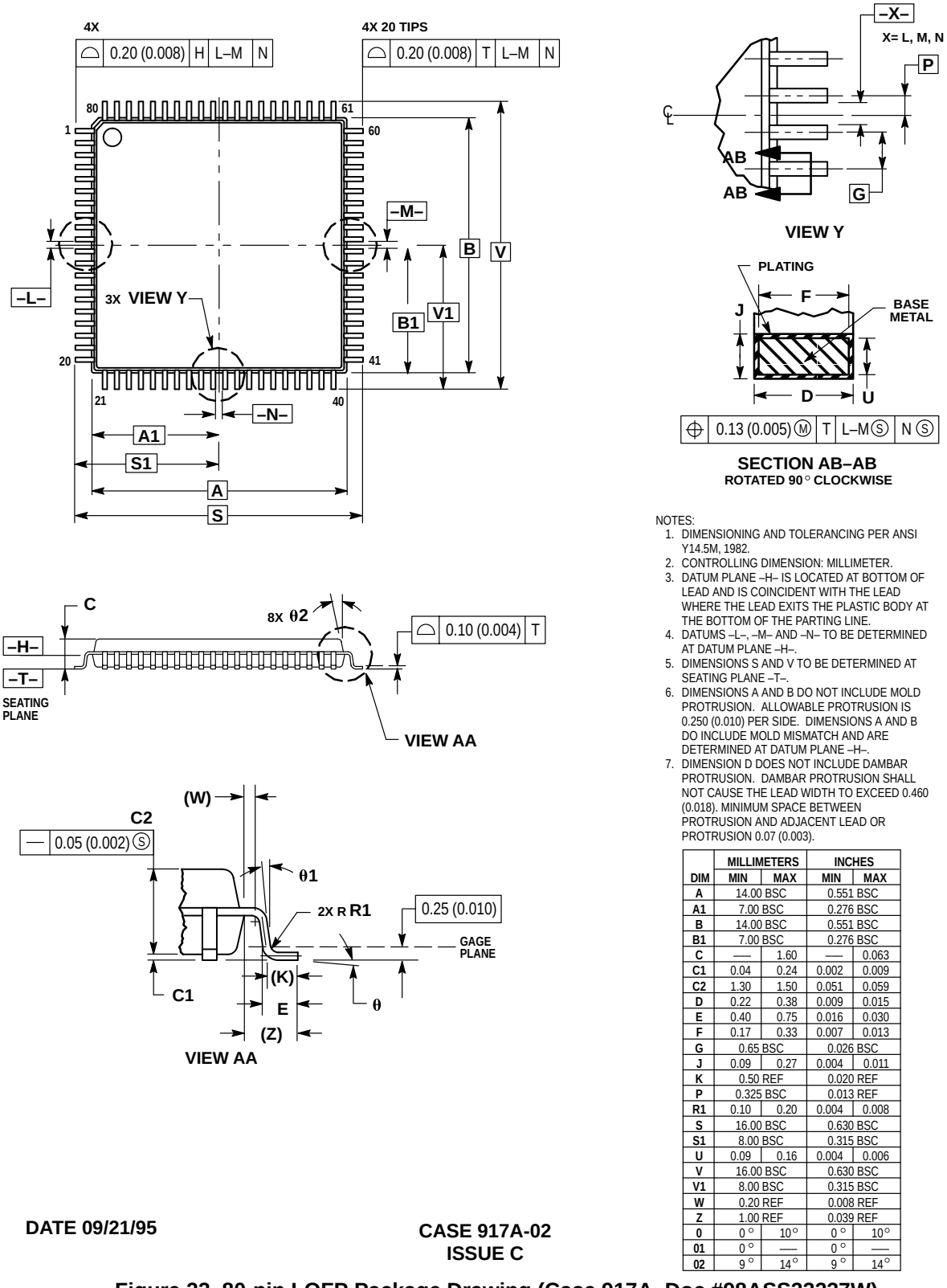
1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 3.0 V, bus frequency = 4.0 MHz.

4 **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.460 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.00 BSC		0.551 BSC	
A1	7.00 BSC		0.276 BSC	
B	14.00 BSC		0.551 BSC	
B1	7.00 BSC		0.276 BSC	
C	—	1.60	—	0.063
C1	0.04	0.24	0.002	0.009
C2	1.30	1.50	0.051	0.059
D	0.22	0.38	0.009	0.015
E	0.40	0.75	0.016	0.030
F	0.17	0.33	0.007	0.013
G	0.65 BSC		0.026 BSC	
J	0.09	0.27	0.004	0.011
K	0.50 REF		0.020 REF	
P	0.325 BSC		0.013 REF	
R1	0.10	0.20	0.004	0.008
S	16.00 BSC		0.630 BSC	
S1	8.00 BSC		0.315 BSC	
U	0.09	0.16	0.004	0.006
V	16.00 BSC		0.630 BSC	
V1	8.00 BSC		0.315 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	10°	0°	10°
θ1	0°	—	0°	—
θ2	9°	14°	9°	14°

DATE 09/21/95

CASE 917A-02
ISSUE C

Figure 23. 80-pin LQFP Package Drawing (Case 917A, Doc #98ASS23237W)

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

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TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: D	
	CASE NUMBER: 840F-02	06 APR 2005	
	STANDARD: JEDEC MS-026 BCD		

Figure 26. 64-pin LQFP Package Drawing (Case 840F, Doc #98ASS23234W), Sheet 3 of 3

6 Product Documentation

Find the most current versions of all documents at: http://www.freescale.com

Reference Manual (MCF51QE128RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

7 Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web are the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://www.freescale.com

The following revision history table summarizes changes contained in this document.

Table 22. Revision History

Revision	Date	Description of Changes
3	25 Jun 2007	Table 8: Changed Condition entires in specs #6 (V_{IH}) and #7 (V_{IL}) from $V_{DD} \geq 1.8V$ to $V_{DD} > 2.7V$ and $V_{DD} \leq 1.8V$ to $V_{DD} > 1.8V$. Table 8: Changed V_{DD} rising and V_{DD} falling min/typ/max specs in row #19 (Low-voltage warning threshold—high range) from 2.35, 2.40, and 2.50 to 2.36, 2.46, and 2.56 respectively.
4	17 Sep 2007	Added information about the MCF51QE32 device. Changed the SRAM size for the MCF51QE64 device (was 4 Kbytes, is 8 Kbytes). Corrected the number of ADC channels for the MCF51QE64 device (was 22, is 20). Corrected the number of ADC channels for the 64-pin package of the MCF51QE64 device (was 22, is 20).
		Changed ACMP electricals, V_{AIO} specification's test category from P to C.
5	28 May 2008	Updated the tables **Thermal Characteristics**, **DC Characteristics**, **Supply Current Characteristics**, **XOSC and ICS Specifications (Temperature Range = –40 to 85°C Ambient)**, **ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)**, **Control Timing**, and **Analog Comparator Electrical Specifications**, **12-bit ADC Characteristics (VREFH = VDDAD, VREFL = VSSAD)** Updated the figures **Typical Run IDD for FBE and FEI, IDD vs. VDD (ACMP and ADC off, All Other Modules Enabled)**, **Deviation of DCO Output from Trimmed Frequency (50.33 MHz, 3.0 V)**, and **Deviation of DCO Output from Trimmed Frequency (50.33 MHz, 25°C)**
6	24 Jun 2008	Updated the table **Thermal Characteristics** Updated the row corresponding to Num 18 in the table **DC Characteristics** Updated the tables **MCF51QE128 Series Features by MCU and Package**, **DC Characteristics**, **Supply Current Characteristics**, **Thermal Characteristics**, **Control Timing**, and **Ordering Information** Updated the figures **Typical Run IDD for FBE and FEI, IDD vs. VDD (ADC off, All Other Modules Enabled)**, **Deviation of DCO Output Across Temperature at VDD = 3.0 V**, and **Deviation of DCO Output Across VDD at 25×C**
7	14 Oct 2008	Updated the Stop2 and Stop3 mode supply current in the Supply Current Characteristics table. Replaced the stop mode adders section from the Supply Current Characteristics with its own Stop Mode Adders table with new specifications.

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