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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	37
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 15x12b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f334c4t6

Table 2. STM32F334x4/6/8 family device features and peripheral counts (continued)

Peripheral		STM32F334Kx	STM32F334Cx	STM32F334Rx
Comm. interfaces	SPI	1		
	I^2C	1		
	USART	2	3	
	CAN	1		
GPIOs	Normal I/Os (TC, TTa)	10	20	26
	5-Volt tolerant I/Os (FT,FTf)	15	17	25
Capacitive sensing channels		14	17	18
DMA channels		7		
12-bit ADCs Number of channels		2 10	2 15	2 21
12-bit DAC channels		3		
Ultra-fast analog comparator		2	3	
Operational amplifiers		1		
CPU frequency		72 MHz		
Operating voltage		2.0 to 3.6 V		
Operating temperature		Ambient operating temperature: - 40 to 85 °C / - 40 to 105 °C Junction temperature: - 40 to 125 °C		
Packages		LQFP32	LQFP48	LQFP64

1. This total considers also the PWMs generated on the complementary output channels.

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed, following a specific sequence to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

3.8 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 7 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers, high-resolution timer, DAC and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F334x4/6/8 devices embed a nested vectored interrupt controller (NVIC) able to handle up to 60 interrupt channels, that can be masked and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The external interrupt/event controller consists of 27 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked

3.14.1 217 ps high-resolution timer (HRTIM1)

The high-resolution timer (HRTIM1) allows generating digital signals with high-accuracy timings, such as PWM or phase-shifted pulses.

It consists of 6 timers, 1 master and 5 slaves, totaling 10 high-resolution outputs, which can be coupled by pairs for deadtime insertion. It also features 5 fault inputs for protection purposes and 10 inputs to handle external events such as current limitation, zero voltage or zero current switching.

HRTIM1 timer is made of a digital kernel clocked at 144 MHz followed by delay lines. Delay lines with closed loop control guarantee a 217 ps resolution whatever the voltage, temperature or chip-to-chip manufacturing process deviation. The high-resolution is available on the 10 outputs in all operating modes: variable duty cycle, variable frequency, and constant ON time.

The slave timers can be combined to control multiswitch complex converters or operate independently to manage multiple independent converters.

The waveforms are defined by a combination of user-defined timings and external events such as analog or digital feedbacks signals.

HRTIM1 timer includes options for blanking and filtering out spurious events or faults. It also offers specific modes and features to offload the CPU: DMA requests, burst mode controller, push-pull and resonant mode.

It supports many topologies including LLC, Full bridge phase shifted, buck or boost converters, either in voltage or current mode, as well as lighting application (fluorescent or LED). It can also be used as a general purpose timer, for instance to achieve high-resolution PWM-emulated DAC.

In debug mode, the HRTIM1 counters can be frozen and the PWM outputs enter safe state.

3.14.2 Advanced timer (TIM1)

The advanced-control timer can be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timers (described in *Section 3.14.3* using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

3.16.2 Universal synchronous / asynchronous receivers / transmitters (USARTs)

The STM32F334x4/6/8 devices have three embedded universal synchronous receivers/transmitters (USART1, USART2 and USART3).

The USART interfaces are able to communicate at speeds of up to 9 Mbits/s.

USART1 provides hardware management of the CTS and RTS signals. It supports IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and has LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

The features available in the USART interfaces are showed below in *Table 8*.

Table 8. USART features

USART modes/features(1)	USART1	USART2 USART3
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode	X	X
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	-
LIN mode	X	-
Dual clock domain and wakeup from Stop mode	X	-
Receiver timeout interrupt	X	-
Modbus communication	X	-
Auto baud rate detection	X	-
Driver Enable	X	X

1. X = supported.

3.16.3 Serial peripheral interface (SPI)

A SPI interface allows to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

The features available in SPI1 are showed below in *Table 9*.

Table 9. STM32F334x4/6/8 SPI implementation

SPI features(1)	SPI1
Hardware CRC calculation	X
Rx/Tx FIFO	X

Table 9. STM32F334x4/6/8 SPI implementation (continued)

SPI features[1]	SPI1
NSS pulse mode	X
TI mode	X

1. X = supported.

3.16.4 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

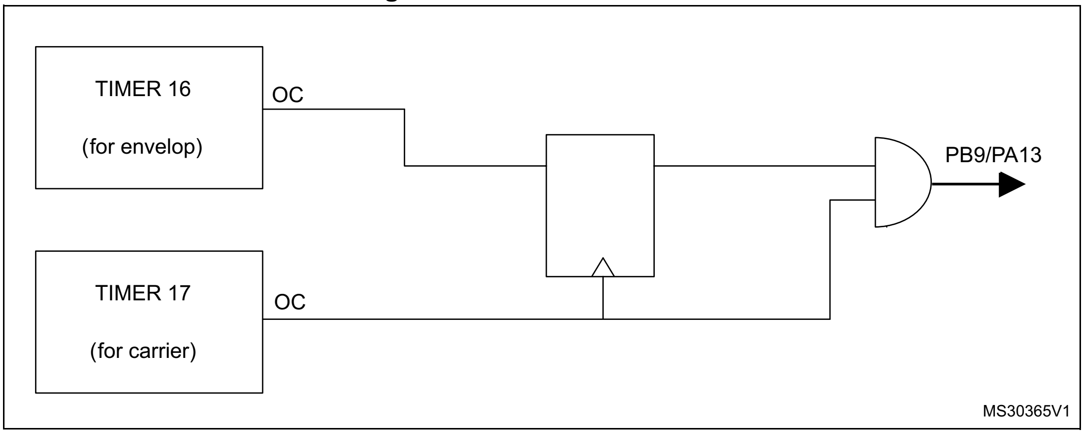
3.17 Infrared transmitter

The STM32F334x4/6/8 devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

Figure 3. Infrared transmitter



3.18 Touch sensing controller (TSC)

The STM32F334x4/6/8 devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 18 capacitive sensing channels distributed over 6 analog I/Os group.

Capacitive sensing technology is able to detect the presence of a finger near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of

3.19 Development support

3.19.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Table 13. STM32F334x4/6/8 pin definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Pin functions	
LQFP 32	LQFP 48	LQFP 64				Alternate functions	Additional functions
13	17	23	PA7	I/O	TTa	TIM17_CH1, TIM3_CH2, TSC_G2_IO4, SPI1_MOSI, TIM1_CH1N, EVENTOUT	ADC2_IN4(2), COMP2_INP, OPAMP2_VINP
-	-	24	PC4	I/O	TTa	EVENTOUT, TIM1_ETR, USART1_TX	ADC2_IN5(2)
-	-	25	PC5	I/O	TTa	EVENTOUT, TIM15_BKIN, TSC_G3_IO1, USART1_RX	ADC2_IN11, OPAMP2_VINM
14	18	26	PB0	I/O	TTa	TIM3_CH3, TSC_G3_IO2, TIM1_CH2N, EVENTOUT	ADC1_IN11, COMP4_INP, OPAMP2_VINP
15	19	27	PB1	I/O	TTa	TIM3_CH4, TSC_G3_IO3, TIM1_CH3N, COMP4_OUT, HRTIM1_SCOUT, EVENTOUT	ADC1_IN12
-	20	28	PB2	I/O	TTa	TSC_G3_IO4, HRTIM_SCIN, EVENTOUT	ADC2_IN12, COMP4_INM
-	21	29	PB10	I/O	TT	TIM2_CH3, TSC_SYNC, USART3_TX, HRTIM1_FLT3, EVENTOUT	-
-	22	30	PB11	I/O	TTa	TIM2_CH4, TSC_G6_IO1, USART3_RX, HRTIM1_FLT4, EVENTOUT	COMP6_INP
16	23	31	VSS	S	-	Digital ground	
17	24	32	VDD	S	-	Digital power supply	
-	25	33	PB12	I/O	TTa	TSC_G6_IO2, TIM1_BKIN, USART3_CK, HRTIM1_CHC1, EVENTOUT	ADC2_IN13
-	26	34	PB13	I/O	TTa	TSC_G6_IO3, TIM1_CH1N, USART3_CTS, HRTIM1_CHC2, EVENTOUT	ADC1_IN13

Table 13. STM32F334x4/6/8 pin definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Pin functions	
LQFP 32	LQFP 48	LQFP 64				Alternate functions	Additional functions
-	27	35	PB14	I/O	TTa	TIM15_CH1, TSC_G6_IO4, TIM1_CH2N, USART3_RTS_DE, HRTIM1_CHD1, EVENTOUT	ADC2_IN14, OPAMP2_VINP
-	28	36	PB15	I/O	TTa	TIM15_CH2, TIM15_CH1N, TIM1_CH3N, HRTIM1_CHD2, EVENTOUT	ADC2_IN15, COMP6_INM, RTC_REFIN
-	-	37	PC6	I/O	FT	EVENTOUT, TIM3_CH1, HRTIM1_EEV10, COMP6_OUT	-
-	-	38	PC7	I/O	FT	EVENTOUT, TIM3_CH2, HRTIM1_FLT5	-
-	-	39	PC8	I/O	FT	EVENTOUT, TIM3_CH3, HRTIM1_CHE1	-
-	-	40	PC9	I/O	FT	EVENTOUT, TIM3_CH4, HRTIM1_CHE2	-
18	29	41	PA8	I/O	FT	MCO, TIM1_CH1, USART1_CK, HRTIM1_CHA1, EVENTOUT	-
19	30	42	PA9	I/O	FT	TSC_G4_IO1, TIM1_CH2, USART1_TX, TIM15_BKIN, TIM2_CH3, HRTIM1_CHA2, EVENTOUT	-
20	31	43	PA10	I/O	FT	TIM17_BKIN, TSC_G4_IO2, TIM1_CH3, USART1_RX, COMP6_OUT, TIM2_CH4, HRTIM1_CHB1, EVENTOUT	-
21	32	44	PA11	I/O	FT	TIM1_CH1N, USART1_CTS, CAN_RX, TIM1_CH4, TIM1_BKIN2, HRTIM1_CHB2, EVENTOUT	-
22	33	45	PA12	I/O	FT	TIM16_CH1, TIM1_CH2N, USART1_RTS_DE, COMP2_OUT, CAN_TX, TIM1_ETR, HRTIM1_FLT1, EVENTOUT	-

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3 σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V, V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

6.1.5 Input voltage on a pin

The input voltage measurement on a pin of the device is described in *Figure 9*.

Figure 8. Pin loading conditions

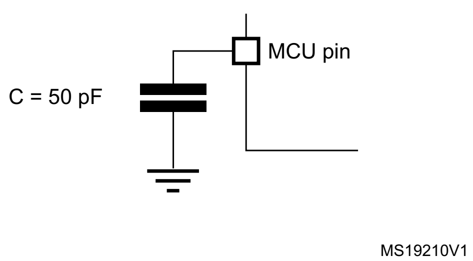


Figure 9. Pin input voltage

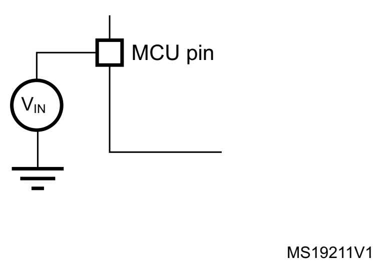


Table 26. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ.	Max. @ T_A (2)			Typ.	Max. @ T_A (2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run/Sleep mode, code executing from Flash or RAM	HSE bypass	72 MHz	224	252(3)	265	269(3)	245	272(3)	288	295(3)	µA
			64 MHz	196	225	237	241	214	243	257	263	
			48 MHz	147	174	183	186	159	186	196	201	
			32 MHz	100	126	133	135	109	133	142	145	
			24 MHz	79	102	107	108	85	108	113	116	
			8 MHz	3	5	5	6	4	6	6	7	
			1 MHz	3	5	5	6	3	5	6	6	
		HSI clock	64 MHz	259	288	304	309	285	315	332	338	
			48 MHz	208	239	251	254	230	258	271	277	
			32 MHz	162	190	198	202	179	206	216	219	
			24 MHz	140	168	175	178	155	181	188	191	
			8 MHz	62	85	88	89	71	94	96	98	

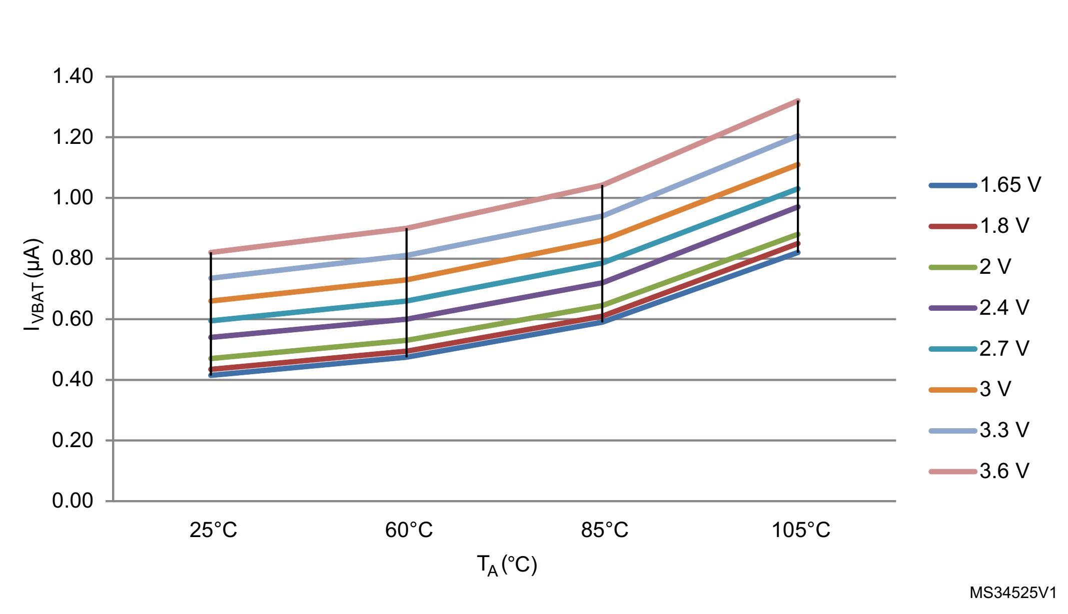
1. Current consumption from the V_{DDA} supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production.
3. Data based characterization results and tested in production with code executing from RAM.

Table 27. Typical and maximum V_{DD} consumption in Stop and Standby modes

Symbol	Parameter	Conditions	Typ. @V_{DD} (V_{DD}=V_{DDA})						Max.(1)			Unit
			2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF	17.51	17.68	17.84	18.17	18.57	19.39	30.6	232.5	612.2	µA
		Regulator in low-power mode, all oscillators OFF	6.44	6.51	6.60	6.73	6.96	7.20	20.0	246.4	585.0	
	Supply current in Standby mode	LSI ON and IWDG ON	0.73	0.89	1.02	1.14	1.28	1.44	-	-	-	
		LSI OFF and IWDG OFF	0.55	0.66	0.75	0.85	0.93	1.01	4.9	7.0	7.9	

1. Data based on characterization results, not tested in production unless otherwise specified.

Figure 12. Typical V_{BAT} current consumption (LSE and RTC ON/LSEDRV[1:0] = ’00’)



Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 3.3$ V
- All I/O pins available on each package are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz), and Flash prefetch is ON
- When the peripherals are enabled, $f_{APB1} = f_{AHB/2}$, $f_{APB2} = f_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8,16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz and 125 kHz respectively.

6.3.10 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 43. Flash memory characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.[1]	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (2 KB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design, not tested in production.

Table 44. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min.[1]	
N_{END}	Endurance	TA = –40 to +85 °C (6 suffix versions) TA = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle[2] at T_A = 85 °C	30	Years
		1 kcycle[2] at T_A = 105 °C	10	
		10 kcycles[2] at T_A = 55 °C	20	

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 45*. They are based on the EMS levels and classes defined in application note AN1709.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 μA/+0 μA range), or other functional failure (for example reset occurrence or oscillator frequency deviation). The test results are given in *Table 49: I/O current injection susceptibility*.

Table 49. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	– 0	NA	mA
	Injected current on PC0, PC1, PC2, PC3 (TTa pins) and PF1 pin (FT pin)	-0	+5	
	Injected current on PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7, PC4, PC5, PB0, PB1, PB2, PB12, PB13, PB14, PB15 with induced leakage current on other pins from this group less than -100 μA or more than +900 μA	-5	+5	
	Injected current on PB11, other TT, FT, and FTf pins	– 5	NA	
	Injected current on all other TC, TTa and RESET pins	– 5	+5	

Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under the conditions summarized in *Table 19*. All I/Os are CMOS and TTL compliant.

Table 50. I/O static characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	TT, TC and TTa I/O	-	-	$0.3\ V_{DD}+0.07$ (1)	V
		FT and FTf I/O	-	-	$0.475\ V_{DD}-0.2$ (1)	
		BOOT0	-	-	$0.3\ V_{DD}-0.3$ (1)	
		All I/Os except BOOT0	-	-	$0.3\ V_{DD}$ (2)	
V_{IH}	High level input voltage	TTa and TT I/O	$0.445\ V_{DD}+0.398$ (1)	-	-	
		FT and FTf I/O	$0.5\ V_{DD+0.2}$ (1)	-	-	
		BOOT0	$0.2\ V_{DD}+0.95$ (1)	-	-	
		All I/Os except BOOT0	$0.7\ V_{DD}$ (2)	-	-	

Table 50. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{hys}	Schmitt trigger hysteresis	TT, TC and TTa I/O	-	200 (1)	-	mV
		FT and FTf I/O	-	100 (1)	-	
		BOOT0	-	300 (1)	-	
I_{lkg}	Input leakage current (3)	TC, FT, TT, FTf and TTa I/O in digital mode $V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±0.1	µA
		TTa I/O in digital mode $V_{DD} \leq V_{IN} \leq V_{DDA}$	-	-	1	
		TTa I/O in analog mode $V_{SS} \leq V_{IN} \leq V_{DDA}$	-	-	±0.2	
		FT and FTf I/O(4) $V_{DD} \leq V_{IN} \leq 5$ V	-	-	10	
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation.
2. Tested in production.
3. Leakage could be higher than the maximum value. if negative current is injected on adjacent pins. Refer to *Table 49: I/O current injection susceptibility*.
4. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up/pull-down resistors must be disabled.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 18* and *Figure 19* for standard I/Os.

Figure 18. TC and TTa I/O input characteristics - CMOS port

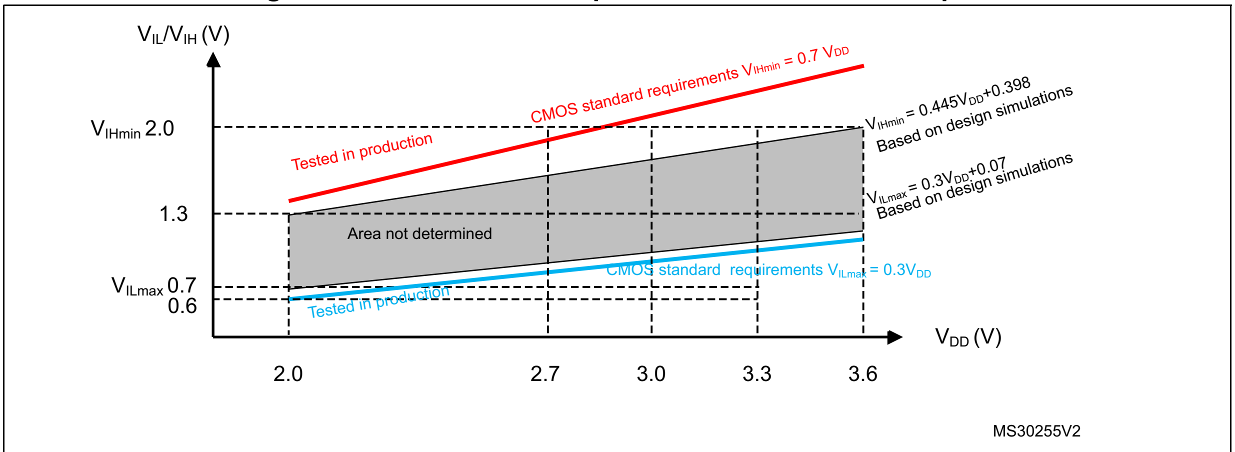


Figure 19. TC and TTa I/O input characteristics - TTL port

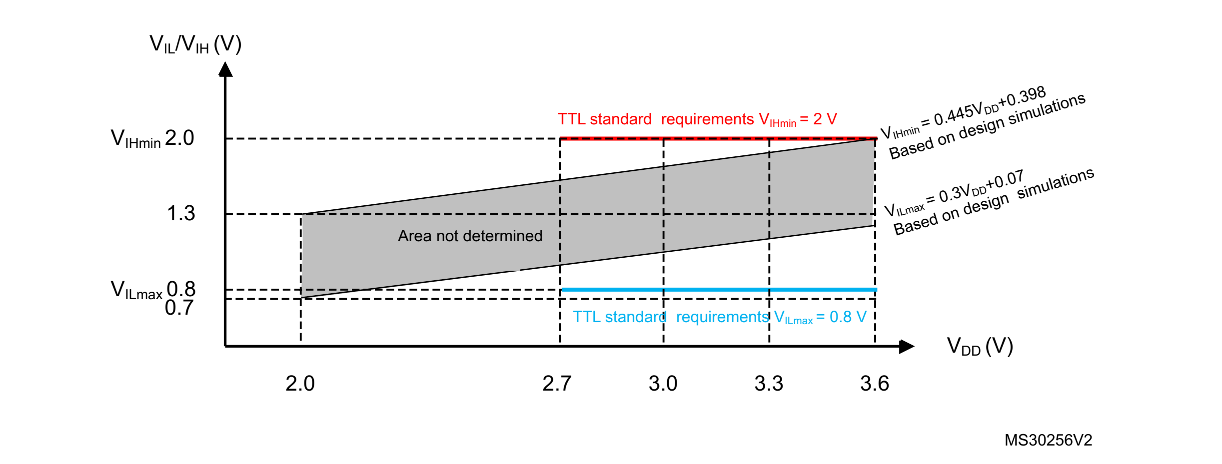


Figure 20. Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port

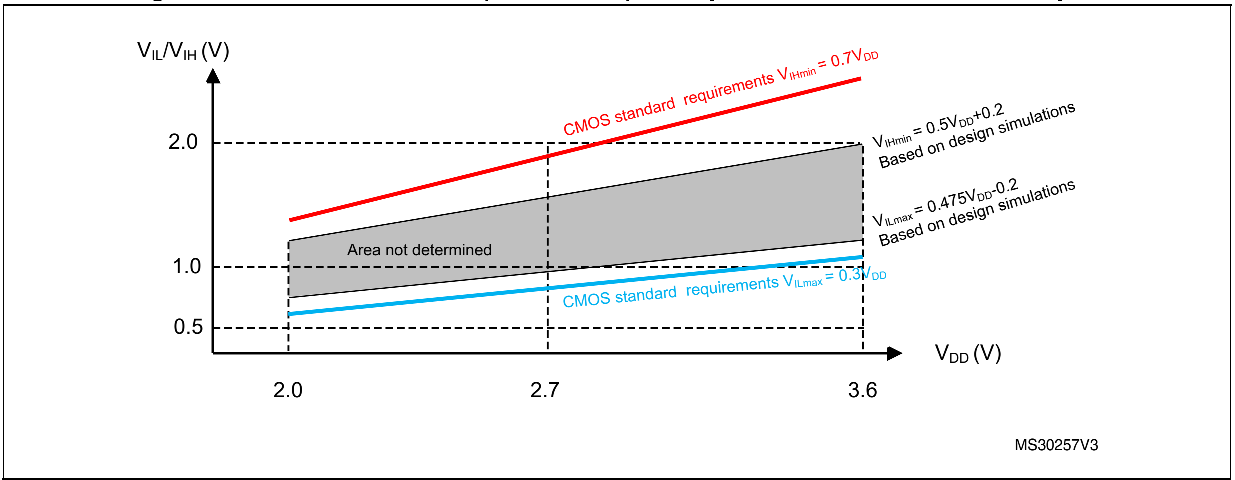
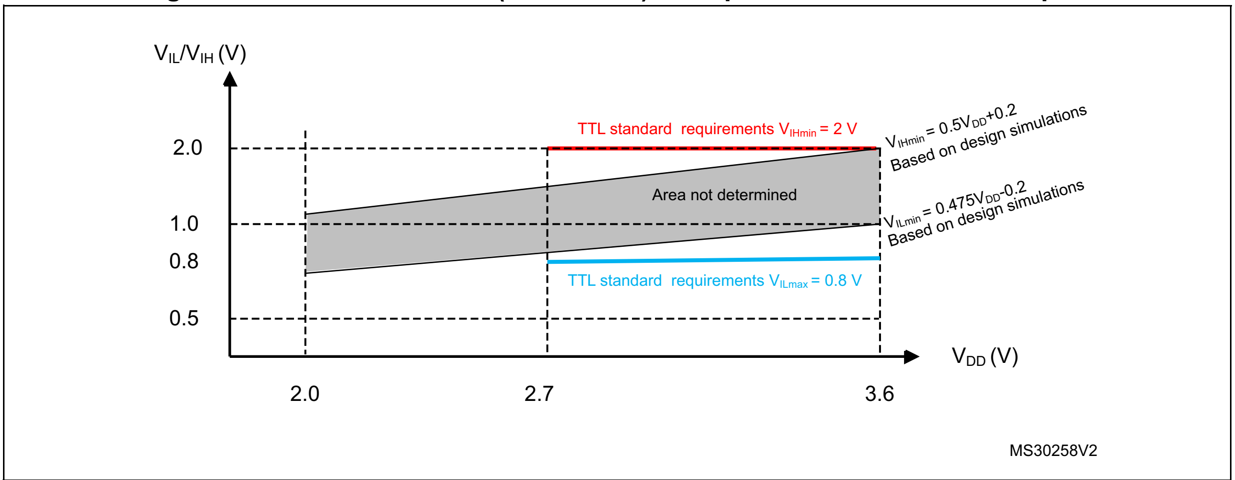


Figure 21. Five volt tolerant (FT and FTf) I/O input characteristics - TTL port



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in Section 6.2:

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see Table 17).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see Table 17).

Output voltage levels

Unless otherwise specified, the parameters given in Table 47: ESD absolute maximum ratings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 19. All I/Os (FT, TTa and TC unless otherwise specified) are CMOS and TTL compliant.

Table 51. Output voltage characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	
V_{OH} (3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH}(3)(4)	Output high level voltage for an I/O pin		V_{DD}–1.3	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	
V_{OH}(3)(4)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OLFM+}(1)(4)	Output low level voltage for an FTf I/O pin in FM+ mode	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in Table 17 and the sum of I_{IO} (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in Table 17 and the sum of I_{IO} (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
4. Data based on design simulation.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in Figure 22 and Table 66, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 19.

Table 55. HRTIM output response to fault protection[1]

Symbol	Parameter	Conditions	Min	Typ.	Max.[2]	Unit
$t_{LAT(DF)}$	Digital fault response latency	Propagation delay from HRTIM1_FLTx digital input to HRTIM_CHxy output pin	-	12	25	ns
$t_{W(FLT)}$	Minimum Fault pulse width	-	12.5	-	-	
$t_{LAT(AF)}$	Analog fault response latency	Propagation delay from comparator COMPx_INP input pin to HRTIM_CHxy output pin	-	25	43	

1. Refer to Fault paragraph in HRTIM section of RM0364.
2. Data based on characterization results, not tested in production.

Table 56. HRTIM output response to external events 1 to 5 (Low-Latency mode[1])

Symbol	Parameter	Conditions	Min	Typ.	Max.[2]	Unit
$t_{LAT(DEEV)}$	Digital external event response latency	Propagation delay from HRTIM1_EEVx digital input to HRTIM_CHxy output pin (30pF load)	-	12	25	ns
$t_{W(FLT)}$	Minimum external event pulse width	-	12.5	-	-	ns
$t_{LAT(AEEV)}$	Analog external event response latency	Propagation delay from comparator COMPx_INP input pin to HRTIM_CHxy output pin (30pF load)	-	25	43	ns
$T_{JIT(EEV)}$	External event response jitter	Jitter of the delay from HRTIM1_EEVx digital input or COMPx_INP input pin to HRTIM_CHxy output pin	-	-	0	t_{HRTIM}[3]
$T_{JIT(PW)}$	Jitter on output pulse width in response to an external event	-	-	-	1	t_{HRTIM}[3]

1. EExFAST bit in HRTIM_EECR1 register is set (Low Latency mode). This functionality is available on external events channels 1 to 5. Refer to Latency to external events paragraph in HRTIM section of RM0364.
2. Data based on characterization results, not tested in production.
3. T_{HRTIM} = 1 / f_{HRTIM} with f_{HRTIM}= 144 MHz or f_{HRTIM} = 128 MHZ depending on the clock controller configuration. (Refer to Reset and clock control section in RM0364.)

Table 69. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DNL(3)	Differential non linearity Difference between two consecutive code-1LSB)	Given for a 10-bit input code DAC1 channel 1	-	-	±0.5	LSB
		Given for a 12-bit input code DAC1 channel 1	-	-	±2	LSB
		Given for a 10-bit input code DAC1 channel 2 & DAC2 channel 1	-	-	-0.75/+0.25	LSB
		Given for a 12-bit input code DAC1 channel 2 & DAC2 channel 1	-	-	-3/+1	LSB
INL(3)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095)	Given for a 10-bit input code	-	-	±1	LSB
		Given for a 12-bit input code	-	-	±4	LSB
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{DDA}/2$)	-	-	-	±10	mV
		Given for a 10-bit input code at V_{DDA} = 3.6 V	-	-	±3	LSB
		Given for a 12-bit input code	-	-	±12	LSB
Gain error(3)	Gain error	Given for a 12-bit input code	-	-	±0.5	%
$t_{SETTLING}$(3)	Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ	-	3	4	µs
Update rate(3)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ	-	-	1	MS/s
I_{skink}	Output sink current	DAC buffer ON Output level higher than 0.2 V	100	-	-	µA
t_{WAKEUP}(3)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ	-	6.5	10	µs
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	No R_{LOAD}, C_{LOAD} = 50 pF	-	–67	–40	dB

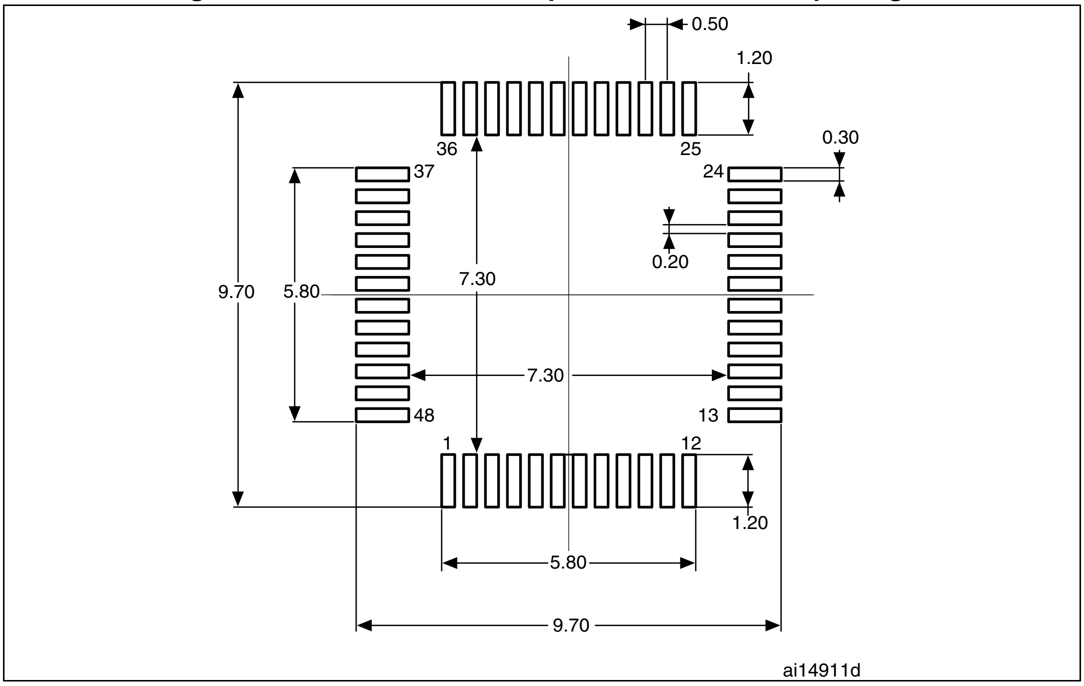
1. Guaranteed by design, not tested in production.
2. Quiescent mode refers to the state of the DAC a keeping steady value on the output, so no dynamic consumption is involved.
3. Data based on characterization results, not tested in production.

Table 76. LQFP48 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-		0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 37. Recommended footprint for the LQFP48 package

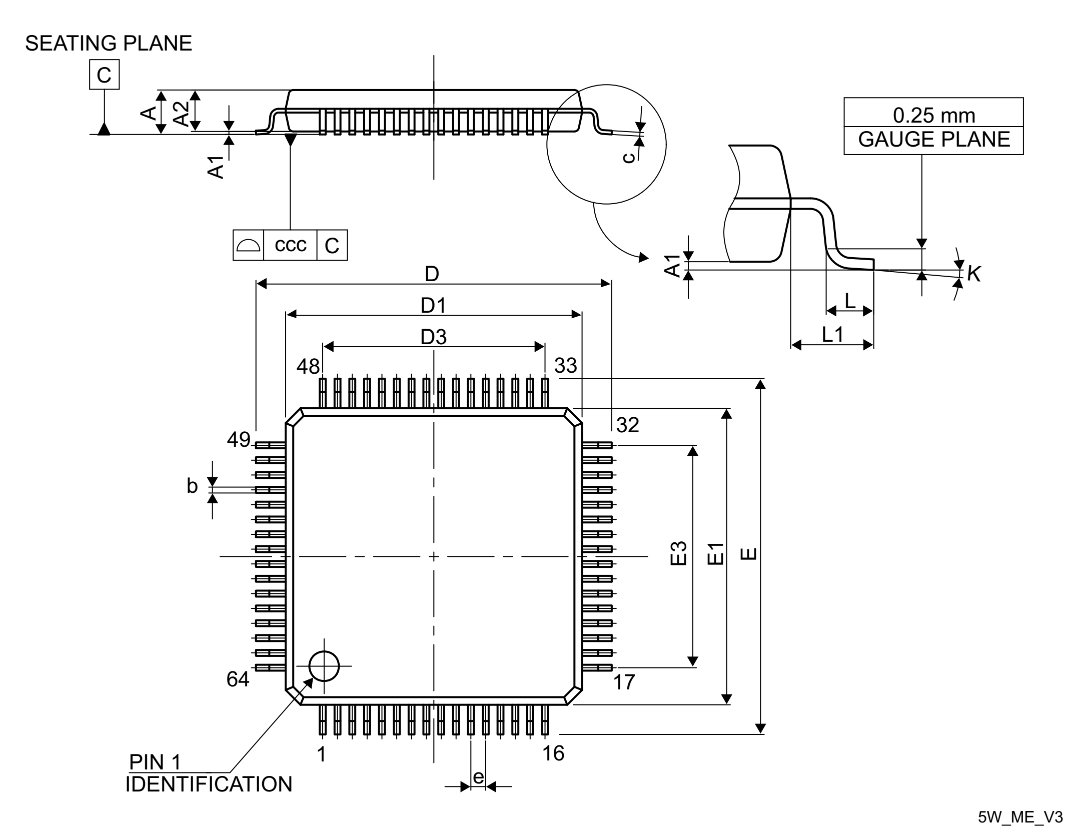


1. Drawing is not to scale.
2. Dimensions are in millimeters.

7.4 LQFP64 package information

LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package.

Figure 39. LQFP64 package outline



1. Drawing is not to scale.

Table 77. LQFP64 package mechanical data

Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	11.800	12.000	-	-	0.4724	-
D1	9.800	10.000	-	-	0.3937	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
e	-	0.500	-	-	0.0197	-