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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 15x12b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f334c6t7

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1 Introduction

This datasheet provides the ordering information and the mechanical device characteristics of the STM32F334x4/6/8 microcontrollers.

This document should be read in conjunction with the STM32F303xx reference manual RM0364 available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M4 core with FPU, refer to:

- ARM® Cortex®-M4 Processor Technical Reference Manual available from the www.arm.com website.
- STM32F3xxx and STM32F4xxx Cortex®-M4 programming manual (PM0214) available from the *www.st.com* website.

2 Description

The STM32F334x4/6/8 family incorporates the high-performance ARM® Cortex®-M4 32-bit RISC core operating at up to 72 MHz frequency embedding a floating point unit (FPU), high-speed embedded memories (up to 64 Kbytes of Flash memory, up to 12 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The STM32F334x4/6/8 microcontrollers offer two fast 12-bit ADCs (5 Msps), up to three ultra-fast comparators, an operational amplifier, three DAC channels, a low-power RTC, one high-resolution timer, one general-purpose 32-bit timer, one timer dedicated to motor control, and four general-purpose 16-bit timers. They also feature standard and advanced communication interfaces: one I^2C, one SPI, up to three USARTs and one CAN.

The STM32F334x4/6/8 family operates in the –40 to +85 °C and –40 to +105 °C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F334x4/6/8 family offers devices in 32, 48 and 64-pin packages.

Depending on the device chosen, different sets of peripherals are included.

Table 2. STM32F334x4/6/8 family device features and peripheral counts

Peripheral		STM32F334Kx			STM32F334Cx			STM32F334Rx		
Flash memory (Kbyte)		16	32	64	16	32	64	16	32	64
SRAM on data bus (Kbyte)		12								
Core coupled memory SRAM on instruction bus (CCM SRAM) (Kbyte)		4								
Timers	High-resolution timer	1 (16-bit / 10 channels)								
	Advanced control	1 (16-bit)								
	General purpose	4 (16-bit) 1 (32 bit)								
	Basic	2 (16-bit)								
	SysTick timer	1								
	Watchdog timers (independent, window)	2								
	PWM channels (all)(1)	20			26			28		
	PWM channels (except complementary)	14			20			22		

Table 2. STM32F334x4/6/8 family device features and peripheral counts (continued)

Peripheral		STM32F334Kx	STM32F334Cx	STM32F334Rx
Comm. interfaces	SPI	1		
	I^2C	1		
	USART	2	3	
	CAN	1		
GPIOs	Normal I/Os (TC, TTa)	10	20	26
	5-Volt tolerant I/Os (FT,FTf)	15	17	25
Capacitive sensing channels		14	17	18
DMA channels		7		
12-bit ADCs Number of channels		2 10	2 15	2 21
12-bit DAC channels		3		
Ultra-fast analog comparator		2	3	
Operational amplifiers		1		
CPU frequency		72 MHz		
Operating voltage		2.0 to 3.6 V		
Operating temperature		Ambient operating temperature: - 40 to 85 °C / - 40 to 105 °C Junction temperature: - 40 to 125 °C		
Packages		LQFP32	LQFP48	LQFP64

1. This total considers also the PWMs generated on the complementary output channels.

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed, following a specific sequence to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

3.8 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 7 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers, high-resolution timer, DAC and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F334x4/6/8 devices embed a nested vectored interrupt controller (NVIC) able to handle up to 60 interrupt channels, that can be masked and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The external interrupt/event controller consists of 27 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked

3.14.1 217 ps high-resolution timer (HRTIM1)

The high-resolution timer (HRTIM1) allows generating digital signals with high-accuracy timings, such as PWM or phase-shifted pulses.

It consists of 6 timers, 1 master and 5 slaves, totaling 10 high-resolution outputs, which can be coupled by pairs for deadtime insertion. It also features 5 fault inputs for protection purposes and 10 inputs to handle external events such as current limitation, zero voltage or zero current switching.

HRTIM1 timer is made of a digital kernel clocked at 144 MHz followed by delay lines. Delay lines with closed loop control guarantee a 217 ps resolution whatever the voltage, temperature or chip-to-chip manufacturing process deviation. The high-resolution is available on the 10 outputs in all operating modes: variable duty cycle, variable frequency, and constant ON time.

The slave timers can be combined to control multiswitch complex converters or operate independently to manage multiple independent converters.

The waveforms are defined by a combination of user-defined timings and external events such as analog or digital feedbacks signals.

HRTIM1 timer includes options for blanking and filtering out spurious events or faults. It also offers specific modes and features to offload the CPU: DMA requests, burst mode controller, push-pull and resonant mode.

It supports many topologies including LLC, Full bridge phase shifted, buck or boost converters, either in voltage or current mode, as well as lighting application (fluorescent or LED). It can also be used as a general purpose timer, for instance to achieve high-resolution PWM-emulated DAC.

In debug mode, the HRTIM1 counters can be frozen and the PWM outputs enter safe state.

3.14.2 Advanced timer (TIM1)

The advanced-control timer can be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timers (described in *Section 3.14.3* using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

Table 13. STM32F334x4/6/8 pin definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Pin functions	
LQFP 32	LQFP 48	LQFP 64				Alternate functions	Additional functions
28	41	57	PB5	I/O	FT	TIM16_BKIN, TIM3_CH2, I2C1_SMBA, SPI1_MOSI, USART2_CK, TIM17_CH1, HRTIM1_EEV6, EVENTOUT	-
29	42	58	PB6	I/O	FTf	TIM16_CH1N, TSC_G5_IO3, I2C1_SCL, USART1_TX, HRTIM1_SCIN, HRTIM1_EEV4, EVENTOUT	-
30	43	59	PB7	I/O	FTf	TIM17_CH1N, TSC_G5_IO4, I2C1_SDA, USART1_RX, TIM3_CH4, HRTIM1_EEV3, EVENTOUT	-
31	44	60	BOOT0	I	B	-	-
-	45	61	PB8	I/O	FTf	TIM16_CH1, TSC_SYNC, I2C1_SCL, USART3_RX, CAN_RX, TIM1_BKIN, HRTIM1_EEV8, EVENTOUT	-
-	46	62	PB9	I/O	FTf	TIM17_CH1, I2C1_SDA, IR_OUT, USART3_TX, COMP2_OUT, CAN_TX, HRTIM1_EEV5, EVENTOUT	-
32	47	63	VSS	S	-	-	-
1	48	64	VDD	S	-	-	-

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch sinks only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
   After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the reference manual.
2. Fast ADC channel.
3. These GPIOs offer a reduced touch sensing sensitivity. It is thus recommended to use them as sampling capacitor I/O.

Table 14. Alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/TIM15/ TIM16/TIM17/ EVENT	TIM1/TIM3/ TIM15/ TIM16	HRTIM1/TSC	I2C1/TIM1	SPI1/Infrared	TIM1/Infrared	USART1/USART2/USART3/ GPCOMP6	GPCOMP2/ GPCOMP4/ GPCOMP6	CAN/TIM1/ TIM15	TIM2/TIM3 /TIM17	TIM1	HRTIM1/ TIM1	HRTIM1/ OPAMP2	-	EVENT
Port B	PB10	-	TIM2_CH3	-	TSC_SYNC	-	-	-	USART3_TX	-	-	-	-	-	HRTIM1_FLT3	-	EVENTOUT
	PB11	-	TIM2_CH4	-	TSC_G6_IO1	-	-	-	USART3_RX	-	-	-	-	-	HRTIM1_FLT4	-	EVENTOUT
	PB12	-	-	-	TSC_G6_IO2	-	-	TIM1_BKIN	USART3_CK	-	-	-	-	-	HRTIM1_CHC1	-	EVENTOUT
	PB13	-	-	-	TSC_G6_IO3	-	-	TIM1_CH1N	USART3_CTS	-	-	-	-	-	HRTIM1_CHC2	-	EVENTOUT
	PB14	-	TIM15_CH1	-	TSC_G6_IO4	-	-	TIM1_CH2N	USART3_RTS_DE	-	-	-	-	-	HRTIM1_CHD1	-	EVENTOUT
	PB15	-	TIM15_CH2	TIM15_CH1N	-	TIM1_CH3N	-	-	-	-	-	-	-	-	HRTIM1_CHD2	-	EVENTOUT
Port C	PC0	-	EVENTOUT	TIM1_CH1	-	-	-	-	-	-	-	-	-	-	-	-	-
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC2	-	EVENTOUT	TIM1_CH3	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC3	-	EVENTOUT	TIM1_CH4	-	-	-	TIM1_BKIN2	-	-	-	-	-	-	-	-	-
	PC4	-	EVENTOUT	TIM1_ETR	-	-	-	-	USART1_TX	-	-	-	-	-	-	-	-
	PC5	-	EVENTOUT	TIM15_BKIN	TSC_G3_IO1	-	-	-	USART1_RX	-	-	-	-	-	-	-	-
	PC6	-	EVENTOUT	TIM3_CH1	HRTIM1_EEV10	-	-	-	COMP6_OUT	-	-	-	-	-	-	-	-
	PC7	-	EVENTOUT	TIM3_CH2	HRTIM1_FLT5	-	-	-	-	-	-	-	-	-	-	-	-
	PC8	-	EVENTOUT	TIM3_CH3	HRTIM1_CHE1	-	-	-	-	-	-	-	-	-	-	-	-
	PC9	-	EVENTOUT	TIM3_CH4	HRTIM1_CHE2	-	-	-	-	-	-	-	-	-	-	-	-
	PC10	-	EVENTOUT	-	-	-	-	-	USART3_TX	-	-	-	-	-	-	-	-
	PC11	-	EVENTOUT	-	HRTIM1_EEV2	-	-	-	USART3_RX	-	-	-	-	-	-	-	-
	PC12	-	EVENTOUT	-	HRTIM1_EEV1	-	-	-	USART3_CK	-	-	-	-	-	-	-	-
	PC13	-	-	-	-	TIM1_CH1N	-	-	-	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Port D	PD2	-	EVENTOUT	TIM3_ETR	-	-	-	-	-	-	-	-	-	-	-	-	-
Port F	PF0	-	-	-	-	-	-	TIM1_CH3N	-	-	-	-	-	-	-	-	-
	PF1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Table 26. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ.	Max. @ T_A(2)			Typ.	Max. @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run/Sleep mode, code executing from Flash or RAM	HSE bypass	72 MHz	224	252(3)	265	269(3)	245	272(3)	288	295(3)	µA
			64 MHz	196	225	237	241	214	243	257	263	
			48 MHz	147	174	183	186	159	186	196	201	
			32 MHz	100	126	133	135	109	133	142	145	
			24 MHz	79	102	107	108	85	108	113	116	
			8 MHz	3	5	5	6	4	6	6	7	
			1 MHz	3	5	5	6	3	5	6	6	
		HSI clock	64 MHz	259	288	304	309	285	315	332	338	
			48 MHz	208	239	251	254	230	258	271	277	
			32 MHz	162	190	198	202	179	206	216	219	
			24 MHz	140	168	175	178	155	181	188	191	
			8 MHz	62	85	88	89	71	94	96	98	

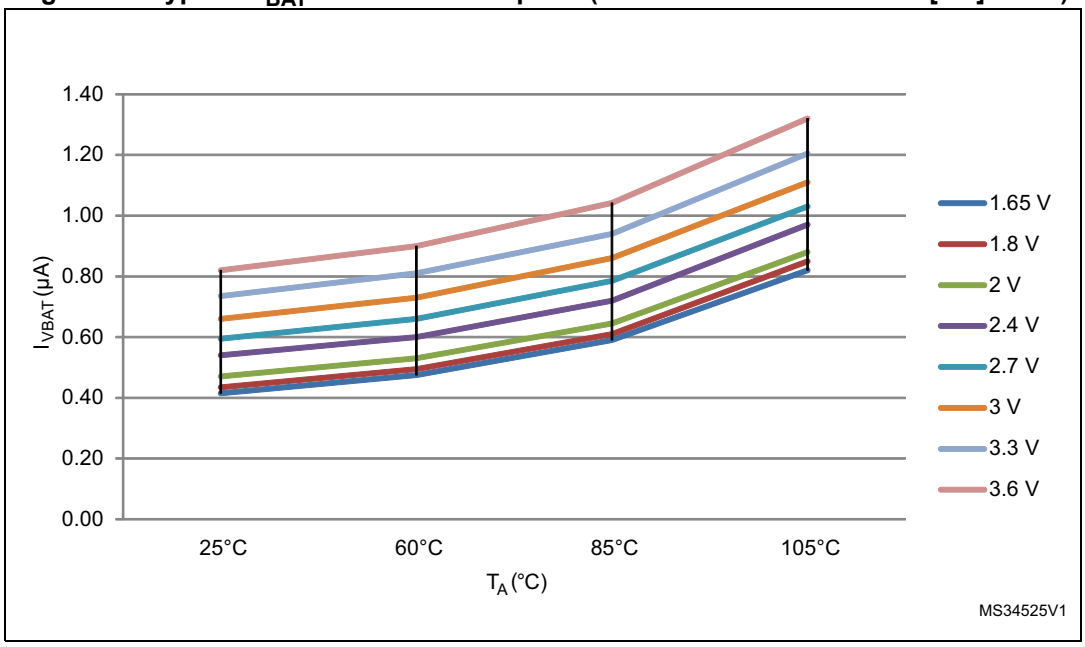
1. Current consumption from the V_{DDA} supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production.
3. Data based characterization results and tested in production with code executing from RAM.

Table 27. Typical and maximum V_{DD} consumption in Stop and Standby modes

Symbol	Parameter	Conditions	Typ. @V_{DD} (V_{DD}=V_{DDA})						Max.(1)			Unit
			2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF	17.51	17.68	17.84	18.17	18.57	19.39	30.6	232.5	612.2	µA
		Regulator in low-power mode, all oscillators OFF	6.44	6.51	6.60	6.73	6.96	7.20	20.0	246.4	585.0	
	Supply current in Standby mode	LSI ON and IWDG ON	0.73	0.89	1.02	1.14	1.28	1.44	-	-	-	
		LSI OFF and IWDG OFF	0.55	0.66	0.75	0.85	0.93	1.01	4.9	7.0	7.9	

1. Data based on characterization results, not tested in production unless otherwise specified.

Figure 12. Typical V_{BAT} current consumption (LSE and RTC ON/LSEDRV[1:0] = '00')



Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 3.3$ V
- All I/O pins available on each package are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz), and Flash prefetch is ON
- When the peripherals are enabled, $f_{APB1} = f_{AHB/2}$, $f_{APB2} = f_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8,16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz and 125 kHz respectively.

Table 30. Typical current consumption in Run mode, code with data processing running from Flash memory

Symbol	Parameter	Conditions	f_{HCLK}	Typ.		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash	72 MHz	70.6	25.2	mA
			64 MHz	60.3	22.6	
			48 MHz	46.0	17.3	
			32 MHz	31.3	12.0	
			24 MHz	25.0	9.3	
			16 MHz	16.2	6.5	
			8 MHz	8.4	3.55	
			4 MHz	4.75	2.21	
			2 MHz	2.81	1.52	
			1 MHz	1.82	1.17	
			500 kHz	1.34	0.94	
			125 kHz	0.93	0.82	
I_{DDA} (1) (2)	Supply current in Run mode from V_{DDA} supply		72 MHz	240.0	234.0	µA
			64 MHz	209.9	208.6	
			48 MHz	154.5	153.5	
			32 MHz	104.1	103.6	
			24 MHz	80.2	80.0	
			16 MHz	56.8	56.6	
			8 MHz	1.14	1.14	
			4 MHz	1.14	1.14	
			2 MHz	1.14	1.14	
			1 MHz	1.14	1.14	
			500 kHz	1.14	1.14	
			125 kHz	1.14	1.14	

1. V_{DDA} supervisor is OFF.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

Table 31. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ.		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Sleep mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM	72 MHz	51.8	6.3	mA
			64 MHz	46.4	5.7	
			48 MHz	35.0	4.40	
			32 MHz	23.7	3.13	
			24 MHz	18.0	2.49	
			16 MHz	12.2	1.85	
			8 MHz	6.2	0.99	
			4 MHz	3.68	0.88	
			2 MHz	2.26	0.80	
			1 MHz	1.55	0.76	
			500 kHz	1.20	0.74	
			125 kHz	0.89	0.72	
I_{DDA} (1) (2)	Supply current in Sleep mode from V_{DDA} supply		72 MHz	239.0	236.7	µA
			64 MHz	209.4	207.8	
			48 MHz	154.0	152.9	
			32 MHz	103.7	103.2	
			24 MHz	80.1	79.8	
			16 MHz	56.7	56.6	
			8 MHz	1.14	1.14	
			4 MHz	1.14	1.14	
			2 MHz	1.14	1.14	
			1 MHz	1.14	1.14	
			500 kHz	1.14	1.14	
			125 kHz	1.14	1.14	

1. V_{DDA} supervisor is OFF.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 50: I/O static characteristics*.

6.3.6 Wakeup time from low-power mode

The wakeup times given in *Table 34* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep mode: the wakeup event is WFE.
- WKUP1 (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 19*.

Table 34. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ. @V_{DD}, V_{DD} = V_{DDA}						Max.	Unit
			2.0 V	2.4 V	2.7 V	3 V	3.3 V	3.6 V		
t_{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	4.3	4.1	4.0	3.9	3.8	3.7	4.5	µs
		Regulator in low-power mode	7.8	6.7	6.1	5.9	5.5	5.3	9	
$t_{WUSTANDBY}$(1)	Wakeup from Standby mode	LSI and IWDG OFF	74.4	64.3	60.0	56.9	54.3	51.1	103	
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	6						-	CPU clock cycles

1. Data based on characterization results, not tested in production.

Table 35. Wakeup time using USART

Symbol	Parameter	Conditions	Typ	Max	Unit
tWUUSART	Wakeup time needed to calculate the maximum USART baudrate allowing to wakeup up from stop mode when USART clock source is HSI	Stop mode with main regulator in low power mode	-	13.125	µs
		Stop mode with main regulator in run mode	-	3.125	

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 13*.

Figure 19. TC and TTa I/O input characteristics - TTL port

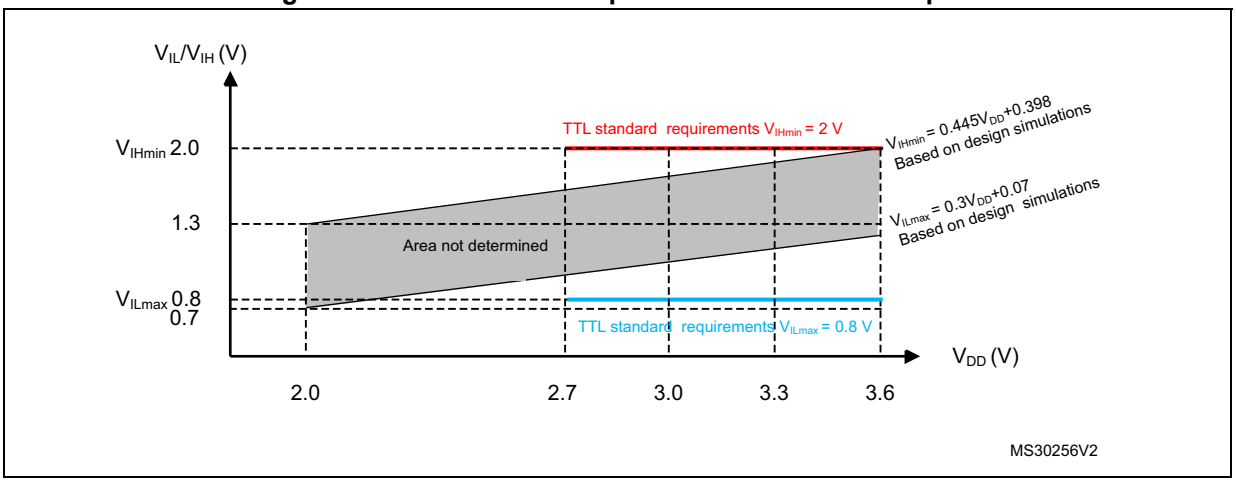


Figure 20. Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port

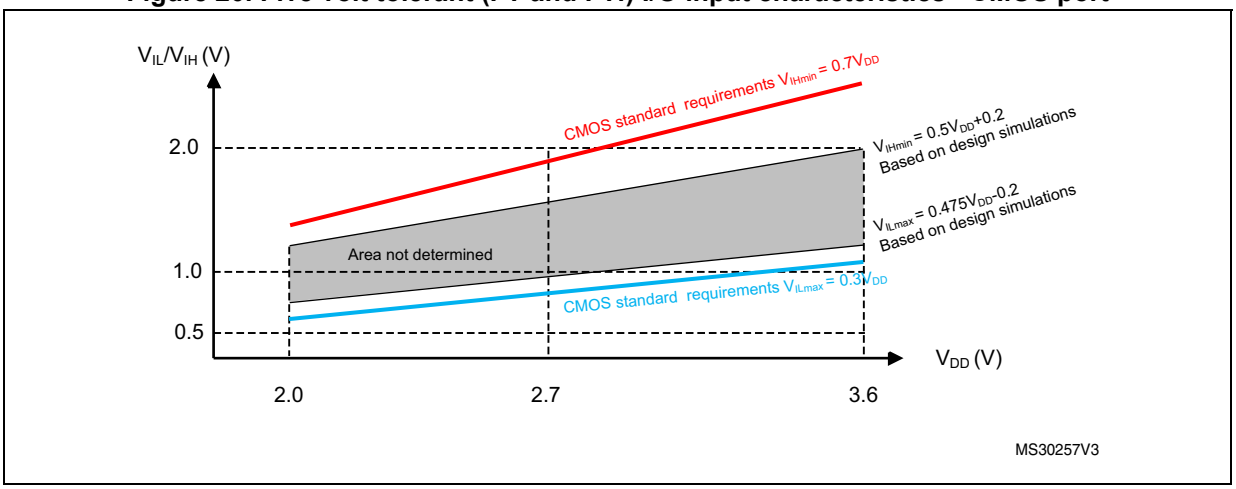


Figure 21. Five volt tolerant (FT and FTf) I/O input characteristics - TTL port

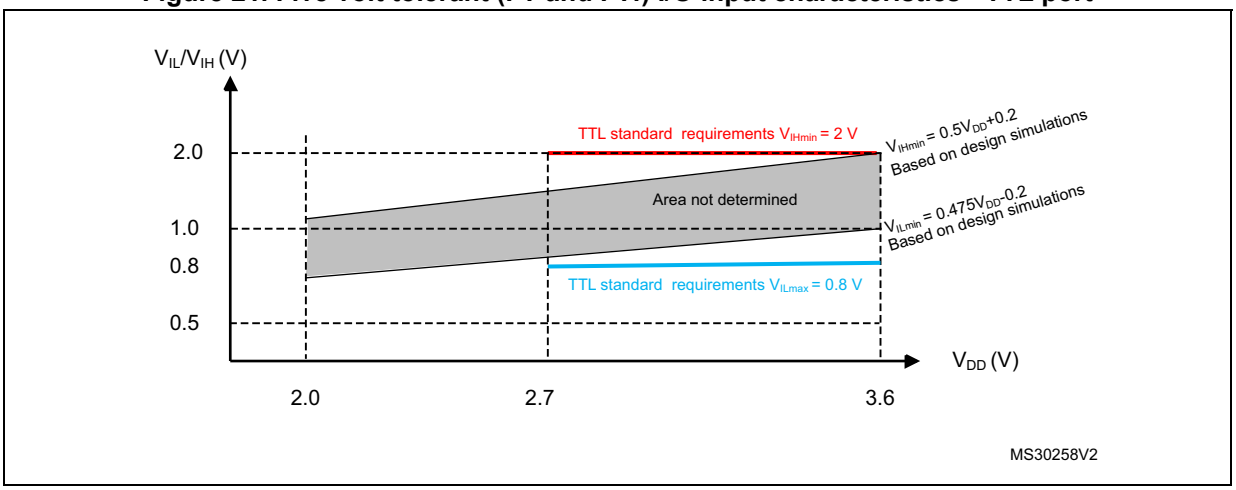


Table 60. IWDG min./max. timeout period at 40 kHz (LSI) (1)

Prescaler divider	PR[2:0] bits	Min. timeout (ms) RL[11:0]= 0x000	Max. timeout (ms) RL[11:0]= 0xFFF
/4	0	0.1	409.6
/8	1	0.2	819.2
/16	2	0.4	1638.4
/32	3	0.8	3276.8
/64	4	1.6	6553.6
/128	5	3.2	13107.2
/256	7	6.4	26214.4

1. These timings are given for a 40 kHz clock but the microcontroller's internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 61. WWDG min./max. timeout value at 72 MHz (PCLK)(1)

Prescaler	WDGTB	Min. timeout value	Max. timeout value
1	0	0.05687	3.6409
2	1	0.1137	7.2817
4	2	0.2275	14.564
8	3	0.4551	29.127

1. Guaranteed by design, not tested in production.

6.3.18 Communication interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 Kbit/s
- Fast-mode (Fm): with a bit rate up to 400 Kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I²C peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDD is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.14: I/O port characteristics* for the I²C I/O characteristics.

All I²C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 64. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{CONV}(1)	Total conversion time (including sampling time)	f_{ADC} = 72 MHz Resolution = 12 bits	0.19	-	8.52	µs
		Resolution = 12 bits	14 to 614 (t_S for sampling + 12.5 for successive approximation)			$1/f_{ADC}$
CMIR	Common Mode Input signal	ADC differential mode	(V_{SSA}+V_{REF}+)/2 -0.18	(V_{SSA} + V_{REF}+)/2	(V_{SSA} + V_{REF}+)/2 + 0.18	V

1. Data guaranteed by design, not tested in production.

Figure 27. ADC typical current consumption in single-ended and differential modes

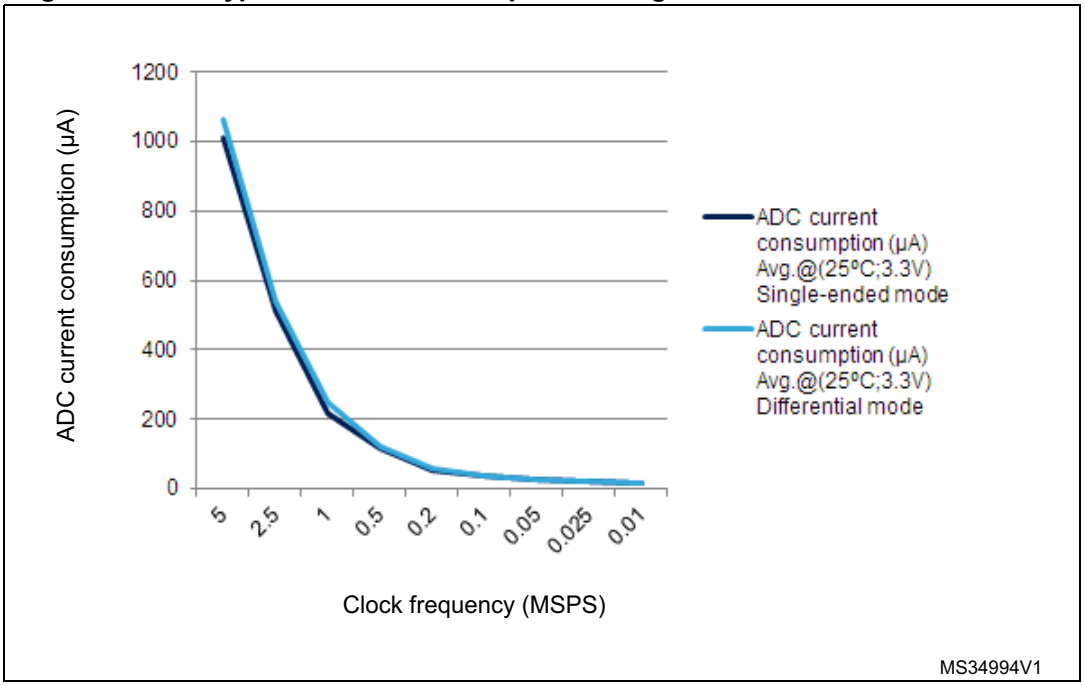


Table 65. Maximum ADC R_{AIN}(1)

Resolution	Sampling cycle @ 72 MHz	Sampling time [ns] @ 72 MHz	R_{AIN} max. (kΩ)		
			Fast channels(2)	Slow channels	Other channels(3)
12 bits	1.5	20.83	0.018	NA	NA
	2.5	34.72	0.150	NA	0.022
	4.5	62.50	0.470	0.220	0.180
	7.5	104.17	0.820	0.560	0.470
	19.5	270.83	2.70	1.80	1.50
	61.5	854.17	8.20	6.80	4.70
	181.5	2520.83	22.0	18.0	15.0
	601.5	8354.17	82.0	68.0	47.0

7 Package information

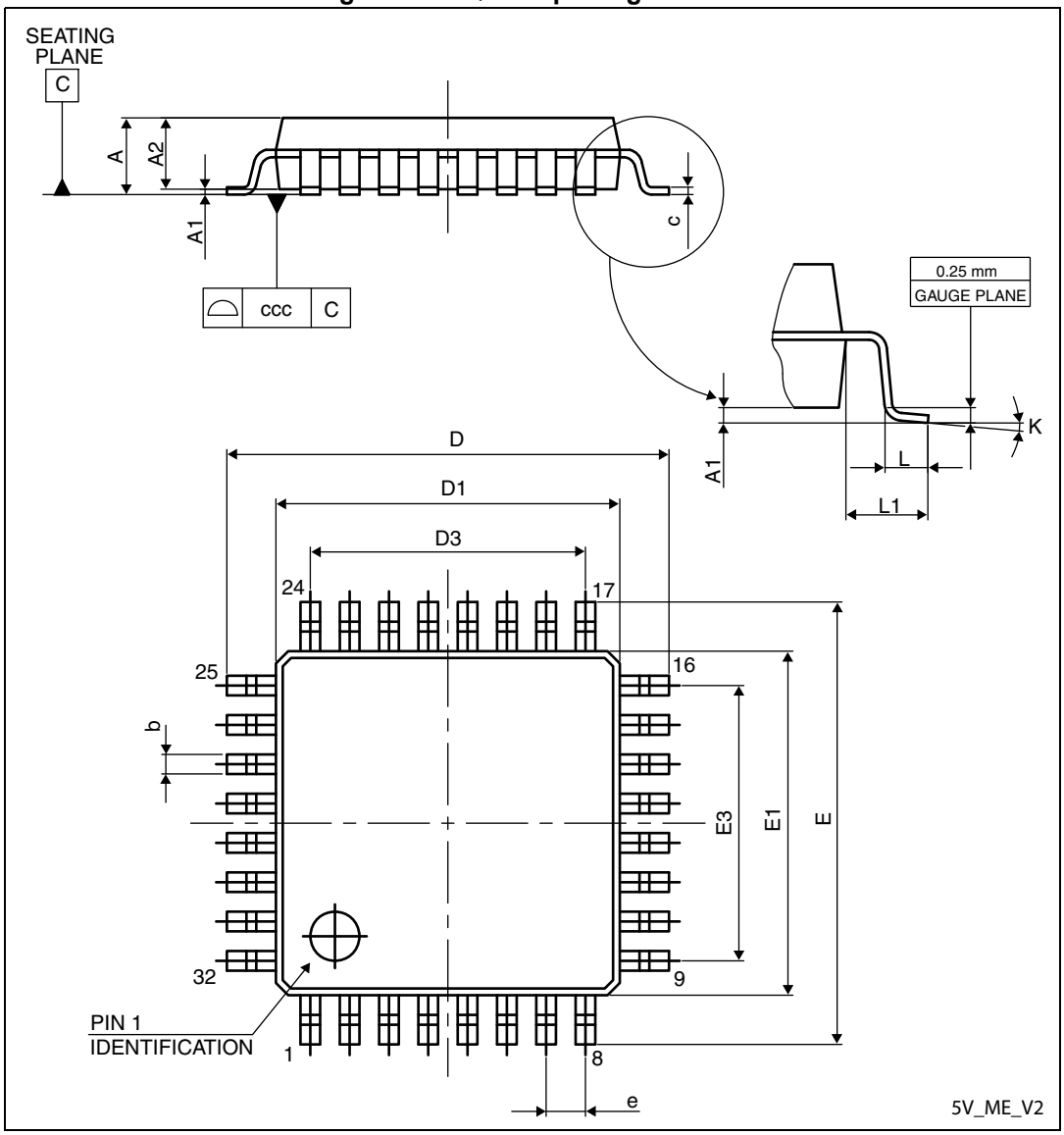
7.1 Package mechanical data

To meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.2 LQFP32 package information

LQFP32 is a 32-pin, 7 x 7mm low-profile quad flat package.

Figure 33. LQFP32 package outline



1. Drawing is not to scale.

Table 75. LQFP32 mechanical data

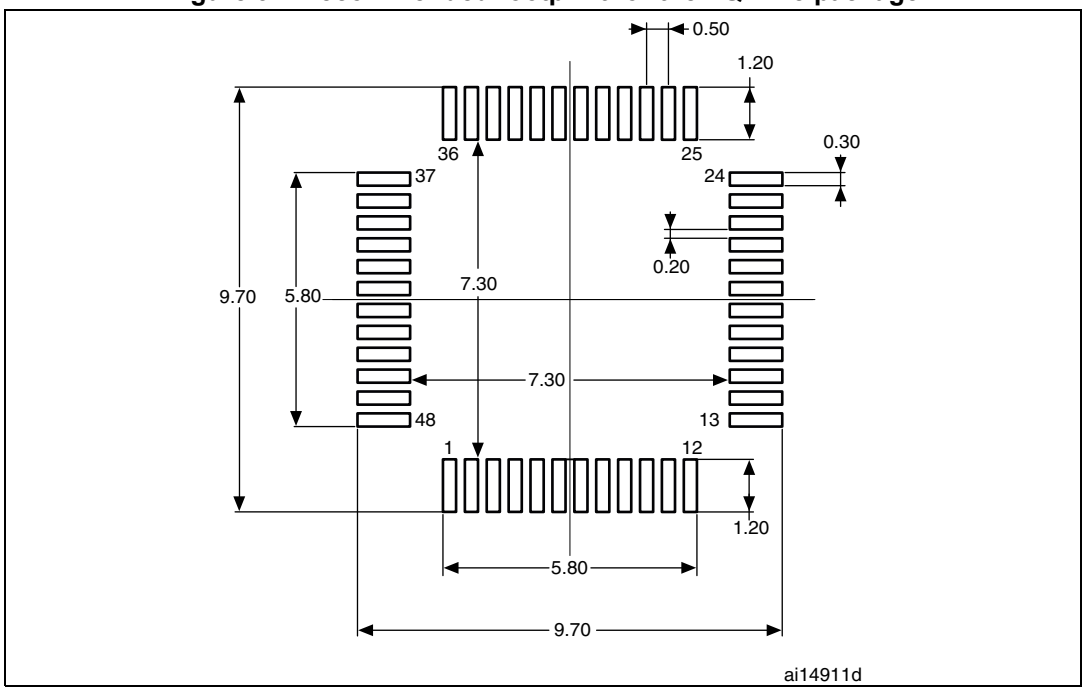
Symbol	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571

Table 76. LQFP48 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-		0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 37. Recommended footprint for the LQFP48 package

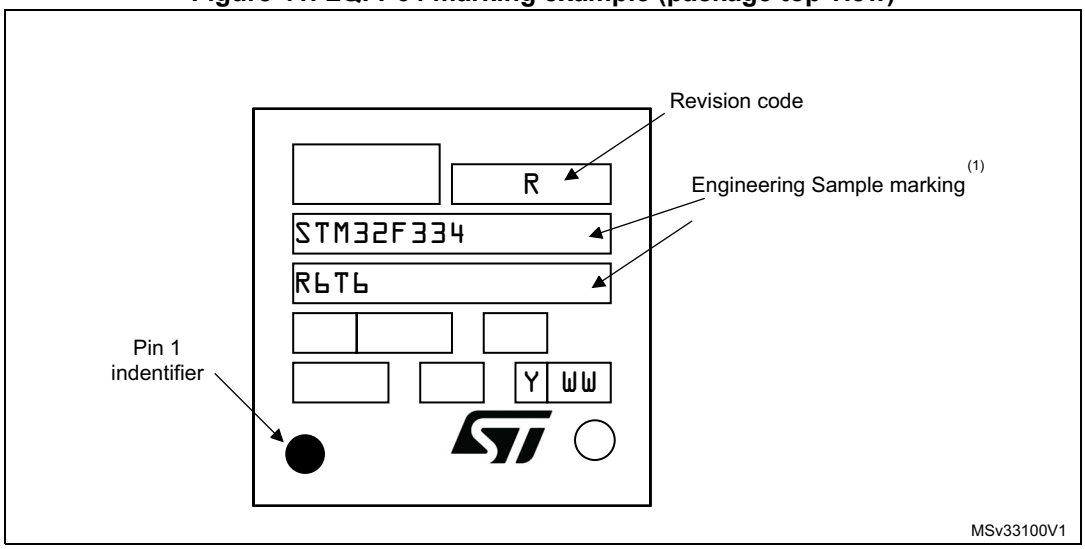


1. Drawing is not to scale.
2. Dimensions are in millimeters.

Device marking for LQFP64

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 41. LQFP64 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.