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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 15x12b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f334c6t7tr

  - Up to 3 USARTs, one with ISO/IEC 7816 interface, LIN, IrDA, modem control
- Debug mode: serial wire debug (SWD), JTAG
- 96-bit unique ID
- All packages ECOPACK®2

Table 1. Device summary

Reference	Part number
STM32F334Kx	STM32F334K4/K6/K8
STM32F334Cx	STM32F334C4/C6/C8
STM32F334Rx	STM32F334R4/R6/R8

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed, following a specific sequence to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

3.8 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 7 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers, high-resolution timer, DAC and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F334x4/6/8 devices embed a nested vectored interrupt controller (NVIC) able to handle up to 60 interrupt channels, that can be masked and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The external interrupt/event controller consists of 27 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked

3.16 Communication interfaces

3.16.1 Inter-integrated circuit interface (I^2C)

The devices feature an I^2C bus interface which can operate in multimaster and slave mode. It can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes.

It supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). It also includes programmable analog and digital noise filters.

Table 6. Comparison of I^2C analog and digital filters

-	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, it provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. It also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I^2C interface can be served by the DMA controller.

The features available in I2C1 are showed below in *Table 7*.

Table 7. STM32F334x4/6/8 I^2C implementation

I^2C features(1)	I2C1
7-bit addressing mode	X
10-bit addressing mode	X
Standard mode (up to 100 kbit/s)	X
Fast mode (up to 400 kbit/s)	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X
Independent clock	X
SMBus	X
Wakeup from STOP	X

1. X = supported.

4 Pinout and pin descriptions

Figure 4. LQFP32 pinout

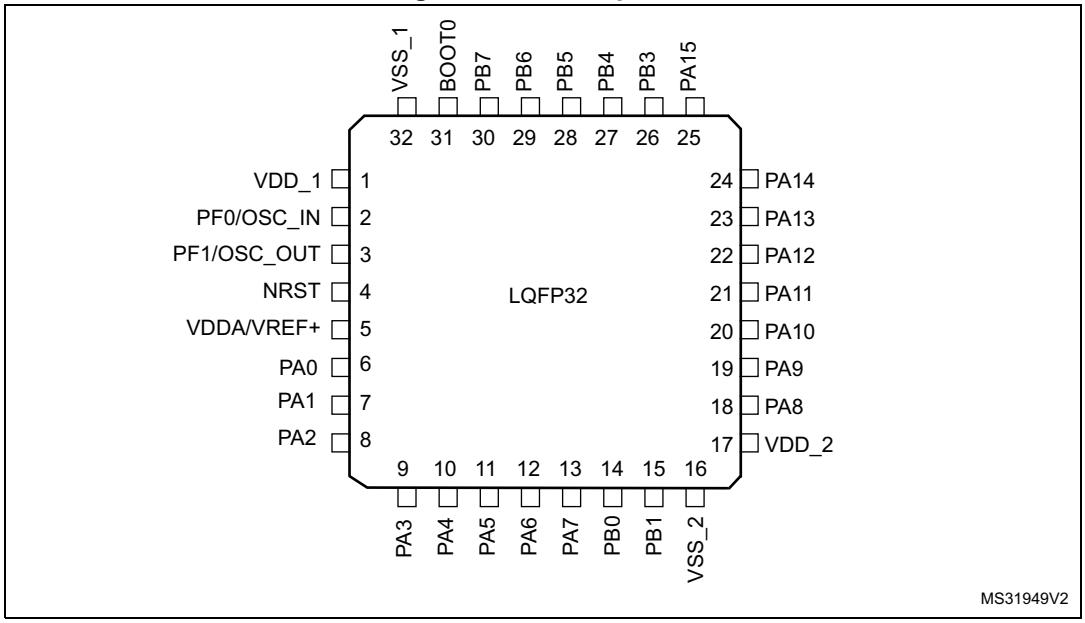


Figure 5. LQFP48 pinout

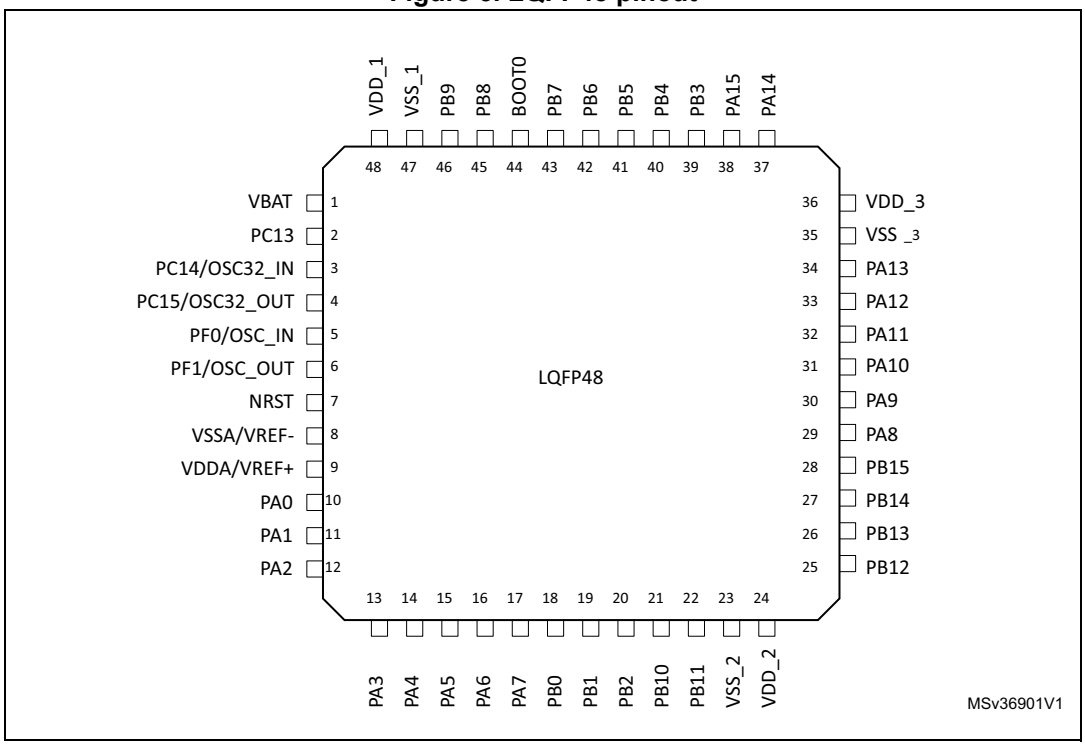


Table 14. Alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/TIM15/ TIM16/TIM17/ EVENT	TIM1/TIM3/ TIM15/ TIM16	HRTIM1/TSC	I2C1/TIM1	SPI1/Infrared	TIM1/Infrared	USART1/USART2/USART3/ GPCOMP6	GPCOMP2/ GPCOMP4/ GPCOMP6	CAN/TIM1/ TIM15	TIM2/TIM3 /TIM17	TIM1	HRTIM1/ TIM1	HRTIM1/ OPAMP2	-	EVENT
Port B	PB10	-	TIM2_CH3	-	TSC_SYNC	-	-	-	USART3_TX	-	-	-	-	-	HRTIM1_FLT3	-	EVENTOUT
	PB11	-	TIM2_CH4	-	TSC_G6_IO1	-	-	-	USART3_RX	-	-	-	-	-	HRTIM1_FLT4	-	EVENTOUT
	PB12	-	-	-	TSC_G6_IO2	-	-	TIM1_BKIN	USART3_CK	-	-	-	-	-	HRTIM1_CHC1	-	EVENTOUT
	PB13	-	-	-	TSC_G6_IO3	-	-	TIM1_CH1N	USART3_CTS	-	-	-	-	-	HRTIM1_CHC2	-	EVENTOUT
	PB14	-	TIM15_CH1	-	TSC_G6_IO4	-	-	TIM1_CH2N	USART3_RTS_DE	-	-	-	-	-	HRTIM1_CHD1	-	EVENTOUT
	PB15	-	TIM15_CH2	TIM15_CH1N	-	TIM1_CH3N	-	-	-	-	-	-	-	-	HRTIM1_CHD2	-	EVENTOUT
Port C	PC0	-	EVENTOUT	TIM1_CH1	-	-	-	-	-	-	-	-	-	-	-	-	-
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC2	-	EVENTOUT	TIM1_CH3	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC3	-	EVENTOUT	TIM1_CH4	-	-	-	TIM1_BKIN2	-	-	-	-	-	-	-	-	-
	PC4	-	EVENTOUT	TIM1_ETR	-	-	-	-	USART1_TX	-	-	-	-	-	-	-	-
	PC5	-	EVENTOUT	TIM15_BKIN	TSC_G3_IO1	-	-	-	USART1_RX	-	-	-	-	-	-	-	-
	PC6	-	EVENTOUT	TIM3_CH1	HRTIM1_EEV10	-	-	-	COMP6_OUT	-	-	-	-	-	-	-	-
	PC7	-	EVENTOUT	TIM3_CH2	HRTIM1_FLT5	-	-	-	-	-	-	-	-	-	-	-	-
	PC8	-	EVENTOUT	TIM3_CH3	HRTIM1_CHE1	-	-	-	-	-	-	-	-	-	-	-	-
	PC9	-	EVENTOUT	TIM3_CH4	HRTIM1_CHE2	-	-	-	-	-	-	-	-	-	-	-	-
	PC10	-	EVENTOUT	-	-	-	-	-	USART3_TX	-	-	-	-	-	-	-	-
	PC11	-	EVENTOUT	-	HRTIM1_EEV2	-	-	-	USART3_RX	-	-	-	-	-	-	-	-
	PC12	-	EVENTOUT	-	HRTIM1_EEV1	-	-	-	USART3_CK	-	-	-	-	-	-	-	-
	PC13	-	-	-	-	TIM1_CH1N	-	-	-	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Port D	PD2	-	EVENTOUT	TIM3_ETR	-	-	-	-	-	-	-	-	-	-	-	-	-
Port F	PF0	-	-	-	-	-	-	TIM1_CH3N	-	-	-	-	-	-	-	-	-
	PF1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 20* are derived from tests performed under the ambient temperature condition summarized in *Table 19*.

Table 20. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Characteristics of the embedded reset and power-control block

The parameters given in *Table 21* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 19*.

Table 21. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{POR/PDR}$(1)	Power on/power down reset threshold	Falling edge	1.8(2)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(3)	POR reset temporization	-	1.5	2.5	4.5	ms

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD}.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Guaranteed by design, not tested in production.

Table 31. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ.		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Sleep mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM	72 MHz	51.8	6.3	mA
			64 MHz	46.4	5.7	
			48 MHz	35.0	4.40	
			32 MHz	23.7	3.13	
			24 MHz	18.0	2.49	
			16 MHz	12.2	1.85	
			8 MHz	6.2	0.99	
			4 MHz	3.68	0.88	
			2 MHz	2.26	0.80	
			1 MHz	1.55	0.76	
			500 kHz	1.20	0.74	
			125 kHz	0.89	0.72	
I_{DDA} (1) (2)	Supply current in Sleep mode from V_{DDA} supply		72 MHz	239.0	236.7	µA
			64 MHz	209.4	207.8	
			48 MHz	154.0	152.9	
			32 MHz	103.7	103.2	
			24 MHz	80.1	79.8	
			16 MHz	56.7	56.6	
			8 MHz	1.14	1.14	
			4 MHz	1.14	1.14	
			2 MHz	1.14	1.14	
			1 MHz	1.14	1.14	
			500 kHz	1.14	1.14	
			125 kHz	1.14	1.14	

1. V_{DDA} supervisor is OFF.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 50: I/O static characteristics*.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 17*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 17*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 47: ESD absolute maximum ratings* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 19*. All I/Os (FT, TTa and TC unless otherwise specified) are CMOS and TTL compliant.

Table 51. Output voltage characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	
V_{OH} (3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH}(3)(4)	Output high level voltage for an I/O pin		V_{DD}–1.3	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	
V_{OH}(3)(4)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OLFM+}(1)(4)	Output low level voltage for an FTf I/O pin in FM+ mode	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 17* and the sum of I_{IO} (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 17* and the sum of I_{IO} (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
4. Data based on design simulation.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 22* and *Table 66*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 19*.

Table 57. HRTIM output response to external events 1 to 10 (Synchronous mode [1])

Symbol	Parameter	Conditions	Min.	Typ.	Max. (2)	Unit
$T_{PROP(HRTIM)}$	External event response latency in HRTIM	HRTIM internal propagation delay [3]	6	-	7	t_{HRTIM}
$t_{LAT(DEEV)}$	Digital external event response latency	Propagation delay from HRTIM1_EEVx digital input to HRTIM_CHxy output pin (30pF load) [4]	-	61	72	ns
$t_{LAT(AEEV)}$	Analog external event response latency	Propagation delay from COMPx_INP input pin to HRTIM_CHxy output pin (30pF load) [4]	-	81	94	ns
$t_{W(FLT)}$	Minimum external event pulse width	-	12.5	-	-	ns
$T_{JIT(EEV)}$	External event response jitter	Jitter of the delay from HRTIM1_EEVx digital input or COMPx_INP to HRTIM_CHxy output pin	-	-	1	t_{HRTIM} (5)
$T_{JIT(PW)}$	Jitter on output pulse width in response to an external event	-	-	-	0	t_{HRTIM} (5)

1. EExFAST bit in HRTIM_EECR1 or HRTIM_EECR2 register is cleared (synchronous mode). External event filtering is disabled, i.e. EExF[3:0]=0000 in HRTIM_EECR2 register. Refer to Latency to external events paragraph in HRTIM section of RM0364.
2. Data based on characterization results, not tested in production.
3. This parameter does not take into account latency introduced by GPIO or comparator. Refer to DEERL or SACRL parameter for complete latency.
4. This parameter is given for f_{HRTIM} = 144 MHz.
5. T_{HRTIM} = 1 / f_{HRTIM} with f_{HRTIM}= 144 MHz or f_{HRTIM} = 128 MHZ depending on the clock controller configuration. (Refer to Reset and clock control section in RM0364.)

Table 58. HRTIM synchronization input / output[1]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{W(SYNCIN)}$	Minimum pulse width on SYNCIN inputs, including HRTIM1_SCIN	-	2	-	-	t_{HRTIM}
$t_{LAT(DF)}$	Response time to external synchronization request	-	-	-	1	t_{HRTIM}
$t_{LAT(AF)}$	Pulse width on HRTIM1_SCOUT output	-	-	16	-	t_{HRTIM}
		f_{HRTIM}=144 MHz	-	111.1	-	ns

1. Guaranteed by design, not tested in production.

6.3.17 Timer characteristics

The parameters given in *Table 59* are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 59. TIMx(1)(2) characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.9	-	ns
		$f_{TIM1CLK}$ = 144 MHz	6.95	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	36	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.0139	910	µs
		$f_{TIM1CLK}$ = 144 MHz	0.0069	455	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.65	s
		$f_{TIM1CLK}$ = 144 MHz	-	29.825	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3,TIM15, TIM16 and TIM17 timers.
2. Guaranteed by design, not tested in production.

Table 60. IWDG min./max. timeout period at 40 kHz (LSI) (1)

Prescaler divider	PR[2:0] bits	Min. timeout (ms) RL[11:0]= 0x000	Max. timeout (ms) RL[11:0]= 0xFFF
/4	0	0.1	409.6
/8	1	0.2	819.2
/16	2	0.4	1638.4
/32	3	0.8	3276.8
/64	4	1.6	6553.6
/128	5	3.2	13107.2
/256	7	6.4	26214.4

1. These timings are given for a 40 kHz clock but the microcontroller's internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 61. WWDG min./max. timeout value at 72 MHz (PCLK)(1)

Prescaler	WDGTB	Min. timeout value	Max. timeout value
1	0	0.05687	3.6409
2	1	0.1137	7.2817
4	2	0.2275	14.564
8	3	0.4551	29.127

1. Guaranteed by design, not tested in production.

6.3.18 Communication interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 Kbit/s
- Fast-mode (Fm): with a bit rate up to 400 Kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I²C peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDD is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.14: I/O port characteristics* for the I²C I/O characteristics.

All I²C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 62. I^2C analog filter characteristics(1)

Symbol	Parameter	Min.	Max.	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter.	50(2)	260(3)	ns

1. Guaranteed by design, not tested in production.
2. Spikes with width below t_{AF}(min.) are filtered.
3. Spikes with width above t_{AF}(max.) are not filtered.

SPI characteristics

Unless otherwise specified, the parameters given in *Table 53* for SPI are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 19: General operating conditions*.

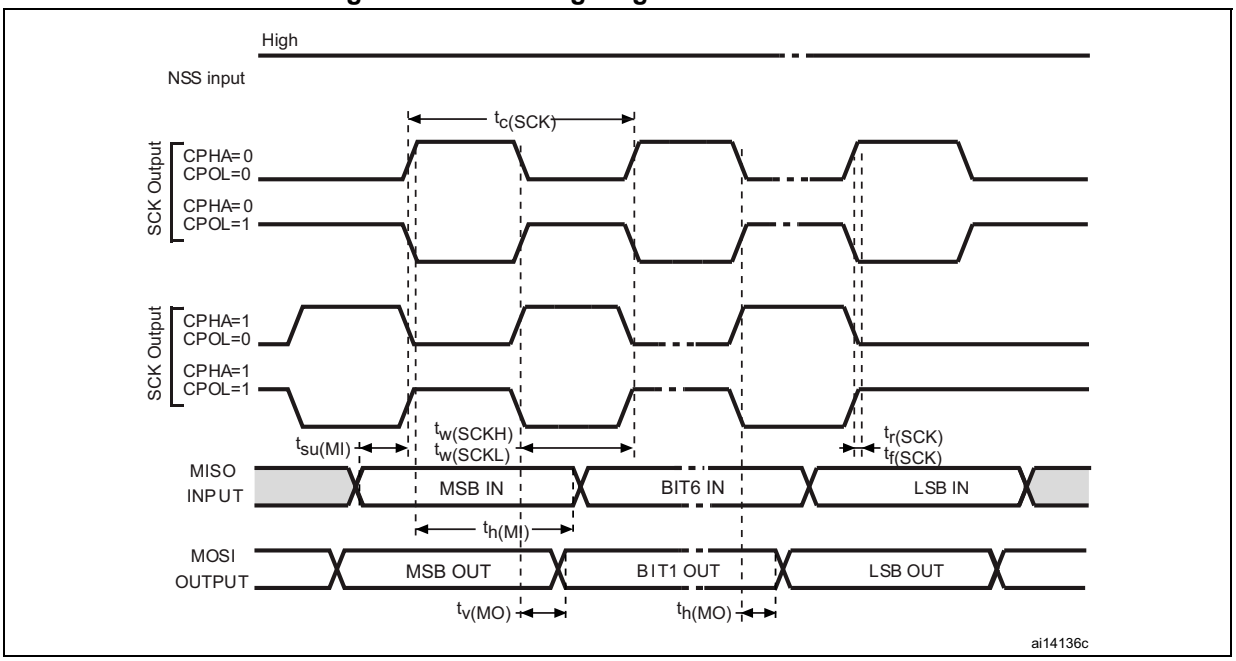
Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 63. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode 2.7<V_{DD}<3.6	-	-	24	MHz
		Master mode 2<V_{DD}<3.6			18	
		Slave mode 2<V_{DD}<3.6			24	
		Slave mode transmitter/full duplex 2<V_{DD}<3.6			18(2)	
DuCy(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	0	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	-	
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	10	-	40	
$t_{dis(SO)}$	Data output disable time	Slave mode	10	-	17	
$t_{v(SO)}$	Data output valid time	Slave mode 2.7<V_{DD}<3.6V	-	12	20	
		Slave mode 2<V_{DD}<3.6V	-	12	27.5	
$t_{v(MO)}$		Master mode	-	1.5	5	
$t_{h(SO)}$	Data output hold time	Slave mode	7.5	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Data based on characterization results, not tested in production.
2. Maximum frequency in Slave transmitter mode is determined by the sum of tv(SO) and tsu(MI) which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having tsu(MI) = 0 while Duty(SCK) = 50%.

Figure 26. SPI timing diagram - master mode(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

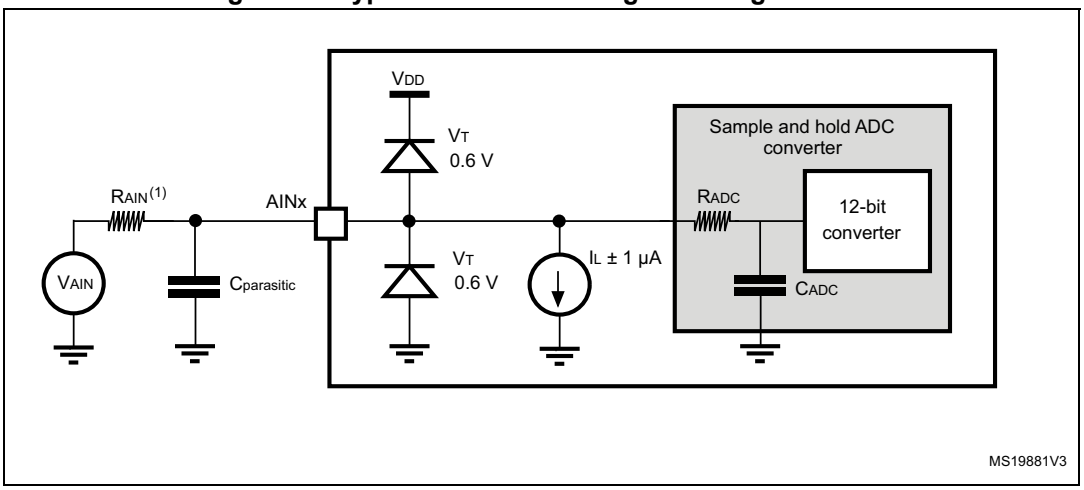
6.3.19 ADC characteristics

Unless otherwise specified, the parameters given in *Table 64* to *Table 67* are guaranteed by design, with conditions summarized in *Table 19*.

Table 64. ADC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage for ADC	-	2	-	3.6	V
I_{DDA}	ADC current consumption (*Figure 27*)	Single ended mode, 5 MSPS,	-	1011.3	1172.0	µA
		Single ended mode, 1 MSPS	-	214.7	322.3	
		Single ended mode, 200 KSPS	-	54.7	81.1	
		Differential mode,5 MSPS,	-	1061.5	1243.6	
		Differential mode, 1 MSPS	-	246.6	337.6	
		Differential mode, 200 KSPS	-	56.4	83.0	

Figure 29. Typical connection diagram using the ADC



1. Refer to *Table 64* for the values of R_{AIN}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 10: Power-supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.20 DAC electrical specifications

Table 69. DAC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage	-	2.4	-	3.6	V
R_{LOAD}(1)	Resistive load	DAC output buffer ON (to V_{SSA})	5	-	-	kΩ
R_{LOAD}(1)	Resistive load	DAC output buffer ON (to V_{DDA})	25	-	-	kΩ
R_O(1)	Output impedance	DAC output buffer OFF	-	-	15	kΩ
C_{LOAD}(1)	Capacitive load	DAC output buffer ON	-	-	50	pF
V_{DAC_OUT}(1)	Voltage on DAC_OUT output	Corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{DDA} = 3.6 V and (0x155) and (0xEAB) at V_{DDA} = 2.4 V	0.2	-	V_{DDA} – 0.2	V
		DAC output buffer OFF	-	0.5	-	mV
			-	-	V_{DDA}– 1LSB	V
I_{DDA}(3)	DAC DC current consumption in quiescent mode(2)	With no load, middle code (0x800) on the input	-	-	380	µA
		With no load, worst code (0xF1C) on the input.	-	-	480	µA

Table 71. Operational amplifier characteristics(1) (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
en	Voltage noise density	@ 1KHz, Output loaded with 4 KΩ	-	109	-	$\frac{nV}{\sqrt{Hz}}$
		@ 10KHz, Output loaded with 4 KΩ	-	43	-	

1. Guaranteed by design, not tested in production.
2. The saturation voltage can also be limited by the I_{load}.
3. R2 is the internal resistance between OPAMP output and OPAMP inverting input.
   R1 is the internal resistance between OPAMP inverting input and ground.
   The PGA gain =1+R2/R1
4. Mostly TTa I/O leakage, when used in analog mode.

Figure 32. OPAMP Voltage Noise versus Frequency

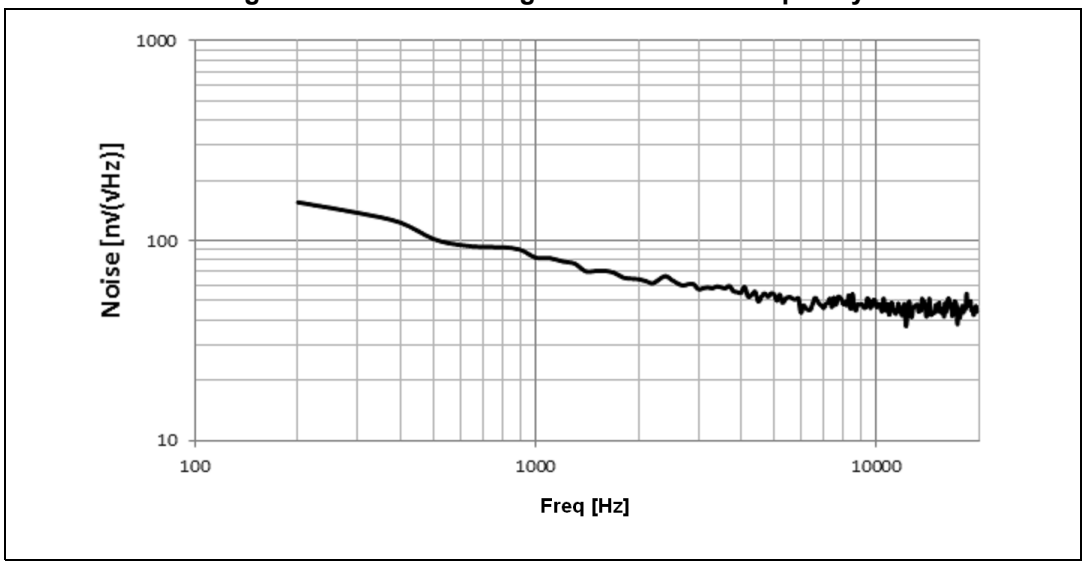
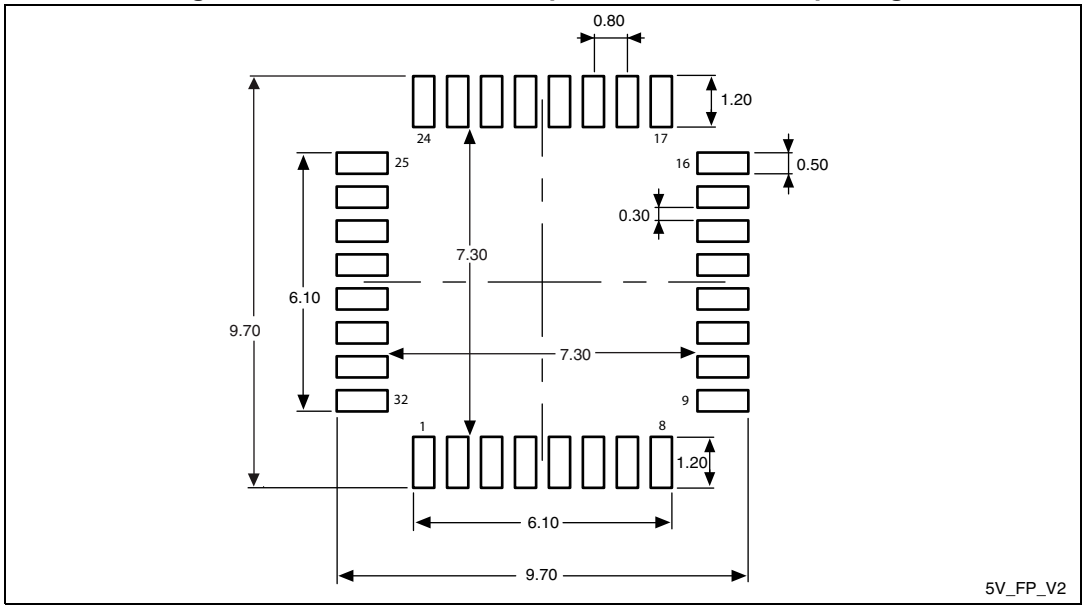


Table 75. LQFP32 mechanical data (continued)

Symbol	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 34. Recommended footprint for the LQFP32 package

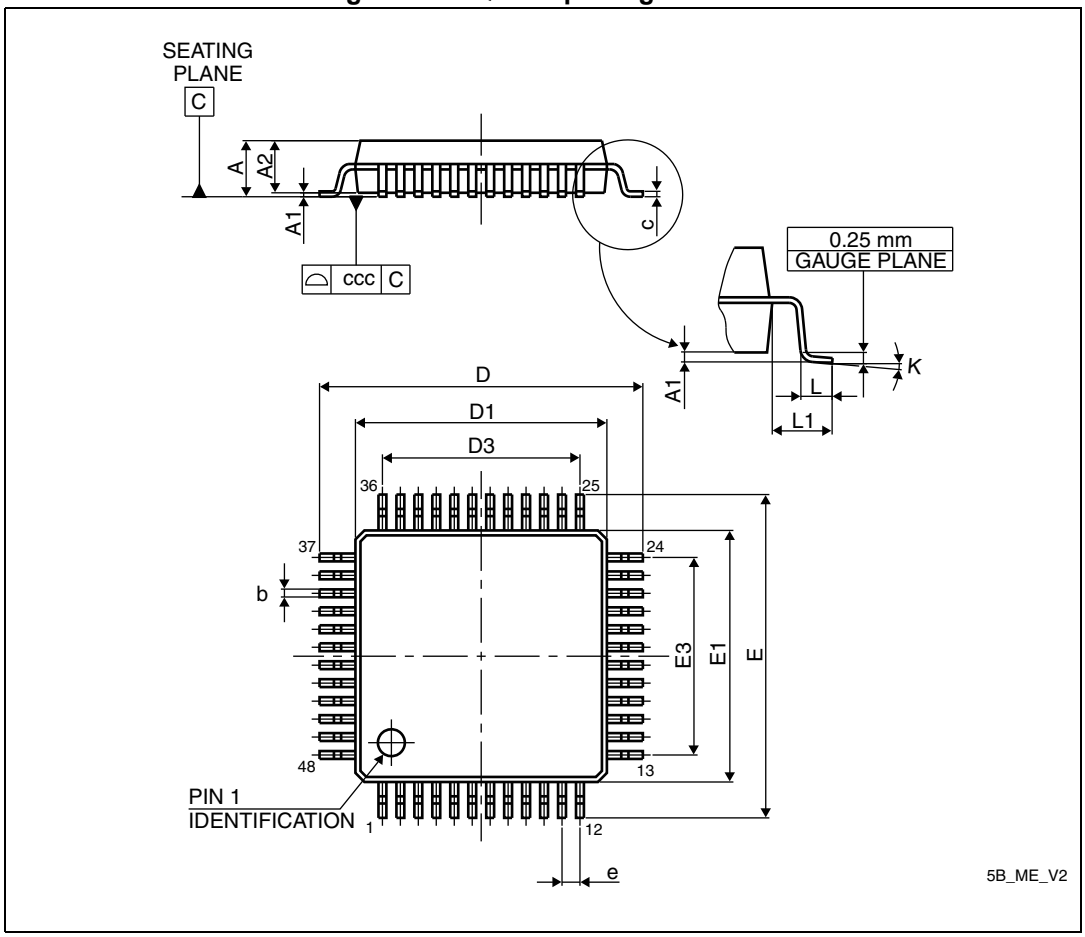


1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

7.3 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7mm low-profile quad flat package.

Figure 36. LQFP48 package outline



1. Drawing is not to scale.

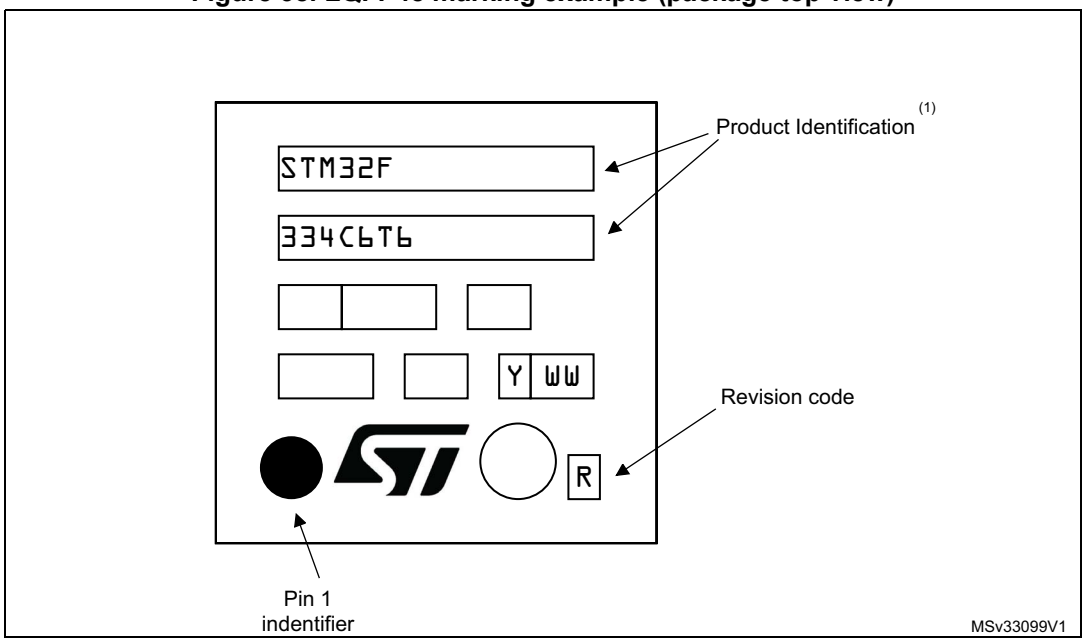
Table 76. LQFP48 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-

Device marking for LQFP48

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 38. LQFP48 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

8 Part numbering

Table 79. Ordering information scheme

Example: STM32 F 334 C 8 T 6 xxx

Device family

STM32 = ARM®-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

334 = STM32F334xx, 2.0 to 3.6 V operating voltage

Pin count

K = 32 pins

C = 48 pins

R = 64 pins

Flash memory size

4 = 16 Kbytes of Flash memory

6 = 32 Kbytes of Flash memory

8 = 64 Kbytes of Flash memory

Package

T = LQFP

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

Options

xxx = programmed parts

TR = tape and reel

9 Revision history

Table 80. Document revision history

Date	Revision	Changes
19-Jun-2014	1	Initial release.
09-Dec-2014	2	Updated: *Table 54: TIMx characteristics* *Table 14: STM32F303x6/8 pin definitions* *Table 59: ADC characteristics* *Table 34: Peripheral current consumption* *Table 40: HSI oscillator characteristics* *Table 17: HSI oscillator accuracy characterization results for soldered parts* *Table 2: STM32F334x4/6/8 family device features and peripheral counts*
2-Feb-2015	3	Updated: *Figure 1: STM32F334x4/6/8 block diagram* *Table 38: HSE oscillator characteristics* *Table 43: Flash memory characteristics* Added *Figure 13: High-speed external clock source AC timing diagram*
09-Jun-2015	4	Udpated : Title *Section 3.14.1: 217 ps high-resolution timer (HRTIM1)* *Section 6.1.6: Power-supply scheme* *Table 19: General operating conditions*
27-Sep-2016	5	Updated: *Section Table 69.: DAC characteristics*, *Section Table 64.: ADC characteristics*,*Table 53: NRST pin characteristics*, *Figure 2: Clock tree*,*Table 13: STM32F334x4/6/8 pin definitions*, *Table 71: Operational amplifier characteristics*, *Figure 20: Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port*, *Table 23: Embedded internal reference voltage*, *Table 39: LSE oscillator characteristics (fLSE = 32.768 kHz)* Added: *Table 35: Wakeup time using USART*