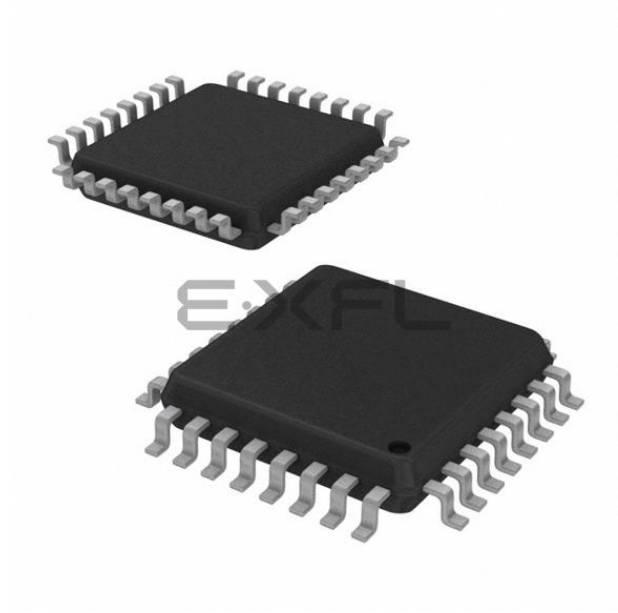

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 9x12b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f334k4t6

2 Description

The STM32F334x4/6/8 family incorporates the high-performance ARM® Cortex®-M4 32-bit RISC core operating at up to 72 MHz frequency embedding a floating point unit (FPU), high-speed embedded memories (up to 64 Kbytes of Flash memory, up to 12 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The STM32F334x4/6/8 microcontrollers offer two fast 12-bit ADCs (5 Msps), up to three ultra-fast comparators, an operational amplifier, three DAC channels, a low-power RTC, one high-resolution timer, one general-purpose 32-bit timer, one timer dedicated to motor control, and four general-purpose 16-bit timers. They also feature standard and advanced communication interfaces: one I^2C, one SPI, up to three USARTs and one CAN.

The STM32F334x4/6/8 family operates in the –40 to +85 °C and –40 to +105 °C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F334x4/6/8 family offers devices in 32, 48 and 64-pin packages.

Depending on the device chosen, different sets of peripherals are included.

Table 2. STM32F334x4/6/8 family device features and peripheral counts

Peripheral		STM32F334Kx			STM32F334Cx			STM32F334Rx		
Flash memory (Kbyte)		16	32	64	16	32	64	16	32	64
SRAM on data bus (Kbyte)		12								
Core coupled memory SRAM on instruction bus (CCM SRAM) (Kbyte)		4								
Timers	High-resolution timer	1 (16-bit / 10 channels)								
	Advanced control	1 (16-bit)								
	General purpose	4 (16-bit) 1 (32 bit)								
	Basic	2 (16-bit)								
	SysTick timer	1								
	Watchdog timers (independent, window)	2								
	PWM channels (all)(1)	20			26			28		
	PWM channels (except complementary)	14			20			22		

3.2.3 Boot modes

At startup, BOOT0 pin and BOOT1 option bit are used to select one of the three boot options:

- Boot from user Flash memory
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART2 (PA2/PA3), I2C1 (PB6/PB7).

3.3 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.4 Power management

3.4.1 Power supply schemes

- V_{SS}, V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. It is provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supply for ADC, DACs, comparators operational amplifiers, reset blocks, RCs and PLL.The minimum voltage to be applied to V_{DDA} differs from one analog peripherals to another. See the *Table 3* below, summarizing the V_{DDA} ranges for analog peripherals. The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be provided first.
- V_{DD18} = 1.65 to 1.95 V (V_{DD18} domain): power supply for digital core, SRAM and Flash memory. V_{DD18} is internally generated through an internal voltage regulator.

Table 3. V_{DDA} ranges for analog peripherals

Analog peripheral	Min V_{DDA}supply	Max V_{DDA}supply
ADC/COMP	2 V	3.6 V
DAC/OPAMP	2.4 V	3.6 V

- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4.2 Power supply supervisor

The device has an integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device

3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

TIM1and HRTIM1 maximum frequency is 144 MHz.

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed, following a specific sequence to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

3.8 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 7 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers, high-resolution timer, DAC and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F334x4/6/8 devices embed a nested vectored interrupt controller (NVIC) able to handle up to 60 interrupt channels, that can be masked and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The external interrupt/event controller consists of 27 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked

3.14.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.15 Real-time clock (RTC) and backup registers

The RTC and the 5 backup registers are supplied through a switch that takes power from either the V_{DD} supply when present or the VBAT pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Two anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.
- 17-bit Auto-reload counter for periodic interrupt with wakeup from STOP/STANDBY capability.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

Table 13. STM32F334x4/6/8 pin definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Pin functions	
LQFP 32	LQFP 48	LQFP 64				Alternate functions	Additional functions
28	41	57	PB5	I/O	FT	TIM16_BKIN, TIM3_CH2, I2C1_SMBA, SPI1_MOSI, USART2_CK, TIM17_CH1, HRTIM1_EEV6, EVENTOUT	-
29	42	58	PB6	I/O	FTf	TIM16_CH1N, TSC_G5_IO3, I2C1_SCL, USART1_TX, HRTIM1_SCIN, HRTIM1_EEV4, EVENTOUT	-
30	43	59	PB7	I/O	FTf	TIM17_CH1N, TSC_G5_IO4, I2C1_SDA, USART1_RX, TIM3_CH4, HRTIM1_EEV3, EVENTOUT	-
31	44	60	BOOT0	I	B	-	-
-	45	61	PB8	I/O	FTf	TIM16_CH1, TSC_SYNC, I2C1_SCL, USART3_RX, CAN_RX, TIM1_BKIN, HRTIM1_EEV8, EVENTOUT	-
-	46	62	PB9	I/O	FTf	TIM17_CH1, I2C1_SDA, IR_OUT, USART3_TX, COMP2_OUT, CAN_TX, HRTIM1_EEV5, EVENTOUT	-
32	47	63	VSS	S	-	-	-
1	48	64	VDD	S	-	-	-

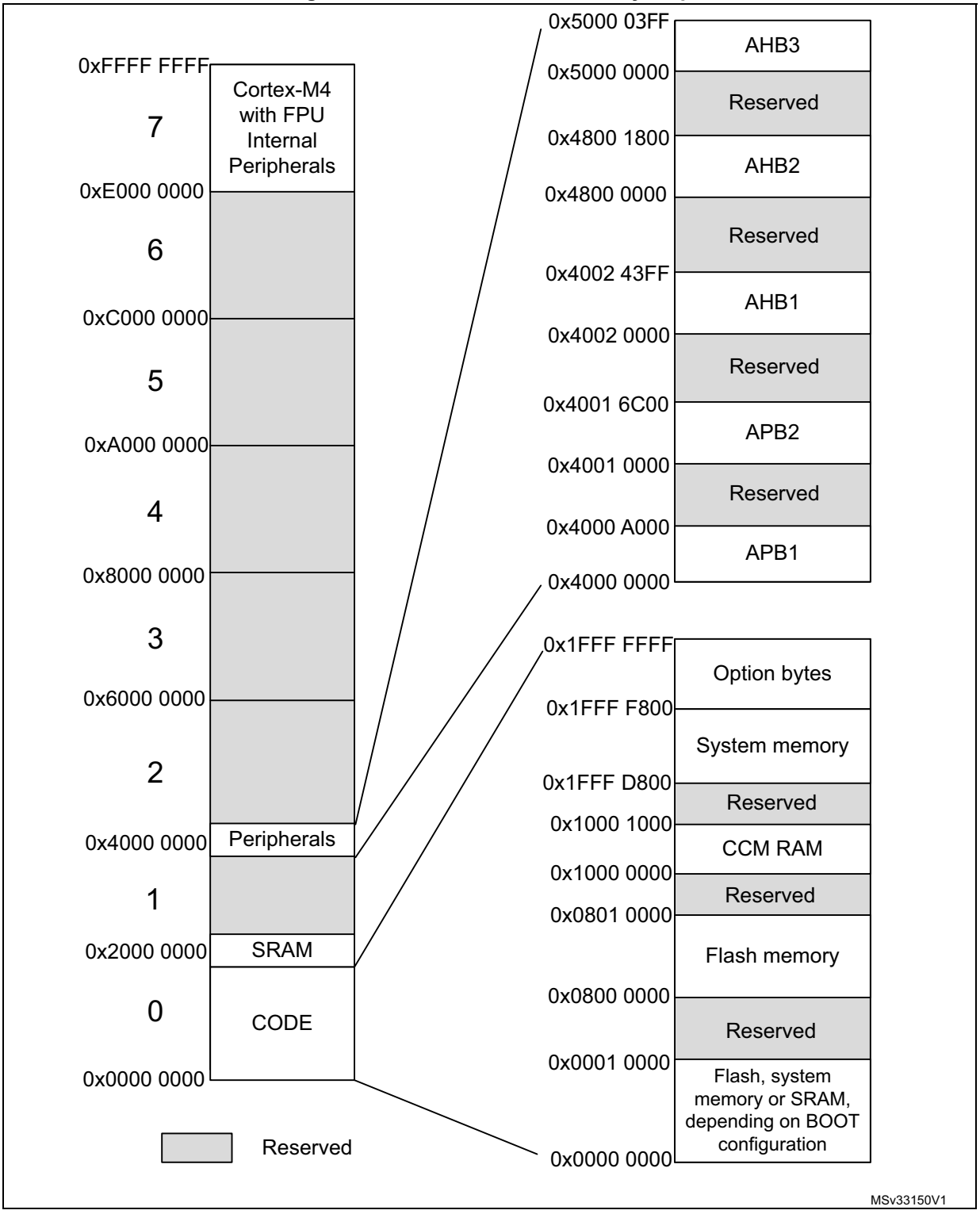
1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch sinks only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
   After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the reference manual.
2. Fast ADC channel.
3. These GPIOs offer a reduced touch sensing sensitivity. It is thus recommended to use them as sampling capacitor I/O.

Table 14. Alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/TIM15/ TIM16/TIM17/ EVENT	TIM1/TIM3/ TIM15/ TIM16	HRTIM1/TSC	I2C1/TIM1	SPI1/Infrared	TIM1/Infrared	USART1/USA RT2/USART3/ GPCOMP6	GPCOMP2/ GPCOMP4/ GPCOMP6	CAN/TIM1/ TIM15	TIM2/TIM3 /TIM17	TIM1	HRTIM1/ TIM1	HRTIM1/ OPAMP2	-	EVENT
Port A	PA0	-	TIM2_CH1/TI M2_ETR	-	TSC_G1_IO1	-	-	-	USART2_CTS	-	-	-	-	-	-	-	EVENTOUT
	PA1	-	TIM2_CH2	-	TSC_G1_IO2	-	-	-	USART2_RTS _DE	-	TIM15_CH1N	-	-	-	-	-	EVENTOUT
	PA2	-	TIM2_CH3	-	TSC_G1_IO3	-	-	-	USART2_TX	COMP2_OUT	TIM15_CH1	-	-	-	-	-	EVENTOUT
	PA3	-	TIM2_CH4	-	TSC_G1_IO4	-	-	-	USART2_RX	-	TIM15_CH2	-	-	-	-	-	EVENTOUT
	PA4	-	-	TIM3_CH2	TSC_G2_IO1	-	SPI1_NSS	-	USART2_CK	-	-	-	-	-	-	-	EVENTOUT
	PA5	-	TIM2_CH1/TI M2_ETR	-	TSC_G2_IO2	-	SPI1_SCK	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA6	-	TIM16_CH1	TIM3_CH1	TSC_G2_IO3	-	SPI1_MISO	TIM1_BKIN	-	-	-	-	-	-	OPAMP2_DIG	-	EVENTOUT
	PA7	-	TIM17_CH1	TIM3_CH2	TSC_G2_IO4	-	SPI1_MOSI	TIM1_CH1N	-	-	-	-	-	-	-	-	EVENTOUT
	PA8	MCO	-	-	-	-	-	TIM1_CH1	USART1_CK	-	-	-	-	-	HRTIM1_CHA1	v	EVENTOUT
	PA9	-	-	-	TSC_G4_IO1	-	-	TIM1_CH2	USART1_TX	-	TIM15_BKIN	TIM2_CH3	-	-	HRTIM1_CHA2	-	EVENTOUT
	PA10	-	TIM17_BKIN	-	TSC_G4_IO2	-	-	TIM1_CH3	USART1_RX	COMP6_OUT	-	TIM2_CH4	-	-	HRTIM1_CHB1	-	EVENTOUT
	PA11	-	-	-	-	-	-	TIM1_CH1N	USART1_CTS	-	CAN_RX	-	TIM1_CH4	TIM1_BKIN2	HRTIM1_CHB2	-	EVENTOUT
	PA12	-	TIM16_CH1	-	-	-	-	TIM1_CH2N	USART1_RTS _DE	COMP2_OUT	CAN_TX	-	TIM1_ETR	-	HRTIM1_FLT1	-	EVENTOUT
	PA13	JTMS/SWDAT	TIM16_CH1N	-	TSC_G4_IO3	-	IR_OUT	-	USART3_CTS	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK/SWCLK	-	-	TSC_G4_IO4	I2C1_SDA	-	TIM1_BKIN	USART2_TX	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM2_CH1/ TIM2_ETR	-	TSC_SYNC	I2C1_SCL	SPI1_NSS	-	USART2_RX	-	TIM1_BKIN	-	-	-	HRTIM1_FLT2	-	EVENTOUT
Port B	PB0	-	-	TIM3_CH3	TSC_G3_IO2	-	-	TIM1_CH2N	-	-	-	-	-	-	-	-	EVENTOUT
	PB1	-	-	TIM3_CH4	TSC_G3_IO3	-	-	TIM1_CH3N	-	COMP4_OUT	-	-	-	-	HRTIM1_SCOUT	-	EVENTOUT
	PB2	-	-	-	TSC_G3_IO4	-	-	-	-	-	-	-	-	-	HRTIM1_SCIN	-	EVENTOUT
	PB3	JTDO/TRACE SWO	TIM2_CH2	-	TSC_G5_IO1	-	SPI1_SCK	-	USART2_TX	-	-	TIM3_ETR	-	HRTIM1_SC OUT	HRTIM1_EEV9	-	EVENTOUT
	PB4	NJTRST	TIM16_CH1	TIM3_CH1	TSC_G5_IO2	-	SPI1_MISO	-	USART2_RX	-	-	TIM17_BK IN	-	-	HRTIM1_EEV7	-	EVENTOUT
	PB5	-	TIM16_BKIN	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI	-	USART2_CK	-	-	TIM17_CH 1	-	-	HRTIM1_EEV6	-	EVENTOUT
	PB6	-	TIM16_CH1N	-	TSC_G5_IO3	I2C1_SCL	-	-	USART1_TX	-	-	-	-	HRTIM1_SCI N	HRTIM1_EEV4	-	EVENTOUT
	PB7	-	TIM17_CH1N	-	TSC_G5_IO4	I2C1_SDA	-	-	USART1_RX	-	-	TIM3_CH4	-	-	HRTIM1_EEV3	-	EVENTOUT
	PB8	-	TIM16_CH1	-	TSC_SYNC	I2C1_SCL	-	-	USART3_RX	-	CAN_RX	-	-	TIM1_BKIN	HRTIM1_EEV8	-	EVENTOUT
	PB9	-	TIM17_CH1	-	-	I2C1_SDA	-	IR_OUT	USART3_TX	COMP2_OUT	CAN_TX	-	-	-	HRTIM1_EEV5	-	EVENTOUT

5 Memory mapping

Figure 7. STM32F334x4/6/8 memory map



6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3 σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V, V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

6.1.5 Input voltage on a pin

The input voltage measurement on a pin of the device is described in *Figure 9*.

Figure 8. Pin loading conditions

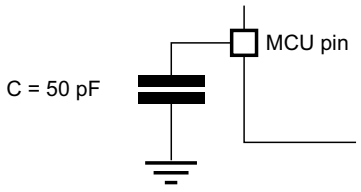


Figure 9. Pin input voltage

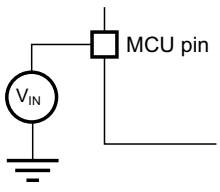


Table 17. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD_x power lines (source)(1)	140	mA
ΣI_{VSS}	Total current out of sum of all VSS_x ground lines (sink)(1)	-140	
I_{VDD}	Maximum current into each V_{DD_x} power line (source)(1)	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	80	
	Total output current sourced by sum of all I/Os and control pins(2)	-80	
$I_{INJ(PIN)}$	Injected current on TT, FT, FTf and B pins(3)	-5 /+0	
	Injected current on TC and RST pin(4)	±5	
	Injected current on TTa pins(5)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS} and V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins.The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 16: Voltage characteristics* for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. I_{INJ}(PIN) must never be exceeded. Refer also to *Table 16: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note 2. below *Table 64*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 18. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

Table 28. Typical and maximum V_{DDA} consumption in Stop and Standby modes

Symbol	Parameter	Conditions		Typ. @V_{DD} (V_{DD} = V_{DDA})						Max.(1)			Unit
				2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DDA}	Supply current in Stop mode	V_{DDA} supervisor ON	Regulator in run/low-power mode, all oscillators OFF	1.67	1.79	1.91	2.04	2.19	2.35	2.5	5.9	6.2	µA
	Supply current in Standby mode		LSI ON and IWDG ON	2.06	2.24	2.41	2.60	2.80	3.04	-	-	-	
			LSI OFF and IWDG OFF	1.54	1.68	1.78	1.92	2.06	2.22	2.6	3.0	3.8	
	Supply current in Stop mode	V_{DDA} supervisor OFF	Regulator in run/low-power mode, all oscillators OFF	0.97	0.99	1.03	1.07	1.14	1.22	-	-	-	
	Supply current in Standby mode		LSI ON and IWDG ON	1.36	1.44	1.52	1.62	1.76	1.91	-	-	-	
			LSI OFF and IWDG OFF	0.86	0.88	0.91	0.95	1.03	1.09	-	-	-	

1. Data based on characterization results, not tested in production.

Table 29. Typical and maximum current consumption from V_{BAT} supply

Symbol	Parameter	Conditions(1)	Typ.@V_{BAT}								Max. @V_{BAT}= 3.6V(2)			Unit
			1.65 V	1.8V	2V	2.4V	2.7V	3V	3.3V	3.6V	T_A= 25°C	T_A= 85°C	T_A= 105°C	
I_{DD_VBAT}	Backup domain supply current	LSE & RTC ON; “Xtal mode” lower driving capability; LSEDRV[1:0] = '00'	0.42	0.44	0.47	0.54	0.60	0.66	0.74	0.82	-	-	-	µA
		LSE & RTC ON; “Xtal mode” higher driving capability; LSEDRV[1:0] = '11'	0.71	0.74	0.77	0.85	0.91	0.98	1.06	1.16	-	-	-	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values.
2. Data based on characterization results, not tested in production.

Table 31. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ.		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Sleep mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM	72 MHz	51.8	6.3	mA
			64 MHz	46.4	5.7	
			48 MHz	35.0	4.40	
			32 MHz	23.7	3.13	
			24 MHz	18.0	2.49	
			16 MHz	12.2	1.85	
			8 MHz	6.2	0.99	
			4 MHz	3.68	0.88	
			2 MHz	2.26	0.80	
			1 MHz	1.55	0.76	
			500 kHz	1.20	0.74	
			125 kHz	0.89	0.72	
I_{DDA} (1) (2)	Supply current in Sleep mode from V_{DDA} supply		72 MHz	239.0	236.7	µA
			64 MHz	209.4	207.8	
			48 MHz	154.0	152.9	
			32 MHz	103.7	103.2	
			24 MHz	80.1	79.8	
			16 MHz	56.7	56.6	
			8 MHz	1.14	1.14	
			4 MHz	1.14	1.14	
			2 MHz	1.14	1.14	
			1 MHz	1.14	1.14	
			500 kHz	1.14	1.14	
			125 kHz	1.14	1.14	

1. V_{DDA} supervisor is OFF.
2. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 50: I/O static characteristics*.

Table 33. Peripheral current consumption (continued)

Peripheral	Typical consumption(1)	Unit
	I_{DD}	
I2C1	13.3	-
CAN	31.3	-
PWR	4.7	-
DAC	15.4	-
DAC2	8.6	-
SPI1	8.2	-

1. The power consumption of the analog part (I_{DDA}) of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.
2. BusMatrix is automatically active when at least one master is ON (CPU or DMA1).
3. The APBx bridge is automatically active when at least one peripheral is ON on the same bus.

Table 45. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP64, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP64, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note *"Software techniques for improving microcontrollers EMC performance"* AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 46. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A =25 °C, LQFP64 package compliant with IEC 61967-2	0.1 to 30 MHz	5	dBµV
			30 to 130 MHz	9	
			130 MHz to 1GHz	31	
			SAE EMI Level	4	-

Figure 19. TC and TTa I/O input characteristics - TTL port

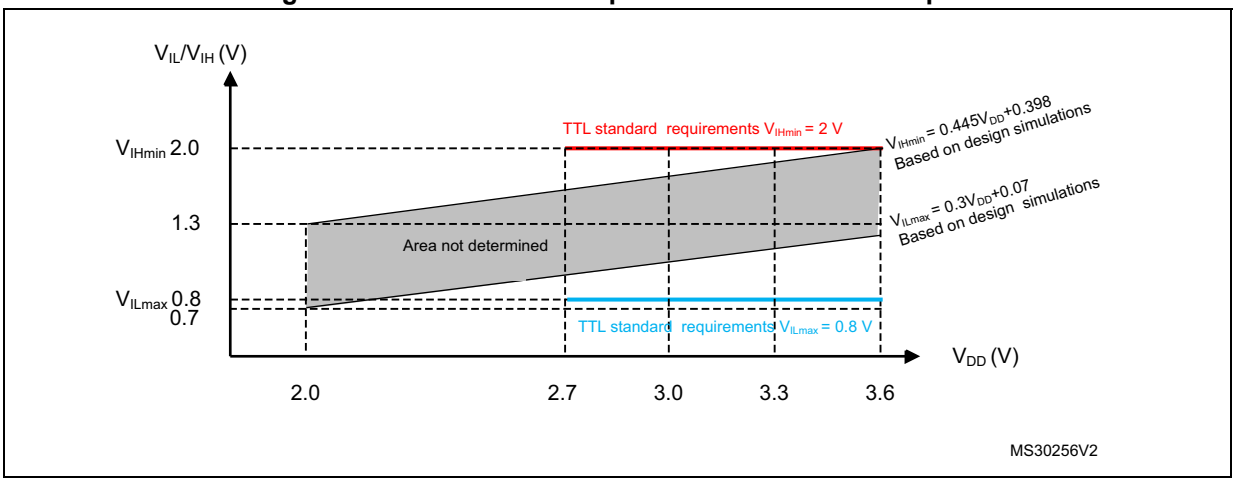


Figure 20. Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port

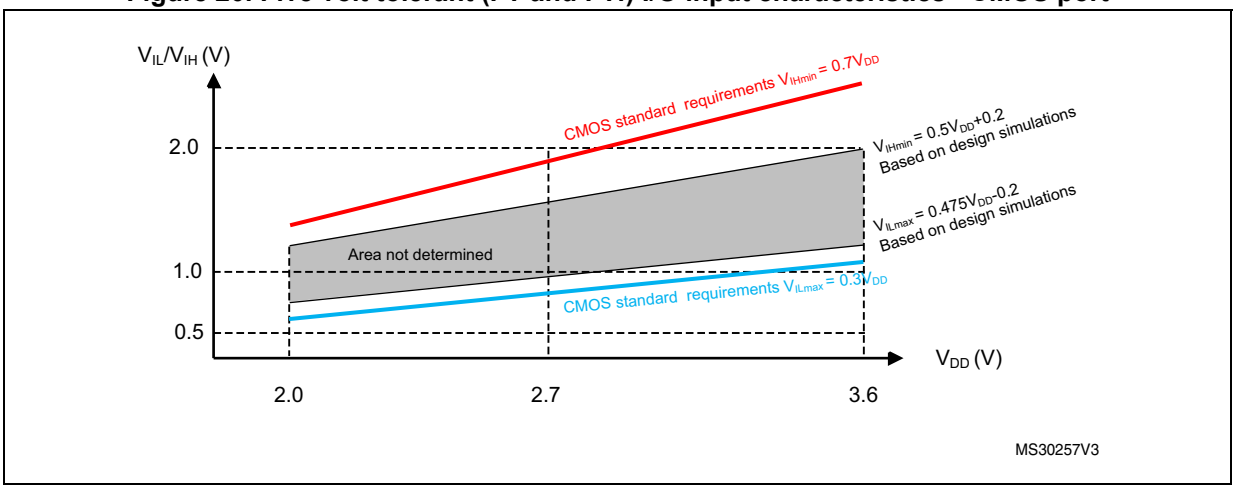
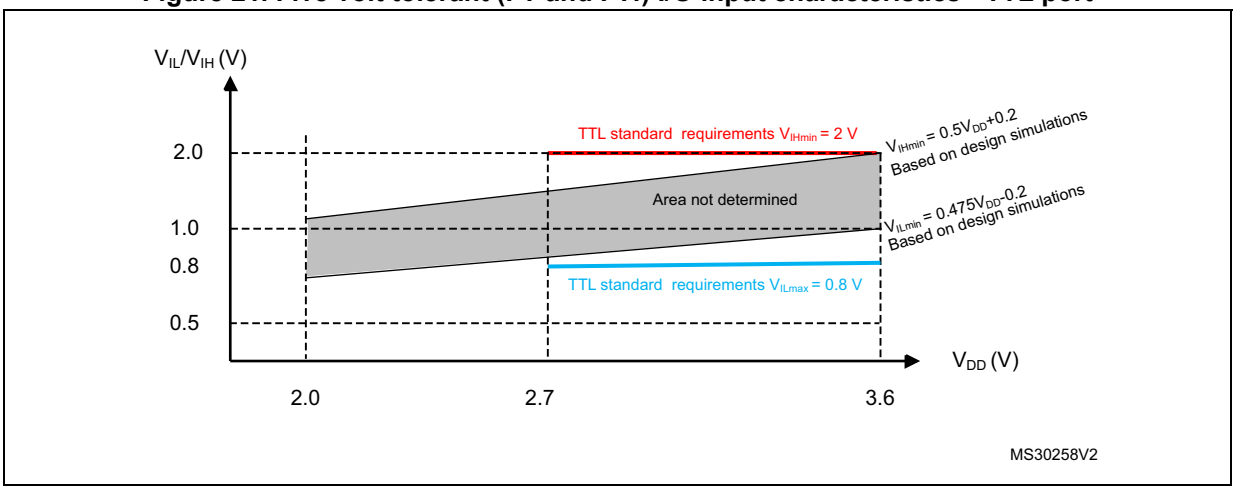


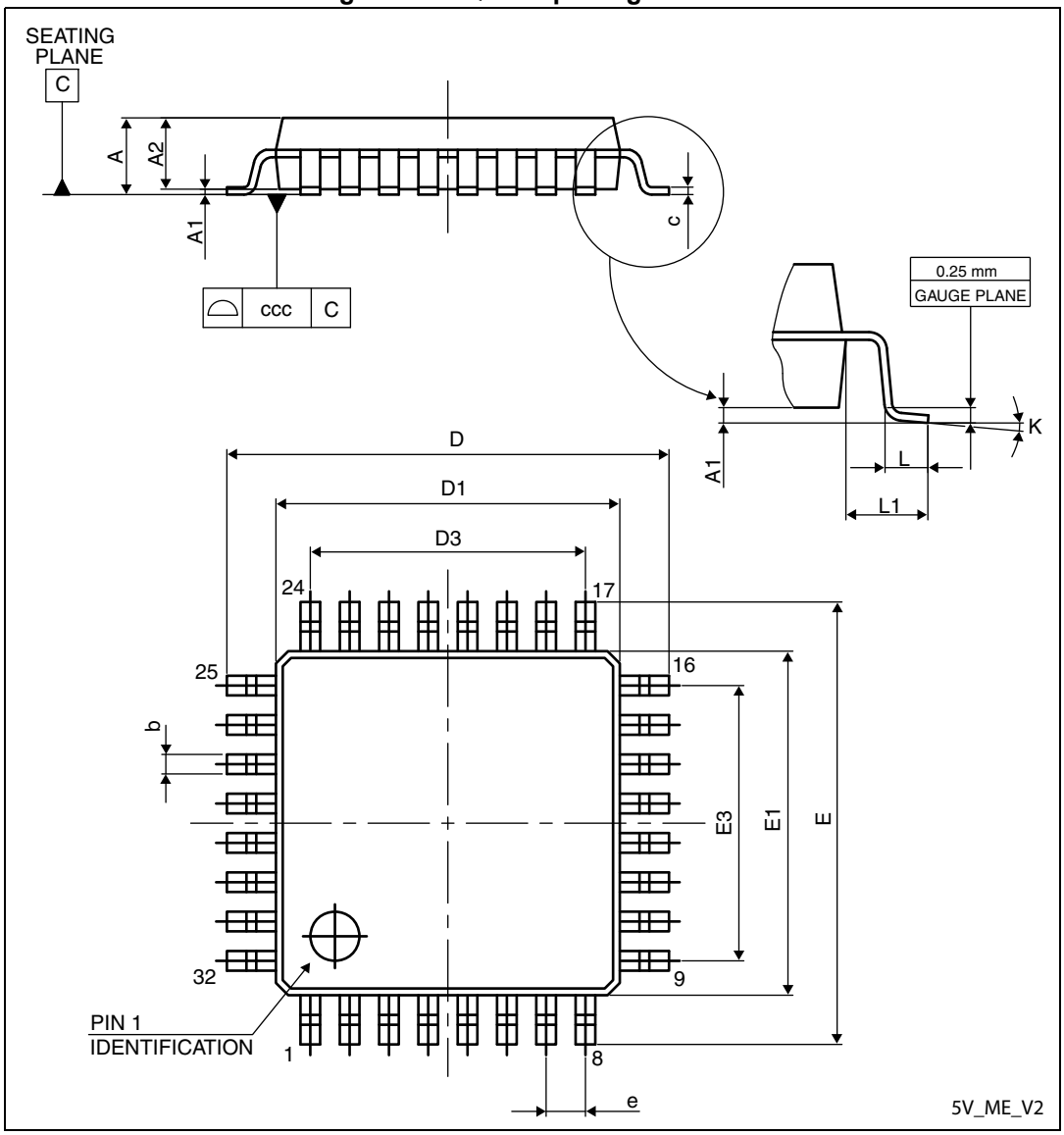
Figure 21. Five volt tolerant (FT and FTf) I/O input characteristics - TTL port



7.2 LQFP32 package information

LQFP32 is a 32-pin, 7 x 7mm low-profile quad flat package.

Figure 33. LQFP32 package outline



1. Drawing is not to scale.

Table 75. LQFP32 mechanical data

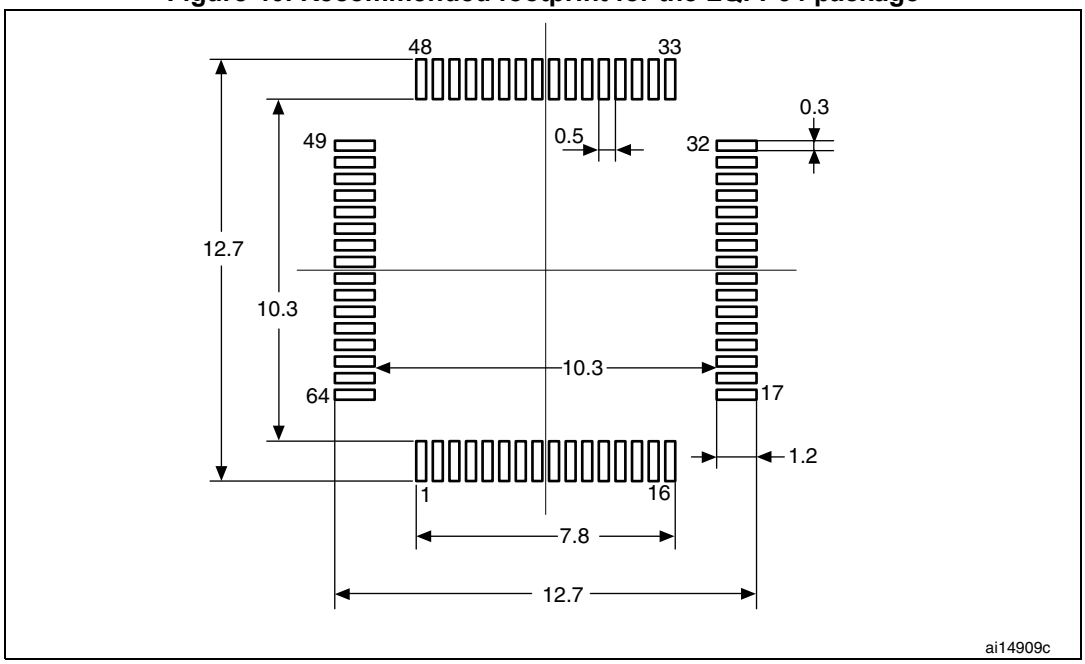
Symbol	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571

Table 77. LQFP64 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
N	Number of pins					
	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 40. Recommended footprint for the LQFP64 package



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Example: high-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output mode at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V = 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW

P_{Dmax} = 175 + 272 = 447 mW

Thus: P_{Dmax} = 447 mW

Using the values obtained in *Table 78* T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

T_{Jmax} = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.1 °C = 102.1 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Table 79: Ordering information scheme*).

8 Part numbering

Table 79. Ordering information scheme

Example: STM32 F 334 C 8 T 6 xxx

Device family

STM32 = ARM®-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

334 = STM32F334xx, 2.0 to 3.6 V operating voltage

Pin count

K = 32 pins

C = 48 pins

R = 64 pins

Flash memory size

4 = 16 Kbytes of Flash memory

6 = 32 Kbytes of Flash memory

8 = 64 Kbytes of Flash memory

Package

T = LQFP

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

Options

xxx = programmed parts

TR = tape and reel