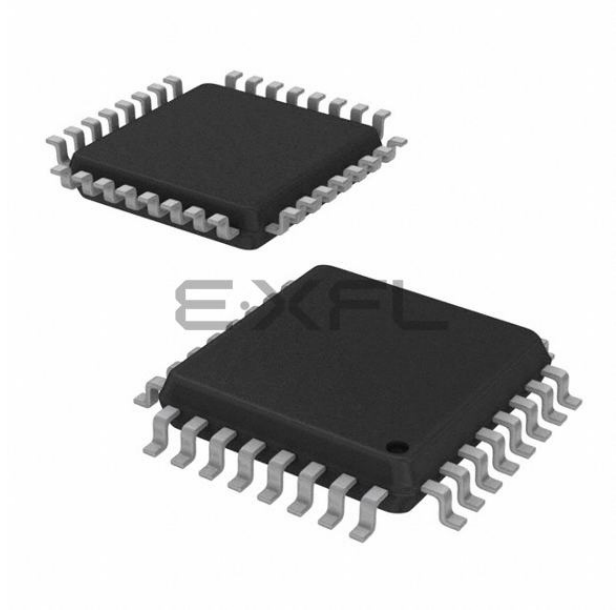

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 9x12b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f334k6t6

List of tables

Table 2. STM32F334x4/6/8 family device features and peripheral counts (continued)

Peripheral		STM32F334Kx	STM32F334Cx	STM32F334Rx
Comm. interfaces	SPI	1		
	I^2C	1		
	USART	2	3	
	CAN	1		
GPIOs	Normal I/Os (TC, TTa)	10	20	26
	5-Volt tolerant I/Os (FT,FTf)	15	17	25
Capacitive sensing channels		14	17	18
DMA channels		7		
12-bit ADCs Number of channels		2 10	2 15	2 21
12-bit DAC channels		3		
Ultra-fast analog comparator		2	3	
Operational amplifiers		1		
CPU frequency		72 MHz		
Operating voltage		2.0 to 3.6 V		
Operating temperature		Ambient operating temperature: - 40 to 85 °C / - 40 to 105 °C Junction temperature: - 40 to 125 °C		
Packages		LQFP32	LQFP48	LQFP64

1. This total considers also the PWMs generated on the complementary output channels.

3 Functional overview

3.1 ARM® Cortex®-M4 core with FPU with embedded Flash and SRAM

The ARM Cortex-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM 32-bit Cortex-M4 RISC processor with FPU features exceptional code-efficiency, delivering the high performance expected from an ARM core, with memory sizes usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allows efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32F334x4/6/8 family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32F334x4/6/8 family devices.

3.2 Memories

3.2.1 Embedded Flash memory

All STM32F334x4/6/8 devices feature up to 64 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

3.2.2 Embedded SRAM

The STM32F334x4/6/8 devices feature up to 12 Kbytes of embedded SRAM with hardware parity check. The memory can be accessed in read/write at CPU clock speed with 0 wait states, allowing the CPU to achieve 90 Dhrystone Mips at 72 MHz when running code from CCM (core coupled memory) RAM.

The SRAM is organized as follows:

- 4 Kbytes of SRAM on instruction and data bus with parity check (core coupled memory or CCM) and used to execute critical routines or to access data
- 12 Kbytes of SRAM with parity check mapped on the data bus.

remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.4.3 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR), and power-down.

- The MR mode is used in the nominal regulation mode (Run)
- The LPR mode is used in Stop mode.
- The power-down mode is used in Standby mode: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The voltage regulator is always enabled after reset. It is disabled in Standby mode.

3.4.4 Low-power modes

The STM32F334x4/6/8 supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm, COMPx, I2C or USARTx.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.14.1 217 ps high-resolution timer (HRTIM1)

The high-resolution timer (HRTIM1) allows generating digital signals with high-accuracy timings, such as PWM or phase-shifted pulses.

It consists of 6 timers, 1 master and 5 slaves, totaling 10 high-resolution outputs, which can be coupled by pairs for deadtime insertion. It also features 5 fault inputs for protection purposes and 10 inputs to handle external events such as current limitation, zero voltage or zero current switching.

HRTIM1 timer is made of a digital kernel clocked at 144 MHz followed by delay lines. Delay lines with closed loop control guarantee a 217 ps resolution whatever the voltage, temperature or chip-to-chip manufacturing process deviation. The high-resolution is available on the 10 outputs in all operating modes: variable duty cycle, variable frequency, and constant ON time.

The slave timers can be combined to control multiswitch complex converters or operate independently to manage multiple independent converters.

The waveforms are defined by a combination of user-defined timings and external events such as analog or digital feedbacks signals.

HRTIM1 timer includes options for blanking and filtering out spurious events or faults. It also offers specific modes and features to offload the CPU: DMA requests, burst mode controller, push-pull and resonant mode.

It supports many topologies including LLC, Full bridge phase shifted, buck or boost converters, either in voltage or current mode, as well as lighting application (fluorescent or LED). It can also be used as a general purpose timer, for instance to achieve high-resolution PWM-emulated DAC.

In debug mode, the HRTIM1 counters can be frozen and the PWM outputs enter safe state.

3.14.2 Advanced timer (TIM1)

The advanced-control timer can be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timers (described in *Section 3.14.3* using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

Table 9. STM32F334x4/6/8 SPI implementation (continued)

SPI features(1)	SPI1
NSS pulse mode	X
TI mode	X

1. X = supported.

3.16.4 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

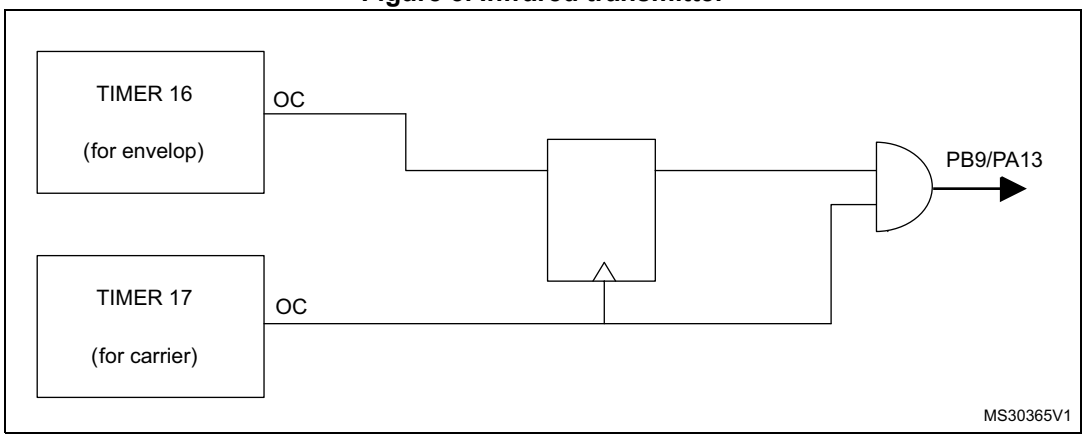
3.17 Infrared transmitter

The STM32F334x4/6/8 devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

Figure 3. Infrared transmitter



3.18 Touch sensing controller (TSC)

The STM32F334x4/6/8 devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 18 capacitive sensing channels distributed over 6 analog I/Os group.

Capacitive sensing technology is able to detect the presence of a finger near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of

Table 13. STM32F334x4/6/8 pin definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Pin functions	
LQFP 32	LQFP 48	LQFP 64				Alternate functions	Additional functions
-	27	35	PB14	I/O	TTa	TIM15_CH1, TSC_G6_IO4, TIM1_CH2N, USART3_RTS_DE, HRTIM1_CHD1, EVENTOUT	ADC2_IN14, OPAMP2_VINP
-	28	36	PB15	I/O	TTa	TIM15_CH2, TIM15_CH1N, TIM1_CH3N, HRTIM1_CHD2, EVENTOUT	ADC2_IN15, COMP6_INM, RTC_REFIN
-	-	37	PC6	I/O	FT	EVENTOUT, TIM3_CH1, HRTIM1_EEV10, COMP6_OUT	-
-	-	38	PC7	I/O	FT	EVENTOUT, TIM3_CH2, HRTIM1_FLT5	-
-	-	39	PC8	I/O	FT	EVENTOUT, TIM3_CH3, HRTIM1_CHE1	-
-	-	40	PC9	I/O	FT	EVENTOUT, TIM3_CH4, HRTIM1_CHE2	-
18	29	41	PA8	I/O	FT	MCO, TIM1_CH1, USART1_CK, HRTIM1_CHA1, EVENTOUT	-
19	30	42	PA9	I/O	FT	TSC_G4_IO1, TIM1_CH2, USART1_TX, TIM15_BKIN, TIM2_CH3, HRTIM1_CHA2, EVENTOUT	-
20	31	43	PA10	I/O	FT	TIM17_BKIN, TSC_G4_IO2, TIM1_CH3, USART1_RX, COMP6_OUT, TIM2_CH4, HRTIM1_CHB1, EVENTOUT	-
21	32	44	PA11	I/O	FT	TIM1_CH1N, USART1_CTS, CAN_RX, TIM1_CH4, TIM1_BKIN2, HRTIM1_CHB2, EVENTOUT	-
22	33	45	PA12	I/O	FT	TIM16_CH1, TIM1_CH2N, USART1_RTS_DE, COMP2_OUT, CAN_TX, TIM1_ETR, HRTIM1_FLT1, EVENTOUT	-

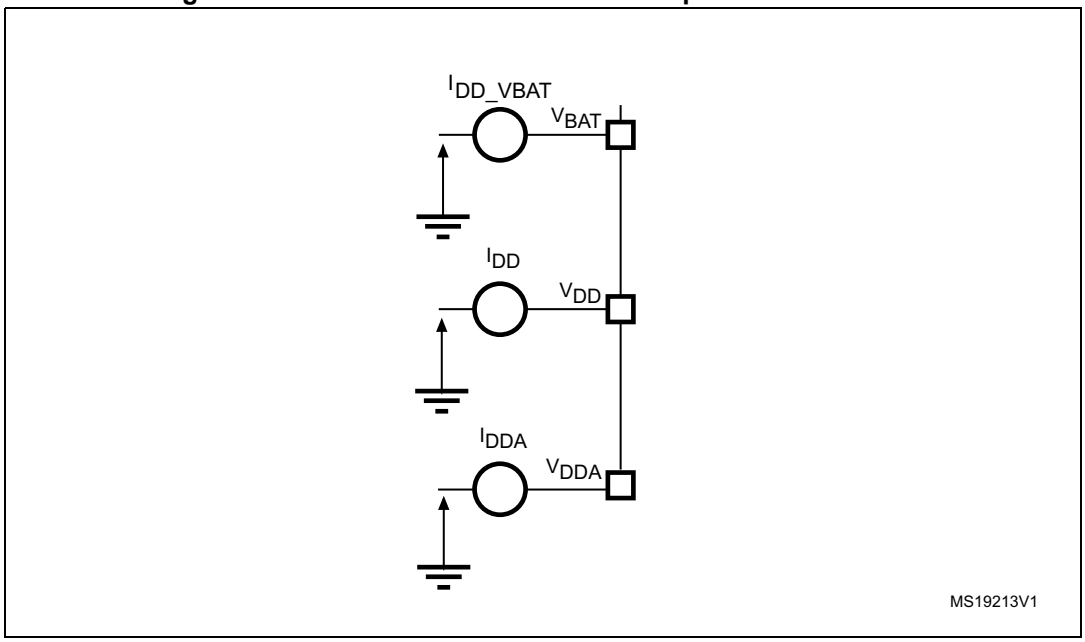
Table 13. STM32F334x4/6/8 pin definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Pin functions	
LQFP 32	LQFP 48	LQFP 64				Alternate functions	Additional functions
28	41	57	PB5	I/O	FT	TIM16_BKIN, TIM3_CH2, I2C1_SMBA, SPI1_MOSI, USART2_CK, TIM17_CH1, HRTIM1_EEV6, EVENTOUT	-
29	42	58	PB6	I/O	FTf	TIM16_CH1N, TSC_G5_IO3, I2C1_SCL, USART1_TX, HRTIM1_SCIN, HRTIM1_EEV4, EVENTOUT	-
30	43	59	PB7	I/O	FTf	TIM17_CH1N, TSC_G5_IO4, I2C1_SDA, USART1_RX, TIM3_CH4, HRTIM1_EEV3, EVENTOUT	-
31	44	60	BOOT0	I	B	-	-
-	45	61	PB8	I/O	FTf	TIM16_CH1, TSC_SYNC, I2C1_SCL, USART3_RX, CAN_RX, TIM1_BKIN, HRTIM1_EEV8, EVENTOUT	-
-	46	62	PB9	I/O	FTf	TIM17_CH1, I2C1_SDA, IR_OUT, USART3_TX, COMP2_OUT, CAN_TX, HRTIM1_EEV5, EVENTOUT	-
32	47	63	VSS	S	-	-	-
1	48	64	VDD	S	-	-	-

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch sinks only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
   After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the reference manual.
2. Fast ADC channel.
3. These GPIOs offer a reduced touch sensing sensitivity. It is thus recommended to use them as sampling capacitor I/O.

6.1.7 Measurement of the current consumption

Figure 11. Scheme of the current-consumption measurement



6.3 Operating conditions

6.3.1 General operating conditions

Table 19. General operating conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	
f_{PCLK2}	Internal APB2 clock frequency	-	0	72	
V_{DD}	Standard operating voltage	-	2	3.6	V
V_{DD18}	Core, SRAM and Flash memory power supply	-	1.65	1.95	
V_{DDA}	Analog operating voltage (OPAMP and DAC not used)	Must have a potential equal to or higher than V_{DD}	2	3.6	
	Analog operating voltage (OPAMP and DAC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.65	3.6	V
V_{IN}	I/O input voltage	TC I/O	–0.3	V_{DD}+0.3	V
		TT I/O	-0.3	3.6	
		TTa I/O	–0.3	V_{DDA}+0.3	
		FT and FTf I/O(1)	–0.3	5.5	
		BOOT0	0	5.5	
PD	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(2)	LQFP64	-	444	mW
PD	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(2)	LQFP48	-	364	mW
PD	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7	LQFP32	-	333	mW
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(3)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low power dissipation(3)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. To sustain a voltage higher than V_{DD}+0.3 V, the internal pull-up/pull-down resistors must be disabled.
2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Section Table 78.: Package thermal characteristics*).
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.5: Thermal characteristics*).

Table 26. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ.	Max. @ T_A(2)			Typ.	Max. @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run/Sleep mode, code executing from Flash or RAM	HSE bypass	72 MHz	224	252(3)	265	269(3)	245	272(3)	288	295(3)	µA
			64 MHz	196	225	237	241	214	243	257	263	
			48 MHz	147	174	183	186	159	186	196	201	
			32 MHz	100	126	133	135	109	133	142	145	
			24 MHz	79	102	107	108	85	108	113	116	
			8 MHz	3	5	5	6	4	6	6	7	
			1 MHz	3	5	5	6	3	5	6	6	
		HSI clock	64 MHz	259	288	304	309	285	315	332	338	
			48 MHz	208	239	251	254	230	258	271	277	
			32 MHz	162	190	198	202	179	206	216	219	
			24 MHz	140	168	175	178	155	181	188	191	
			8 MHz	62	85	88	89	71	94	96	98	

1. Current consumption from the V_{DDA} supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production.
3. Data based characterization results and tested in production with code executing from RAM.

Table 27. Typical and maximum V_{DD} consumption in Stop and Standby modes

Symbol	Parameter	Conditions	Typ. @V_{DD} (V_{DD}=V_{DDA})						Max.(1)			Unit
			2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF	17.51	17.68	17.84	18.17	18.57	19.39	30.6	232.5	612.2	µA
		Regulator in low-power mode, all oscillators OFF	6.44	6.51	6.60	6.73	6.96	7.20	20.0	246.4	585.0	
	Supply current in Standby mode	LSI ON and IWDG ON	0.73	0.89	1.02	1.14	1.28	1.44	-	-	-	
		LSI OFF and IWDG OFF	0.55	0.66	0.75	0.85	0.93	1.01	4.9	7.0	7.9	

1. Data based on characterization results, not tested in production unless otherwise specified.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 33: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT+CS}$

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input configuration
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption:
  - With all peripherals clocked off
  - With only one peripheral clocked on
- Ambient operating temperature at 25°C and $V_{DD} = V_{DDA} = 3.3$ V

Table 33. Peripheral current consumption

Peripheral	Typical consumption(1)	Unit
	I_{DD}	
BusMatrix (2)	11.1	µA/MHz
DMA1	8.0	-
CRC	2.1	-
GPIOA	8.7	-
GPIOB	8.4	-
GPIOC	8.4	-
GPIOD	2.6	-
GPIOF	1.7	-
TSC	4.7	-
ADC1&2	17.4	-
APB2-Bridge (3)	3.3	-
SYSCFG	4.2	-
TIM1	32.3	-
USART1	20.3	-
TIM15	13.8	-
TIM16	9.7	-
TIM17	10.3	-
HRTIM	324.2	-
APB1-Bridge (3)	5.3	-
TIM2	43.4	-
TIM3	34.0	-
TIM6	9.7	-
TIM7	10.3	-
WWDG	6.9	-
USART2	18.8	-
USART3	19.1	-

Table 33. Peripheral current consumption (continued)

Peripheral	Typical consumption(1)	Unit
	I_{DD}	
I2C1	13.3	-
CAN	31.3	-
PWR	4.7	-
DAC	15.4	-
DAC2	8.6	-
SPI1	8.2	-

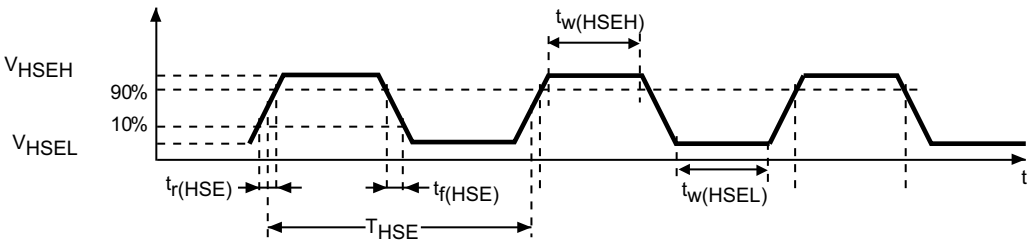
1. The power consumption of the analog part (I_{DDA}) of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.
2. BusMatrix is automatically active when at least one master is ON (CPU or DMA1).
3. The APBx bridge is automatically active when at least one peripheral is ON on the same bus.

Table 36. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSE_ext}	User external clock source frequency(1)	-	1	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time(1)		15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	

1. Guaranteed by design, not tested in production.

Figure 13. High-speed external clock source AC timing diagram



MS19214V2

Low-speed external user clock generated from an external source

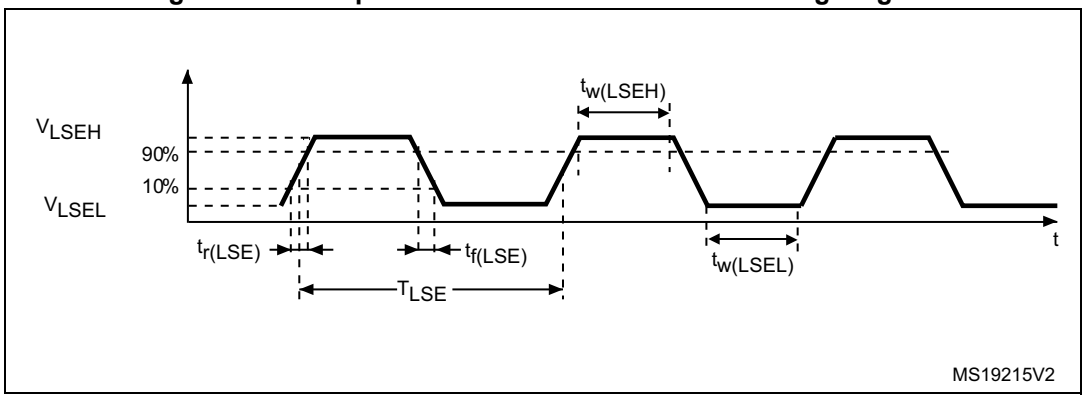
In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 14*

Table 37. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	

1. Guaranteed by design, not tested in production.

Figure 14. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

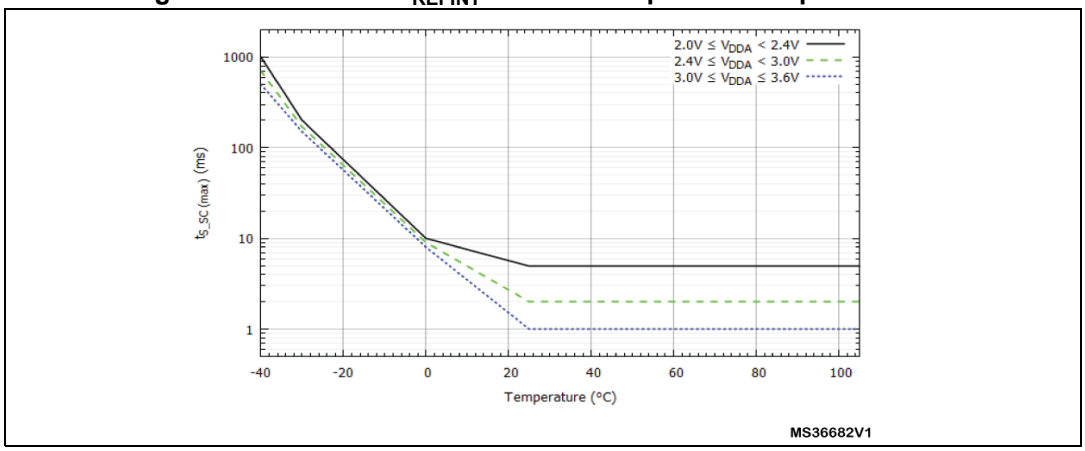
The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 38*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 38. HSE oscillator characteristics

Symbol	Parameter	Conditions(1)	Min.(2)	Typ.	Max.(2)	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
I_{DD}	HSE current consumption	During startup(3)	-	-	8.5	mA
		V_{DD}= 3.3 V, Rm= 30Ω, CL=10 pF@8 MHz	-	0.4	-	
		V_{DD}= 3.3 V, Rm= 45Ω, CL=10 pF@8 MHz	-	0.5	-	
		V_{DD}= 3.3 V, Rm= 30Ω, CL=5 pF@32 MHz	-	0.8	-	
		V_{DD}= 3.3 V, Rm= 30Ω, CL=10 pF@32 MHz	-	1	-	
		V_{DD}= 3.3 V, Rm= 30Ω, CL=20 pF@32 MHz	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 31. Maximum V_{REFINT} scaler startup time from power-down



6.3.22 Operational amplifier characteristics

Table 71. Operational amplifier characteristics(1)

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage		-	2.4	-	3.6	V
CMIR	Common mode input range		-	0	-	V_{DDA}	V
VI_{OFFSET}	Input offset voltage	Maximum calibration range	25°C, No Load on output.	-	-	4	mV
			All voltage/Temp.	-	-	6	
		After offset calibration	25°C, No Load on output.	-	-	1.6	
			All voltage/Temp.	-	-	3	
ΔVI_{OFFSET}	Input offset voltage drift		-	-	5	-	µV/°C
I_{LOAD}	Drive current		-	-	-	500	µA
IDDOPAMP	Consumption		No load, quiescent mode	-	690	1450	µA
CMRR	Common mode rejection ratio		-	-	90	-	dB
PSRR	Power supply rejection ratio		DC	73	117	-	dB
GBW	Bandwidth		-	-	8.2	-	MHz
SR	Slew rate		-	-	4.7	-	V/µs
R_{LOAD}	Resistive load		-	4	-	-	kΩ
C_{LOAD}	Capacitive load		-	-	-	50	pF

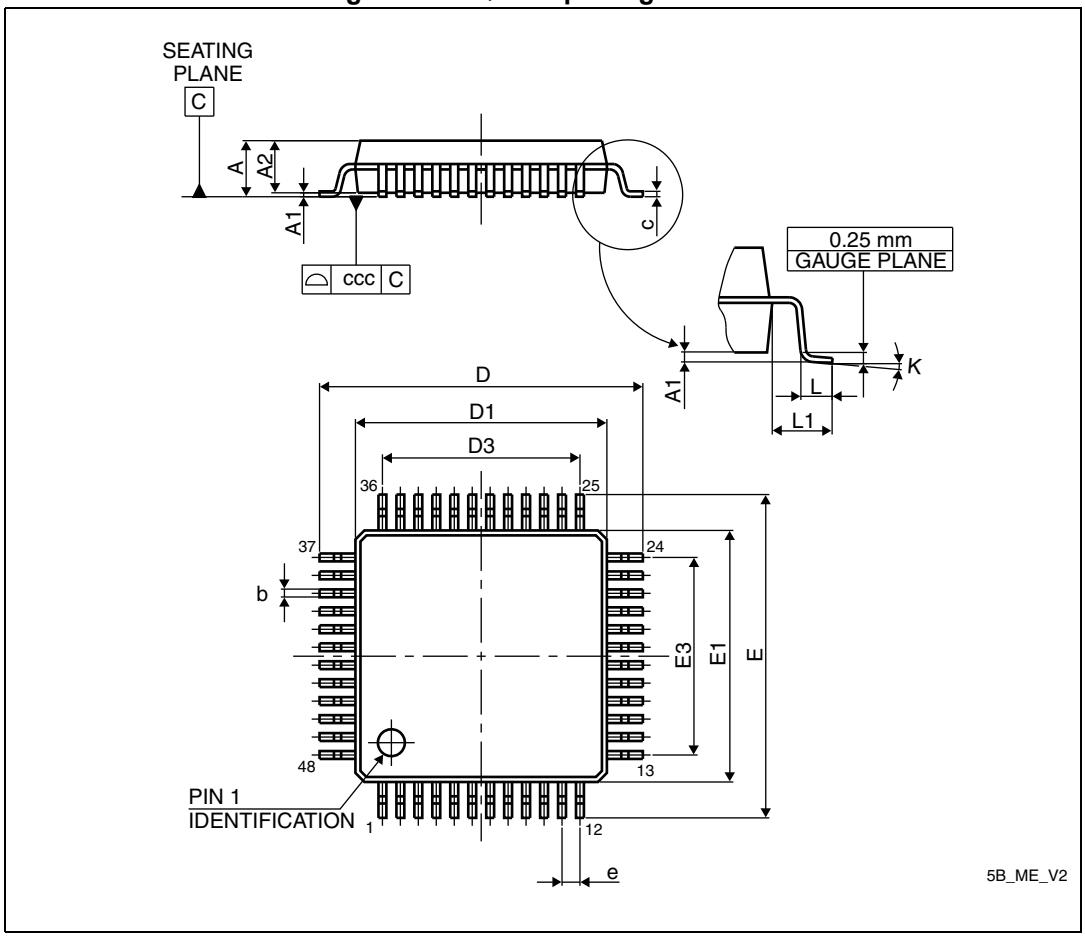
Table 71. Operational amplifier characteristics(1) (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VOH_{SAT}	High saturation voltage(2)	R_{load} = min, Input at V_{DDA}.	V_{DDA}-100	-		mV
		R_{load} = 20K, Input at V_{DDA}.	V_{DDA}-20	-		
VOL_{SAT}	Low saturation voltage	R_{load} = min, input at 0 V	-	-	100	
		R_{load} = 20K, input at 0 V.	-	-	20	
φm	Phase margin	-	-	62	-	°
$t_{OFFTRIM}$	Offset trim time: during calibration, minimum time needed between two steps to have 1 mV accuracy	-	-	-	2	ms
t_{WAKEUP}	Wake up time from OFF state.	C_{LOAD} ≤50 pf, R_{LOAD} ≥ 4 kΩ, Follower configuration	-	2.8	5	µs
$t_{S\_OPAM\_VOUT}$	ADC sampling time when reading the OPAMP output		400	-	-	ns
PGA gain	Non inverting gain value	-	-	2	-	-
			-	4	-	-
			-	8	-	-
			-	16	-	-
$R_{network}$	R2/R1 internal resistance values in PGA mode (3)	Gain=2	-	5.4/5.4	-	kΩ
		Gain=4	-	16.2/5.4	-	
		Gain=8	-	37.8/5.4	-	
		Gain=16	-	40.5/2.7	-	
PGA gain error	PGA gain error	-	-1%	-	1%	-
I_{bias}	OPAMP input bias current	-	-	-	±0.2(4)	µA
PGA BW	PGA bandwidth for different non inverting gain	PGA Gain = 2, C_{load} = 50pF, R_{load} = 4 KΩ	-	4	-	MHz
		PGA Gain = 4, C_{load} = 50pF, R_{load} = 4 KΩ	-	2	-	
		PGA Gain = 8, C_{load} = 50pF, R_{load} = 4 KΩ	-	1	-	
		PGA Gain = 16, C_{load} = 50pF, R_{load} = 4 KΩ	-	0.5	-	

7.3 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7mm low-profile quad flat package.

Figure 36. LQFP48 package outline



1. Drawing is not to scale.

Table 76. LQFP48 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-

9 Revision history

Table 80. Document revision history

Date	Revision	Changes
19-Jun-2014	1	Initial release.
09-Dec-2014	2	Updated: *Table 54: TIMx characteristics* *Table 14: STM32F303x6/8 pin definitions* *Table 59: ADC characteristics* *Table 34: Peripheral current consumption* *Table 40: HSI oscillator characteristics* *Table 17: HSI oscillator accuracy characterization results for soldered parts* *Table 2: STM32F334x4/6/8 family device features and peripheral counts*
2-Feb-2015	3	Updated: *Figure 1: STM32F334x4/6/8 block diagram* *Table 38: HSE oscillator characteristics* *Table 43: Flash memory characteristics* Added *Figure 13: High-speed external clock source AC timing diagram*
09-Jun-2015	4	Udpated : Title *Section 3.14.1: 217 ps high-resolution timer (HRTIM1)* *Section 6.1.6: Power-supply scheme* *Table 19: General operating conditions*
27-Sep-2016	5	Updated: *Section Table 69.: DAC characteristics*, *Section Table 64.: ADC characteristics*,*Table 53: NRST pin characteristics*, *Figure 2: Clock tree*,*Table 13: STM32F334x4/6/8 pin definitions*, *Table 71: Operational amplifier characteristics*, *Figure 20: Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port*, *Table 23: Embedded internal reference voltage*, *Table 39: LSE oscillator characteristics (fLSE = 32.768 kHz)* Added: *Table 35: Wakeup time using USART*