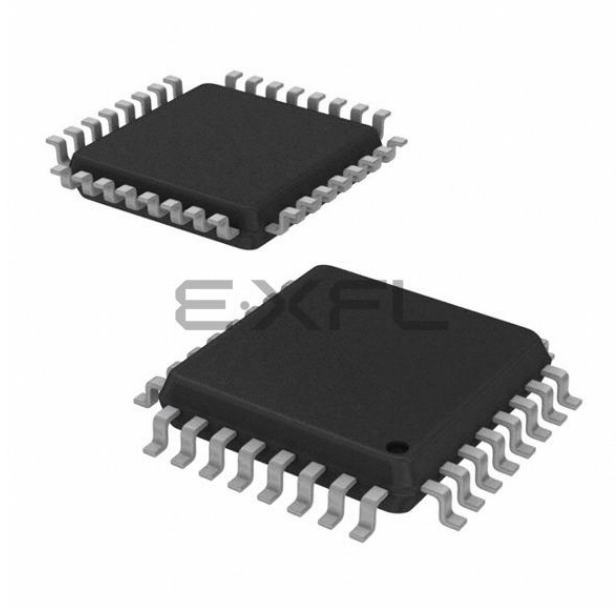


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 9x12b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f334k8t6

Contents

3.5 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Table 4. STM32F334x4/6/8 peripheral interconnect matrix

Interconnect source	Interconnect destination	Interconnect action
TIMx	TIMx	Timers synchronization or chaining
	ADCx DACx	Conversion triggers
	DMA	Memory to memory transfer trigger
	COMPx	Comparator output blanking
COMPx	TIMx	Timer input: ocrefclear input, input capture
ADCx	TIM/HRTIM1	Timer triggered by analog watchdog
GPIO RTCCLK HSE/32 MC0	TIM16	Clock source used as input channel for HSI and LSI calibration
CSS CPU (hard fault) RAM (parity error) COMPx PVD GPIO	TIM1 TIM15, 16, 17	Timer break
GPIO	TIMx	External trigger, timer break
	ADCx DACx	Conversion external trigger
DACx	COMPx	Comparator inverting input
HRTIM1	DACx/ADCx	Conversion trigger
COMPx	HRTIM1	COMPx output is an input event or a fault input for HRTIM1
OPAMP2	HRTIM1	OPAMP2 output is an input event for HRTIM1
GPIO	HRTIM1	External fault/event/ Synchro inputs for HRTIM1
HRTIM1	GPIO	Synchro output for HRTIM1

Note: For more details about the interconnect actions, refer to the corresponding sections in the RM0364 reference manual.

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed, following a specific sequence to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

3.8 Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 7 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers, high-resolution timer, DAC and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F334x4/6/8 devices embed a nested vectored interrupt controller (NVIC) able to handle up to 60 interrupt channels, that can be masked and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The external interrupt/event controller consists of 27 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked

Table 12. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TT	3.3 V tolerant I/O
		TC	Standard 3.3 V I/O
		B	Dedicated BOOT0 pin
		RST	Bi-directional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 13. STM32F334x4/6/8 pin definitions

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Pin functions	
LQFP 32	LQFP 48	LQFP 64				Alternate functions	Additional functions
-	1	1	VBAT	S	-	Backup power supply	
-	2	2	PC13(1)	I/O	TC	TIM1_CH1N	RTC_TAMP1/RTC_TS/ RTC_OUT/WKUP2
-	3	3	PC14 / OSC32_IN(1)	I/O	TC	-	OSC32_IN
-	4	4	PC15 / OSC32_OUT(1)	I/O	TC	-	OSC32_OUT
2	5	5	PF0 / OSC_IN	I/O	FT	TIM1_CH3N	OSC_IN
3	6	6	PF1 / OSC_OUT	I/O	FT	-	OSC_OUT
4	7	7	NRST	I/O	RST	Device reset input / internal reset output (active low)	

Table 13. STM32F334x4/6/8 pin definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Pin functions	
LQFP 32	LQFP 48	LQFP 64				Alternate functions	Additional functions
-	27	35	PB14	I/O	TTa	TIM15_CH1, TSC_G6_IO4, TIM1_CH2N, USART3_RTS_DE, HRTIM1_CHD1, EVENTOUT	ADC2_IN14, OPAMP2_VINP
-	28	36	PB15	I/O	TTa	TIM15_CH2, TIM15_CH1N, TIM1_CH3N, HRTIM1_CHD2, EVENTOUT	ADC2_IN15, COMP6_INM, RTC_REFIN
-	-	37	PC6	I/O	FT	EVENTOUT, TIM3_CH1, HRTIM1_EEV10, COMP6_OUT	-
-	-	38	PC7	I/O	FT	EVENTOUT, TIM3_CH2, HRTIM1_FLT5	-
-	-	39	PC8	I/O	FT	EVENTOUT, TIM3_CH3, HRTIM1_CHE1	-
-	-	40	PC9	I/O	FT	EVENTOUT, TIM3_CH4, HRTIM1_CHE2	-
18	29	41	PA8	I/O	FT	MCO, TIM1_CH1, USART1_CK, HRTIM1_CHA1, EVENTOUT	-
19	30	42	PA9	I/O	FT	TSC_G4_IO1, TIM1_CH2, USART1_TX, TIM15_BKIN, TIM2_CH3, HRTIM1_CHA2, EVENTOUT	-
20	31	43	PA10	I/O	FT	TIM17_BKIN, TSC_G4_IO2, TIM1_CH3, USART1_RX, COMP6_OUT, TIM2_CH4, HRTIM1_CHB1, EVENTOUT	-
21	32	44	PA11	I/O	FT	TIM1_CH1N, USART1_CTS, CAN_RX, TIM1_CH4, TIM1_BKIN2, HRTIM1_CHB2, EVENTOUT	-
22	33	45	PA12	I/O	FT	TIM16_CH1, TIM1_CH2N, USART1_RTS_DE, COMP2_OUT, CAN_TX, TIM1_ETR, HRTIM1_FLT1, EVENTOUT	-

Table 13. STM32F334x4/6/8 pin definitions (continued)

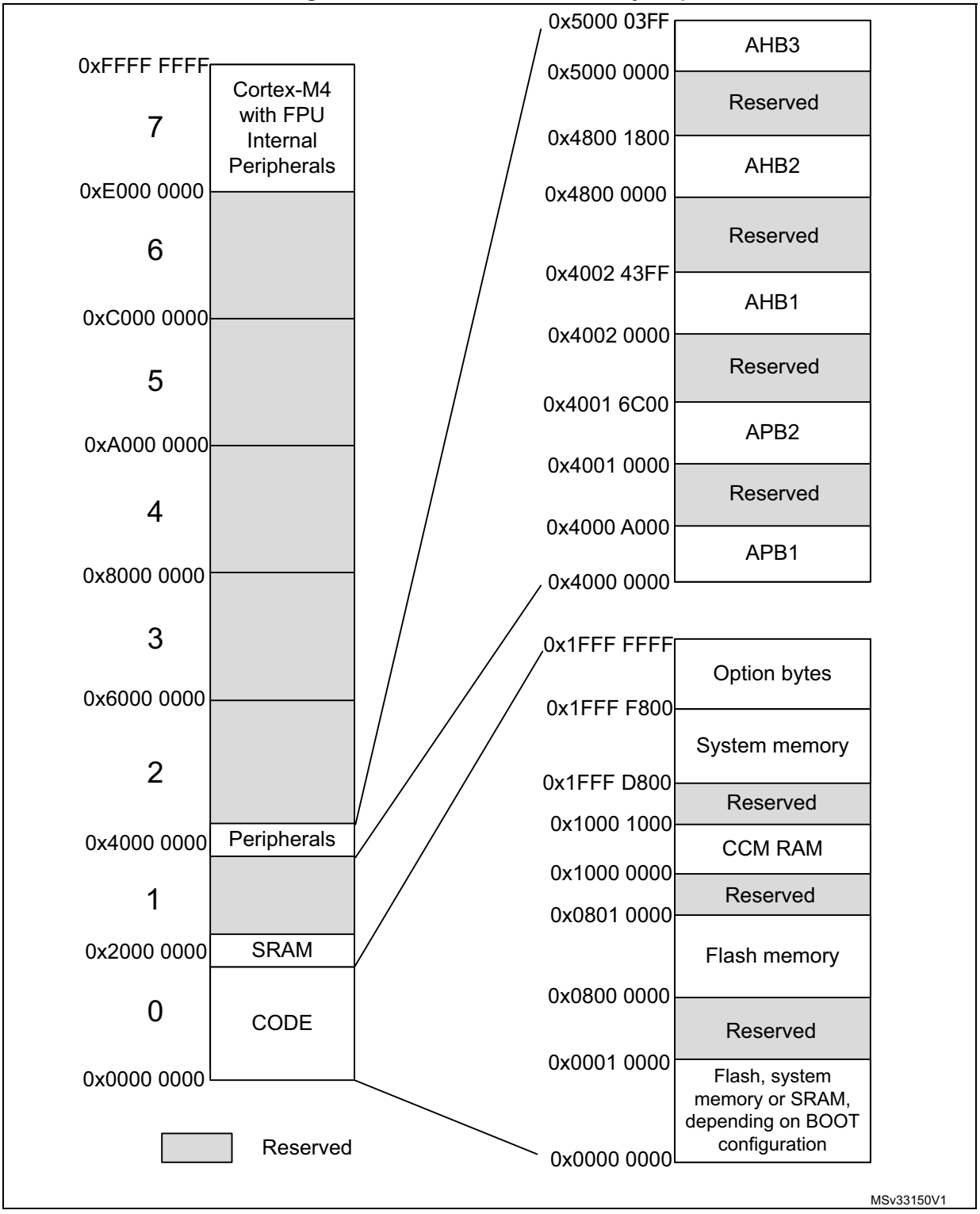
Pin Number			Pin name (function after reset)	Pin type	I/O structure	Pin functions	
LQFP 32	LQFP 48	LQFP 64				Alternate functions	Additional functions
23	34	46	PA13	I/O	FT	JTMS/SWDAT, TIM16_CH1N, TSC_G4_IO3, IR_OUT, USART3_CTS, EVENTOUT	-
-	35	47	VSS	S	-	-	-
-	36	48	VDD	S	-	-	-
24	37	49	PA14	I/O	FTf	JTCK/SWCLK, TSC_G4_IO4, I2C1_SDA, TIM1_BKIN, USART2_TX, EVENTOUT	-
25	38	50	PA15	I/O	FTf	JTDI, TIM2_CH1/TIM2_ETR, TSC_SYNC, I2C1_SCL, SPI1_NSS, USART2_RX, TIM1_BKIN, HRTIM1_FLT2, EVENTOUT	-
-	-	51	PC10	I/O	FT	EVENTOUT, USART3_TX	-
-	-	52	PC11	I/O	FT	EVENTOUT, HRTIM1_EEV2, USART3_RX	-
-	-	53	PC12	I/O	FT	EVENTOUT, HRTIM1_EEV1, USART3_CK	-
-	-	54	PD2	I/O	FT	EVENTOUT, TIM3_ETR	-
26	39	55	PB3	I/O	FT	JTDO/TRACE SWO, TIM2_CH2, TSC_G5_IO1, SPI1_SCK, USART2_TX, TIM3_ETR, HRTIM1_SCOUT, HRTIM1_EEV9, EVENTOUT	-
27	40	56	PB4	I/O	FT	NJTRST, TIM16_CH1, TIM3_CH1, TSC_G5_IO2, SPI1_MISO, USART2_RX, TIM17_BKIN, HRTIM1_EEV7, EVENTOUT	-

Table 14. Alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/TIM15/ TIM16/TIM17/ EVENT	TIM1/TIM3/ TIM15/ TIM16	HRTIM1/TSC	I2C1/TIM1	SPI1/Infrared	TIM1/Infrared	USART1/USART2/USART3/ GPCOMP6	GPCOMP2/ GPCOMP4/ GPCOMP6	CAN/TIM1/ TIM15	TIM2/TIM3 /TIM17	TIM1	HRTIM1/ TIM1	HRTIM1/ OPAMP2	-	EVENT
Port B	PB10	-	TIM2_CH3	-	TSC_SYNC	-	-	-	USART3_TX	-	-	-	-	-	HRTIM1_FLT3	-	EVENTOUT
	PB11	-	TIM2_CH4	-	TSC_G6_IO1	-	-	-	USART3_RX	-	-	-	-	-	HRTIM1_FLT4	-	EVENTOUT
	PB12	-	-	-	TSC_G6_IO2	-	-	TIM1_BKIN	USART3_CK	-	-	-	-	-	HRTIM1_CHC1	-	EVENTOUT
	PB13	-	-	-	TSC_G6_IO3	-	-	TIM1_CH1N	USART3_CTS	-	-	-	-	-	HRTIM1_CHC2	-	EVENTOUT
	PB14	-	TIM15_CH1	-	TSC_G6_IO4	-	-	TIM1_CH2N	USART3_RTS_DE	-	-	-	-	-	HRTIM1_CHD1	-	EVENTOUT
	PB15	-	TIM15_CH2	TIM15_CH1N	-	TIM1_CH3N	-	-	-	-	-	-	-	-	HRTIM1_CHD2	-	EVENTOUT
Port C	PC0	-	EVENTOUT	TIM1_CH1	-	-	-	-	-	-	-	-	-	-	-	-	-
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC2	-	EVENTOUT	TIM1_CH3	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC3	-	EVENTOUT	TIM1_CH4	-	-	-	TIM1_BKIN2	-	-	-	-	-	-	-	-	-
	PC4	-	EVENTOUT	TIM1_ETR	-	-	-	-	USART1_TX	-	-	-	-	-	-	-	-
	PC5	-	EVENTOUT	TIM15_BKIN	TSC_G3_IO1	-	-	-	USART1_RX	-	-	-	-	-	-	-	-
	PC6	-	EVENTOUT	TIM3_CH1	HRTIM1_EEV10	-	-	-	COMP6_OUT	-	-	-	-	-	-	-	-
	PC7	-	EVENTOUT	TIM3_CH2	HRTIM1_FLT5	-	-	-	-	-	-	-	-	-	-	-	-
	PC8	-	EVENTOUT	TIM3_CH3	HRTIM1_CHE1	-	-	-	-	-	-	-	-	-	-	-	-
	PC9	-	EVENTOUT	TIM3_CH4	HRTIM1_CHE2	-	-	-	-	-	-	-	-	-	-	-	-
	PC10	-	EVENTOUT	-	-	-	-	-	USART3_TX	-	-	-	-	-	-	-	-
	PC11	-	EVENTOUT	-	HRTIM1_EEV2	-	-	-	USART3_RX	-	-	-	-	-	-	-	-
	PC12	-	EVENTOUT	-	HRTIM1_EEV1	-	-	-	USART3_CK	-	-	-	-	-	-	-	-
	PC13	-	-	-	-	TIM1_CH1N	-	-	-	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Port D	PD2	-	EVENTOUT	TIM3_ETR	-	-	-	-	-	-	-	-	-	-	-	-	-
Port F	PF0	-	-	-	-	-	-	TIM1_CH3N	-	-	-	-	-	-	-	-	-
	PF1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

5 Memory mapping

Figure 7. STM32F334x4/6/8 memory map



On-chip peripheral current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input configuration
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption:
  - With all peripherals clocked off
  - With only one peripheral clocked on
- Ambient operating temperature at 25°C and $V_{DD} = V_{DDA} = 3.3$ V

Table 33. Peripheral current consumption

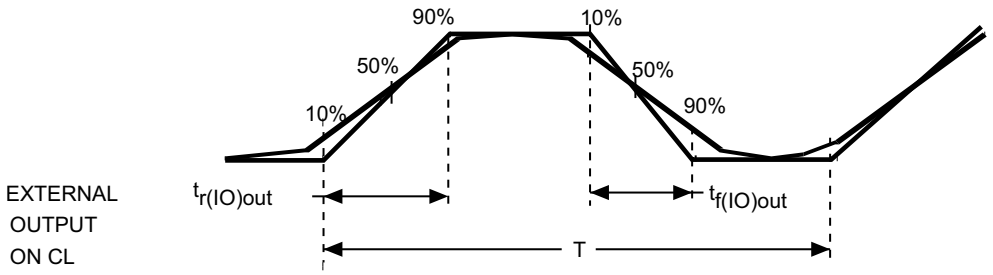
Peripheral	Typical consumption(1)	Unit
	I_{DD}	
BusMatrix (2)	11.1	µA/MHz
DMA1	8.0	-
CRC	2.1	-
GPIOA	8.7	-
GPIOB	8.4	-
GPIOC	8.4	-
GPIOD	2.6	-
GPIOF	1.7	-
TSC	4.7	-
ADC1&2	17.4	-
APB2-Bridge (3)	3.3	-
SYSCFG	4.2	-
TIM1	32.3	-
USART1	20.3	-
TIM15	13.8	-
TIM16	9.7	-
TIM17	10.3	-
HRTIM	324.2	-
APB1-Bridge (3)	5.3	-
TIM2	43.4	-
TIM3	34.0	-
TIM6	9.7	-
TIM7	10.3	-
WWDG	6.9	-
USART2	18.8	-
USART3	19.1	-

Table 52. I/O AC characteristics(1)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min.	Max.	Unit
x0	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	2(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	10(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	25 (3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25 (3)	
11	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	50(3)	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	30(3)	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	20(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
FM+ configuration(4)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	2(4)	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	12(4)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	34(4)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0364 reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 22*.
3. Guaranteed by design, not tested in production.
4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the RM0364 reference manual for a description of FM+ I/O mode configuration.

Figure 22. I/O AC characteristics definition



Maximum frequency is achieved if (t_r + t_f) ≤ (2/3)T and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

ai14131d

6.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 50*).

Unless otherwise specified, the parameters given in *Table 53* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 19*.

Table 53. NRST pin characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	-	-	$0.3V_{DD}$+ 0.07(1)	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	$0.445V_{DD}$+ 0.398(1)	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100(1)	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	500(1)	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Table 60. IWDG min./max. timeout period at 40 kHz (LSI) (1)

Prescaler divider	PR[2:0] bits	Min. timeout (ms) RL[11:0]= 0x000	Max. timeout (ms) RL[11:0]= 0xFFF
/4	0	0.1	409.6
/8	1	0.2	819.2
/16	2	0.4	1638.4
/32	3	0.8	3276.8
/64	4	1.6	6553.6
/128	5	3.2	13107.2
/256	7	6.4	26214.4

1. These timings are given for a 40 kHz clock but the microcontroller's internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 61. WWDG min./max. timeout value at 72 MHz (PCLK)(1)

Prescaler	WDGTB	Min. timeout value	Max. timeout value
1	0	0.05687	3.6409
2	1	0.1137	7.2817
4	2	0.2275	14.564
8	3	0.4551	29.127

1. Guaranteed by design, not tested in production.

6.3.18 Communication interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 Kbit/s
- Fast-mode (Fm): with a bit rate up to 400 Kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I²C peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDD is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.14: I/O port characteristics* for the I²C I/O characteristics.

All I²C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 62. I^2C analog filter characteristics(1)

Symbol	Parameter	Min.	Max.	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter.	50(2)	260(3)	ns

1. Guaranteed by design, not tested in production.
2. Spikes with width below t_{AF}(min.) are filtered.
3. Spikes with width above t_{AF}(max.) are not filtered.

SPI characteristics

Unless otherwise specified, the parameters given in *Table 53* for SPI are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 19: General operating conditions*.

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 63. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode 2.7<V_{DD}<3.6	-	-	24	MHz
		Master mode 2<V_{DD}<3.6			18	
		Slave mode 2<V_{DD}<3.6			24	
		Slave mode transmitter/full duplex 2<V_{DD}<3.6			18(2)	
DuCy(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	0	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	-	
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	10	-	40	
$t_{dis(SO)}$	Data output disable time	Slave mode	10	-	17	
$t_{v(SO)}$	Data output valid time	Slave mode 2.7<V_{DD}<3.6V	-	12	20	
		Slave mode 2<V_{DD}<3.6V	-	12	27.5	
$t_{v(MO)}$		Master mode	-	1.5	5	
$t_{h(SO)}$	Data output hold time	Slave mode	7.5	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Data based on characterization results, not tested in production.
2. Maximum frequency in Slave transmitter mode is determined by the sum of tv(SO) and tsu(MI) which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having tsu(MI) = 0 while Duty(SCK) = 50%.

Table 64. ADC characteristics (continued)

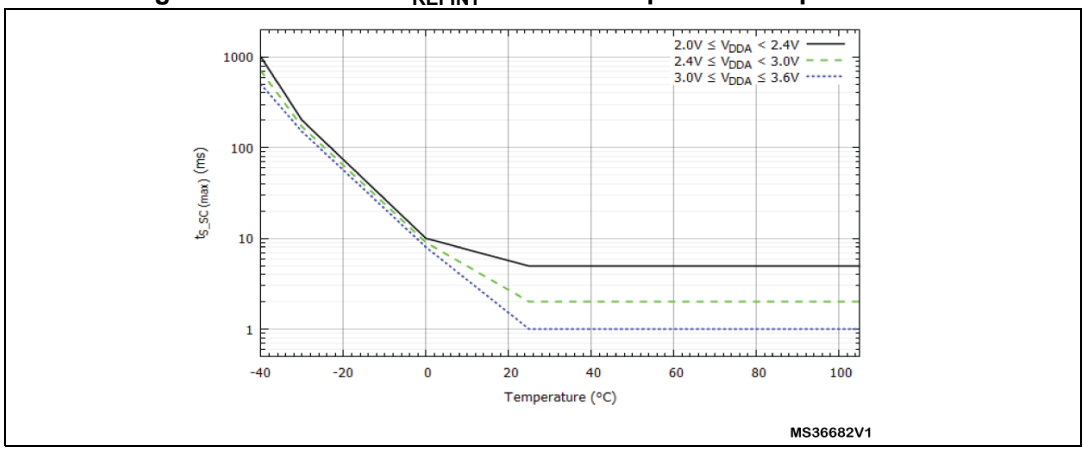
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{REF-}	Negative reference voltage			0		V
f_{ADC}	ADC clock frequency	-	0.14	-	72	MHz
f_S(1)	Sampling rate	Resolution = 12 bits, Fast Channel	0.01	-	5.14	MSPS
		Resolution = 10 bits, Fast Channel	0.012	-	6	
		Resolution = 8 bits, Fast Channel	0.014	-	7.2	
		Resolution = 6 bits, Fast Channel	0.0175	-	9	
f_{TRIG}(1)	External trigger frequency	f_{ADC} = 72 MHz Resolution = 12 bits	-	-	5.14	MHz
		Resolution = 12 bits	-	-	14	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN}(1)	External input impedance	-	-	-	100	kΩ
C_{ADC}(1)	Internal sample and hold capacitor	-	-	5	-	pF
t_{CAL}(1)	Calibration time	f_{ADC} = 72 MHz	1.56			µs
		-	112			$1/f_{ADC}$
t_{latr}(1)	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2	$1/f_{ADC}$
		CKMODE = 10	-	-	2.25	$1/f_{ADC}$
		CKMODE = 11	-	-	2.125	$1/f_{ADC}$
$t_{latrinj}$(1)	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3	$1/f_{ADC}$
		CKMODE = 10	-	-	3.25	$1/f_{ADC}$
		CKMODE = 11	-	-	3.125	$1/f_{ADC}$
t_S(1)	Sampling time	f_{ADC} = 72 MHz	0.021	-	8.35	µs
		-	1.5	-	601.5	$1/f_{ADC}$
$t_{ADCVREG\_STUP}$(1)	ADC Voltage Regulator Start-up time	-	-	-	10	µs
t_{STAB}	Power-up time	-	1			conversion cycle

Table 65. Maximum ADC R_{AIN}(1) (continued)

Resolution	Sampling cycle @ 72 MHz	Sampling time [ns] @ 72 MHz	R_{AIN} max. (kΩ)		
			Fast channels(2)	Slow channels	Other channels(3)
10 bits	1.5	20.83	0.082	NA	NA
	2.5	34.72	0.270	0.082	0.100
	4.5	62.50	0.560	0.390	0.330
	7.5	104.17	1.20	0.82	0.68
	19.5	270.83	3.30	2.70	2.20
	61.5	854.17	10.0	8.2	6.8
	181.5	2520.83	33.0	27.0	22.0
	601.5	8354.17	100.0	82.0	68.0
8 bits	1.5	20.83	0.150	NA	0.039
	2.5	34.72	0.390	0.180	0.180
	4.5	62.50	0.820	0.560	0.470
	7.5	104.17	1.50	1.20	1.00
	19.5	270.83	3.90	3.30	2.70
	61.5	854.17	12.00	12.00	8.20
	181.5	2520.83	39.00	33.00	27.00
	601.5	8354.17	100.00	100.00	82.00
6 bits	1.5	20.83	0.270	0.100	0.150
	2.5	34.72	0.560	0.390	0.330
	4.5	62.50	1.200	0.820	0.820
	7.5	104.17	2.20	1.80	1.50
	19.5	270.83	5.60	4.70	3.90
	61.5	854.17	18.0	15.0	12.0
	181.5	2520.83	56.0	47.0	39.0
	601.5	8354.17	100.00	100.0	100.0

1. Data based on characterization results, not tested in production.
2. All fast channels, expect channel on PA6.
3. Channels available on PA6.

Figure 31. Maximum V_{REFINT} scaler startup time from power-down



6.3.22 Operational amplifier characteristics

Table 71. Operational amplifier characteristics(1)

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage		-	2.4	-	3.6	V
CMIR	Common mode input range		-	0	-	V_{DDA}	V
VI_{OFFSET}	Input offset voltage	Maximum calibration range	25°C, No Load on output.	-	-	4	mV
			All voltage/Temp.	-	-	6	
		After offset calibration	25°C, No Load on output.	-	-	1.6	
			All voltage/Temp.	-	-	3	
ΔVI_{OFFSET}	Input offset voltage drift		-	-	5	-	µV/°C
I_{LOAD}	Drive current		-	-	-	500	µA
IDDOPAMP	Consumption		No load, quiescent mode	-	690	1450	µA
CMRR	Common mode rejection ratio		-	-	90	-	dB
PSRR	Power supply rejection ratio		DC	73	117	-	dB
GBW	Bandwidth		-	-	8.2	-	MHz
SR	Slew rate		-	-	4.7	-	V/µs
R_{LOAD}	Resistive load		-	4	-	-	kΩ
C_{LOAD}	Capacitive load		-	-	-	50	pF

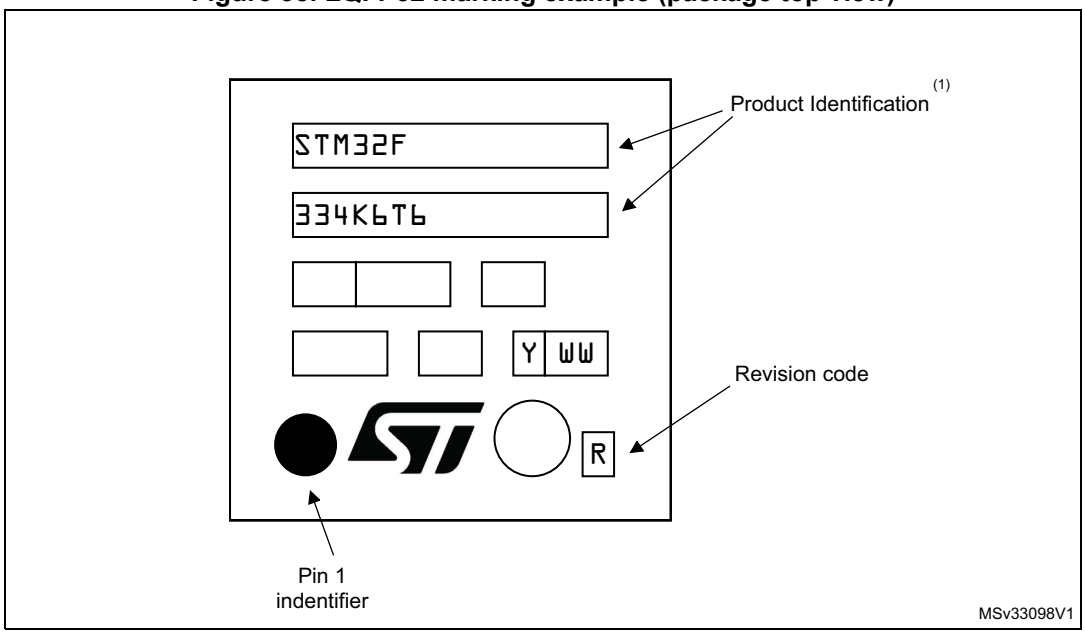
Table 71. Operational amplifier characteristics(1) (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VOH_{SAT}	High saturation voltage(2)	R_{load} = min, Input at V_{DDA}.	V_{DDA}-100	-		mV
		R_{load} = 20K, Input at V_{DDA}.	V_{DDA}-20	-		
VOL_{SAT}	Low saturation voltage	R_{load} = min, input at 0 V	-	-	100	
		R_{load} = 20K, input at 0 V.	-	-	20	
φm	Phase margin	-	-	62	-	°
$t_{OFFTRIM}$	Offset trim time: during calibration, minimum time needed between two steps to have 1 mV accuracy	-	-	-	2	ms
t_{WAKEUP}	Wake up time from OFF state.	C_{LOAD} ≤50 pf, R_{LOAD} ≥ 4 kΩ, Follower configuration	-	2.8	5	µs
$t_{S\_OPAM\_VOUT}$	ADC sampling time when reading the OPAMP output		400	-	-	ns
PGA gain	Non inverting gain value	-	-	2	-	-
			-	4	-	-
			-	8	-	-
			-	16	-	-
$R_{network}$	R2/R1 internal resistance values in PGA mode (3)	Gain=2	-	5.4/5.4	-	kΩ
		Gain=4	-	16.2/5.4	-	
		Gain=8	-	37.8/5.4	-	
		Gain=16	-	40.5/2.7	-	
PGA gain error	PGA gain error	-	-1%	-	1%	-
I_{bias}	OPAMP input bias current	-	-	-	±0.2(4)	µA
PGA BW	PGA bandwidth for different non inverting gain	PGA Gain = 2, C_{load} = 50pF, R_{load} = 4 KΩ	-	4	-	MHz
		PGA Gain = 4, C_{load} = 50pF, R_{load} = 4 KΩ	-	2	-	
		PGA Gain = 8, C_{load} = 50pF, R_{load} = 4 KΩ	-	1	-	
		PGA Gain = 16, C_{load} = 50pF, R_{load} = 4 KΩ	-	0.5	-	

Device marking for LQFP32

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 35. LQFP32 marking example (package top view)

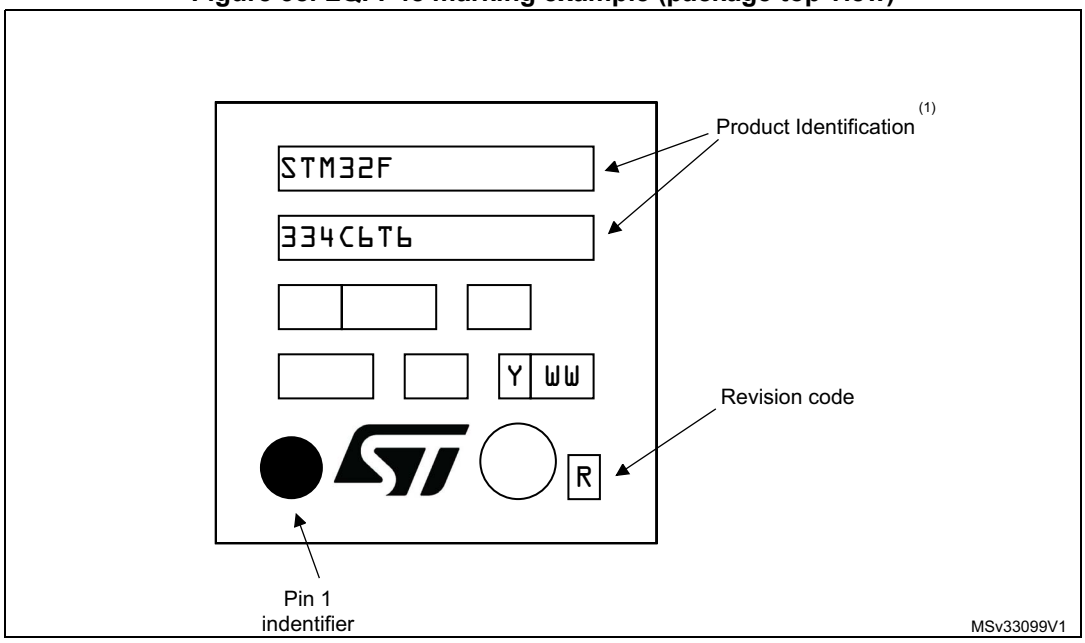


1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Device marking for LQFP48

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 38. LQFP48 marking example (package top view)

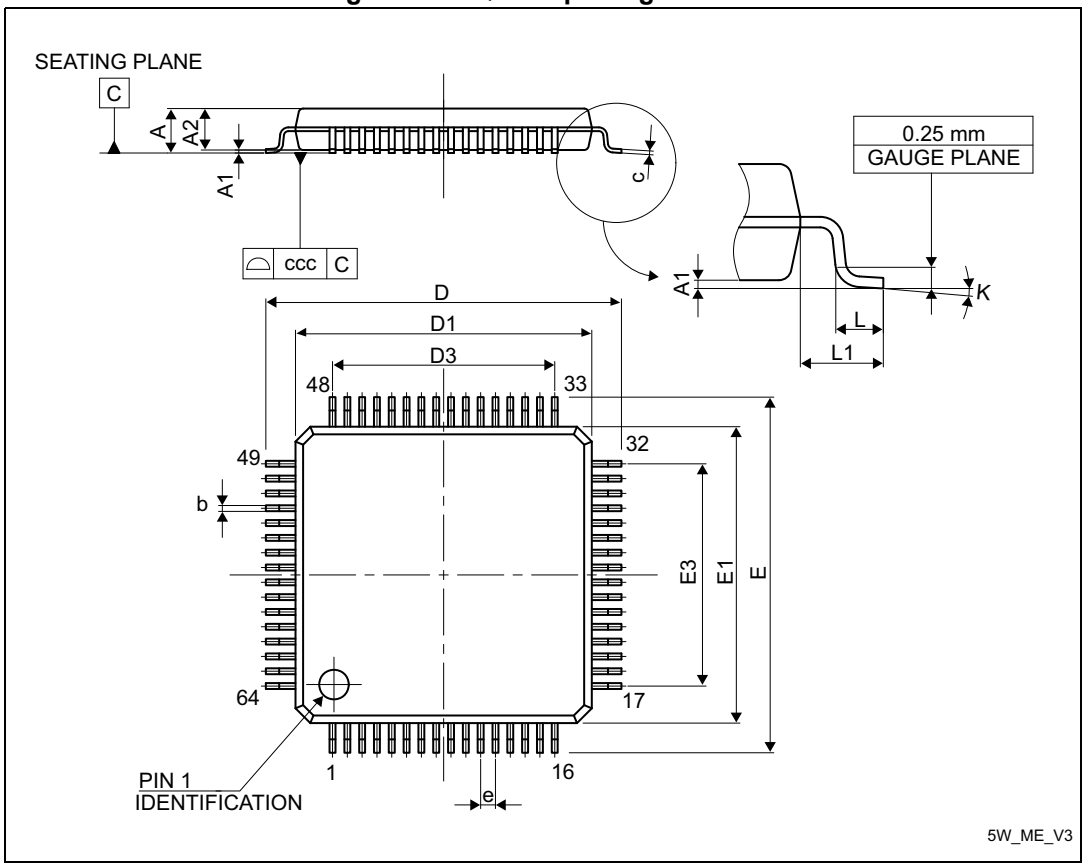


1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.4 LQFP64 package information

LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package.

Figure 39. LQFP64 package outline



1. Drawing is not to scale.

Table 77. LQFP64 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	11.800	12.000	-	-	0.4724	-
D1	9.800	10.000	-	-	0.3937	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
e	-	0.500	-	-	0.0197	-