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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 21x12b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f334r8t6

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3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

TIM1and HRTIM1 maximum frequency is 144 MHz.

3.16 Communication interfaces

3.16.1 Inter-integrated circuit interface (I^2C)

The devices feature an I^2C bus interface which can operate in multimaster and slave mode. It can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes.

It supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). It also includes programmable analog and digital noise filters.

Table 6. Comparison of I^2C analog and digital filters

-	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, it provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. It also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I^2C interface can be served by the DMA controller.

The features available in I2C1 are showed below in *Table 7*.

Table 7. STM32F334x4/6/8 I^2C implementation

I^2C features(1)	I2C1
7-bit addressing mode	X
10-bit addressing mode	X
Standard mode (up to 100 kbit/s)	X
Fast mode (up to 400 kbit/s)	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X
Independent clock	X
SMBus	X
Wakeup from STOP	X

1. X = supported.

Table 9. STM32F334x4/6/8 SPI implementation (continued)

SPI features(1)	SPI1
NSS pulse mode	X
TI mode	X

1. X = supported.

3.16.4 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

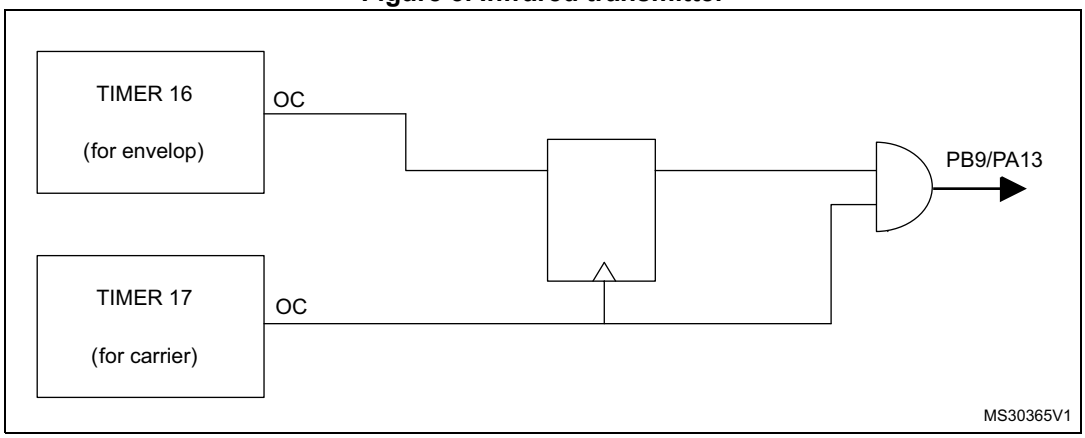
3.17 Infrared transmitter

The STM32F334x4/6/8 devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

Figure 3. Infrared transmitter



3.18 Touch sensing controller (TSC)

The STM32F334x4/6/8 devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 18 capacitive sensing channels distributed over 6 analog I/Os group.

Capacitive sensing technology is able to detect the presence of a finger near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of

Table 13. STM32F334x4/6/8 pin definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Pin functions	
LQFP 32	LQFP 48	LQFP 64				Alternate functions	Additional functions
28	41	57	PB5	I/O	FT	TIM16_BKIN, TIM3_CH2, I2C1_SMBA, SPI1_MOSI, USART2_CK, TIM17_CH1, HRTIM1_EEV6, EVENTOUT	-
29	42	58	PB6	I/O	FTf	TIM16_CH1N, TSC_G5_IO3, I2C1_SCL, USART1_TX, HRTIM1_SCIN, HRTIM1_EEV4, EVENTOUT	-
30	43	59	PB7	I/O	FTf	TIM17_CH1N, TSC_G5_IO4, I2C1_SDA, USART1_RX, TIM3_CH4, HRTIM1_EEV3, EVENTOUT	-
31	44	60	BOOT0	I	B	-	-
-	45	61	PB8	I/O	FTf	TIM16_CH1, TSC_SYNC, I2C1_SCL, USART3_RX, CAN_RX, TIM1_BKIN, HRTIM1_EEV8, EVENTOUT	-
-	46	62	PB9	I/O	FTf	TIM17_CH1, I2C1_SDA, IR_OUT, USART3_TX, COMP2_OUT, CAN_TX, HRTIM1_EEV5, EVENTOUT	-
32	47	63	VSS	S	-	-	-
1	48	64	VDD	S	-	-	-

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch sinks only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
   After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the reference manual.
2. Fast ADC channel.
3. These GPIOs offer a reduced touch sensing sensitivity. It is thus recommended to use them as sampling capacitor I/O.

Table 14. Alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/TIM15/ TIM16/TIM17/ EVENT	TIM1/TIM3/ TIM15/ TIM16	HRTIM1/TSC	I2C1/TIM1	SPI1/Infrared	TIM1/Infrared	USART1/USA RT2/USART3/ GPCOMP6	GPCOMP2/ GPCOMP4/ GPCOMP6	CAN/TIM1/ TIM15	TIM2/TIM3 /TIM17	TIM1	HRTIM1/ TIM1	HRTIM1/ OPAMP2	-	EVENT
Port A	PA0	-	TIM2_CH1/TI M2_ETR	-	TSC_G1_IO1	-	-	-	USART2_CTS	-	-	-	-	-	-	-	EVENTOUT
	PA1	-	TIM2_CH2	-	TSC_G1_IO2	-	-	-	USART2_RTS _DE	-	TIM15_CH1N	-	-	-	-	-	EVENTOUT
	PA2	-	TIM2_CH3	-	TSC_G1_IO3	-	-	-	USART2_TX	COMP2_OUT	TIM15_CH1	-	-	-	-	-	EVENTOUT
	PA3	-	TIM2_CH4	-	TSC_G1_IO4	-	-	-	USART2_RX	-	TIM15_CH2	-	-	-	-	-	EVENTOUT
	PA4	-	-	TIM3_CH2	TSC_G2_IO1	-	SPI1_NSS	-	USART2_CK	-	-	-	-	-	-	-	EVENTOUT
	PA5	-	TIM2_CH1/TI M2_ETR	-	TSC_G2_IO2	-	SPI1_SCK	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA6	-	TIM16_CH1	TIM3_CH1	TSC_G2_IO3	-	SPI1_MISO	TIM1_BKIN	-	-	-	-	-	-	OPAMP2_DIG	-	EVENTOUT
	PA7	-	TIM17_CH1	TIM3_CH2	TSC_G2_IO4	-	SPI1_MOSI	TIM1_CH1N	-	-	-	-	-	-	-	-	EVENTOUT
	PA8	MCO	-	-	-	-	-	TIM1_CH1	USART1_CK	-	-	-	-	-	HRTIM1_CHA1	v	EVENTOUT
	PA9	-	-	-	TSC_G4_IO1	-	-	TIM1_CH2	USART1_TX	-	TIM15_BKIN	TIM2_CH3	-	-	HRTIM1_CHA2	-	EVENTOUT
	PA10	-	TIM17_BKIN	-	TSC_G4_IO2	-	-	TIM1_CH3	USART1_RX	COMP6_OUT	-	TIM2_CH4	-	-	HRTIM1_CHB1	-	EVENTOUT
	PA11	-	-	-	-	-	-	TIM1_CH1N	USART1_CTS	-	CAN_RX	-	TIM1_CH4	TIM1_BKIN2	HRTIM1_CHB2	-	EVENTOUT
	PA12	-	TIM16_CH1	-	-	-	-	TIM1_CH2N	USART1_RTS _DE	COMP2_OUT	CAN_TX	-	TIM1_ETR	-	HRTIM1_FLT1	-	EVENTOUT
	PA13	JTMS/SWDAT	TIM16_CH1N	-	TSC_G4_IO3	-	IR_OUT	-	USART3_CTS	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK/SWCLK	-	-	TSC_G4_IO4	I2C1_SDA	-	TIM1_BKIN	USART2_TX	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM2_CH1/ TIM2_ETR	-	TSC_SYNC	I2C1_SCL	SPI1_NSS	-	USART2_RX	-	TIM1_BKIN	-	-	-	HRTIM1_FLT2	-	EVENTOUT
Port B	PB0	-	-	TIM3_CH3	TSC_G3_IO2	-	-	TIM1_CH2N	-	-	-	-	-	-	-	-	EVENTOUT
	PB1	-	-	TIM3_CH4	TSC_G3_IO3	-	-	TIM1_CH3N	-	COMP4_OUT	-	-	-	-	HRTIM1_SCOUT	-	EVENTOUT
	PB2	-	-	-	TSC_G3_IO4	-	-	-	-	-	-	-	-	-	HRTIM1_SCIN	-	EVENTOUT
	PB3	JTDO/TRACE SWO	TIM2_CH2	-	TSC_G5_IO1	-	SPI1_SCK	-	USART2_TX	-	-	TIM3_ETR	-	HRTIM1_SC OUT	HRTIM1_EEV9	-	EVENTOUT
	PB4	NJTRST	TIM16_CH1	TIM3_CH1	TSC_G5_IO2	-	SPI1_MISO	-	USART2_RX	-	-	TIM17_BK IN	-	-	HRTIM1_EEV7	-	EVENTOUT
	PB5	-	TIM16_BKIN	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI	-	USART2_CK	-	-	TIM17_CH 1	-	-	HRTIM1_EEV6	-	EVENTOUT
	PB6	-	TIM16_CH1N	-	TSC_G5_IO3	I2C1_SCL	-	-	USART1_TX	-	-	-	-	HRTIM1_SCI N	HRTIM1_EEV4	-	EVENTOUT
	PB7	-	TIM17_CH1N	-	TSC_G5_IO4	I2C1_SDA	-	-	USART1_RX	-	-	TIM3_CH4	-	-	HRTIM1_EEV3	-	EVENTOUT
	PB8	-	TIM16_CH1	-	TSC_SYNC	I2C1_SCL	-	-	USART3_RX	-	CAN_RX	-	-	TIM1_BKIN	HRTIM1_EEV8	-	EVENTOUT
	PB9	-	TIM17_CH1	-	-	I2C1_SDA	-	IR_OUT	USART3_TX	COMP2_OUT	CAN_TX	-	-	-	HRTIM1_EEV5	-	EVENTOUT

Table 15. STM32F334x4/6/8 peripheral register boundary addresses

Bus	Boundary address	Size (bytes)	Peripheral
AHB3	0x5000 0000 - 0x5000 03FF	1 K	ADC1 - ADC2
-	0x4800 1800 - 0x4FFF FFFF	~132 M	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1 K	GPIOF
-	0x4800 1000 - 0x4800 13FF	1 K	Reserved
AHB2	0x4800 0C00 - 0x4800 0FFF	1 K	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 K	GPIOC
	0x4800 0400 - 0x4800 07FF	1 K	GPIOB
	0x4800 0000 - 0x4800 03FF	1 K	GPIOA
-	0x4002 4400 - 0x47FF FFFF	~128 M	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 K	TSC
	0x4002 3400 - 0x4002 3FFF	3 K	Reserved
	0x4002 3000 - 0x4002 33FF	1 K	CRC
	0x4002 2400 - 0x4002 2FFF	3 K	Reserved
	0x4002 2000 - 0x4002 23FF	1 K	Flash interface
	0x4002 1400 - 0x4002 1FFF	3 K	Reserved
	0x4002 1000 - 0x4002 13FF	1 K	RCC
	0x4002 0400 - 0x4002 0FFF	3 K	Reserved
	0x4002 0000 - 0x4002 03FF	1 K	DMA1
-	0x4001 8000 - 0x4001 FFFF	32 K	Reserved
APB2	0x4001 7400 - 0x4001 77FF	1 K	HRTIM1
	0x4001 4C00 - 0x4001 73FF	12 K	Reserved
	0x4001 4800 - 0x4001 4BFF	1 K	TIM17
	0x4001 4400 - 0x4001 47FF	1 K	TIM16
	0x4001 4000 - 0x4001 43FF	1 K	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 K	Reserved
APB2	0x4001 3800 - 0x4001 3BFF	1 K	USART1
	0x4001 3400 - 0x4001 37FF	1 K	Reserved
	0x4001 3000 - 0x4001 33FF	1 K	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 K	TIM1
	0x4001 0800 - 0x4001 2BFF	9 K	Reserved
	0x4001 0400 - 0x4001 07FF	1 K	EXTI
	0x4001 0000 - 0x4001 03FF	1 K	SYSCFG + COMP + OPAMP
-	0x4000 9C00 - 0x4000 FFFF	25 K	Reserved

Table 17. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD_x power lines (source)(1)	140	mA
ΣI_{VSS}	Total current out of sum of all VSS_x ground lines (sink)(1)	-140	
I_{VDD}	Maximum current into each V_{DD_x} power line (source)(1)	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	80	
	Total output current sourced by sum of all I/Os and control pins(2)	-80	
$I_{INJ(PIN)}$	Injected current on TT, FT, FTf and B pins(3)	-5 /+0	
	Injected current on TC and RST pin(4)	±5	
	Injected current on TTa pins(5)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS} and V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins.The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 16: Voltage characteristics* for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. I_{INJ}(PIN) must never be exceeded. Refer also to *Table 16: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note 2. below *Table 64*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 18. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 19. General operating conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	
f_{PCLK2}	Internal APB2 clock frequency	-	0	72	
V_{DD}	Standard operating voltage	-	2	3.6	V
V_{DD18}	Core, SRAM and Flash memory power supply	-	1.65	1.95	
V_{DDA}	Analog operating voltage (OPAMP and DAC not used)	Must have a potential equal to or higher than V_{DD}	2	3.6	
	Analog operating voltage (OPAMP and DAC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.65	3.6	V
V_{IN}	I/O input voltage	TC I/O	–0.3	V_{DD}+0.3	V
		TT I/O	-0.3	3.6	
		TTa I/O	–0.3	V_{DDA}+0.3	
		FT and FTf I/O(1)	–0.3	5.5	
		BOOT0	0	5.5	
PD	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(2)	LQFP64	-	444	mW
PD	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(2)	LQFP48	-	364	mW
PD	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7	LQFP32	-	333	mW
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(3)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low power dissipation(3)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. To sustain a voltage higher than V_{DD}+0.3 V, the internal pull-up/pull-down resistors must be disabled.
2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Section Table 78.: Package thermal characteristics*).
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.5: Thermal characteristics*).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 20* are derived from tests performed under the ambient temperature condition summarized in *Table 19*.

Table 20. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Characteristics of the embedded reset and power-control block

The parameters given in *Table 21* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 19*.

Table 21. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{POR/PDR}$(1)	Power on/power down reset threshold	Falling edge	1.8(2)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$(1)	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(3)	POR reset temporization	-	1.5	2.5	4.5	ms

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD}.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Guaranteed by design, not tested in production.

Table 26. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ.	Max. @ T_A(2)			Typ.	Max. @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run/Sleep mode, code executing from Flash or RAM	HSE bypass	72 MHz	224	252(3)	265	269(3)	245	272(3)	288	295(3)	µA
			64 MHz	196	225	237	241	214	243	257	263	
			48 MHz	147	174	183	186	159	186	196	201	
			32 MHz	100	126	133	135	109	133	142	145	
			24 MHz	79	102	107	108	85	108	113	116	
			8 MHz	3	5	5	6	4	6	6	7	
			1 MHz	3	5	5	6	3	5	6	6	
		HSI clock	64 MHz	259	288	304	309	285	315	332	338	
			48 MHz	208	239	251	254	230	258	271	277	
			32 MHz	162	190	198	202	179	206	216	219	
			24 MHz	140	168	175	178	155	181	188	191	
			8 MHz	62	85	88	89	71	94	96	98	

1. Current consumption from the V_{DDA} supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production.
3. Data based characterization results and tested in production with code executing from RAM.

Table 27. Typical and maximum V_{DD} consumption in Stop and Standby modes

Symbol	Parameter	Conditions	Typ. @V_{DD} (V_{DD}=V_{DDA})						Max.(1)			Unit
			2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF	17.51	17.68	17.84	18.17	18.57	19.39	30.6	232.5	612.2	µA
		Regulator in low-power mode, all oscillators OFF	6.44	6.51	6.60	6.73	6.96	7.20	20.0	246.4	585.0	
	Supply current in Standby mode	LSI ON and IWDG ON	0.73	0.89	1.02	1.14	1.28	1.44	-	-	-	
		LSI OFF and IWDG OFF	0.55	0.66	0.75	0.85	0.93	1.01	4.9	7.0	7.9	

1. Data based on characterization results, not tested in production unless otherwise specified.

Table 28. Typical and maximum V_{DDA} consumption in Stop and Standby modes

Symbol	Parameter	Conditions		Typ. @V_{DD} (V_{DD} = V_{DDA})						Max.(1)			Unit
				2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DDA}	Supply current in Stop mode	V_{DDA} supervisor ON	Regulator in run/low-power mode, all oscillators OFF	1.67	1.79	1.91	2.04	2.19	2.35	2.5	5.9	6.2	µA
	Supply current in Standby mode		LSI ON and IWDG ON	2.06	2.24	2.41	2.60	2.80	3.04	-	-	-	
			LSI OFF and IWDG OFF	1.54	1.68	1.78	1.92	2.06	2.22	2.6	3.0	3.8	
	Supply current in Stop mode	V_{DDA} supervisor OFF	Regulator in run/low-power mode, all oscillators OFF	0.97	0.99	1.03	1.07	1.14	1.22	-	-	-	
	Supply current in Standby mode		LSI ON and IWDG ON	1.36	1.44	1.52	1.62	1.76	1.91	-	-	-	
			LSI OFF and IWDG OFF	0.86	0.88	0.91	0.95	1.03	1.09	-	-	-	

1. Data based on characterization results, not tested in production.

Table 29. Typical and maximum current consumption from V_{BAT} supply

Symbol	Parameter	Conditions(1)	Typ.@V_{BAT}								Max. @V_{BAT}= 3.6V(2)			Unit
			1.65 V	1.8V	2V	2.4V	2.7V	3V	3.3V	3.6V	T_A= 25°C	T_A= 85°C	T_A= 105°C	
I_{DD_VBAT}	Backup domain supply current	LSE & RTC ON; “Xtal mode” lower driving capability; LSEDRV[1:0] = '00'	0.42	0.44	0.47	0.54	0.60	0.66	0.74	0.82	-	-	-	µA
		LSE & RTC ON; “Xtal mode” higher driving capability; LSEDRV[1:0] = '11'	0.71	0.74	0.77	0.85	0.91	0.98	1.06	1.16	-	-	-	

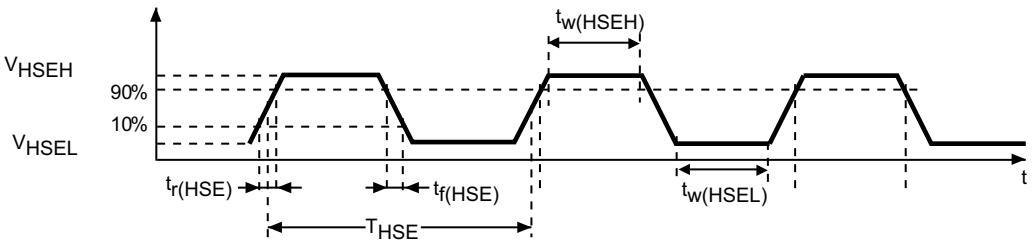
1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values.
2. Data based on characterization results, not tested in production.

Table 36. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSE_ext}	User external clock source frequency(1)	-	1	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time(1)		15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	

1. Guaranteed by design, not tested in production.

Figure 13. High-speed external clock source AC timing diagram



MS19214V2

Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 14*

Table 37. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	

1. Guaranteed by design, not tested in production.

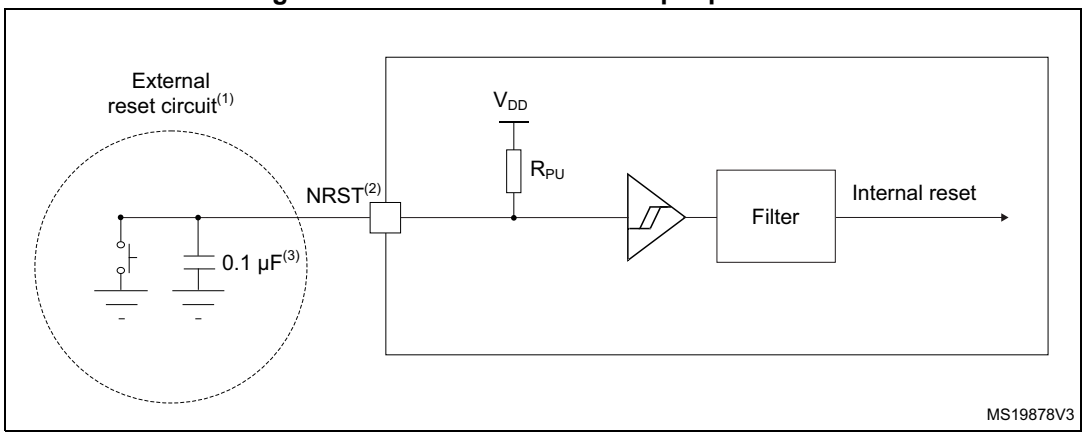
Table 39. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions[1]	Min.[2]	Typ.	Max.[2]	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	0.9	µA
		LSEDRV[1:0]=10 medium low driving capability	-	-	1	
		LSEDRV[1:0]=01 medium high driving capability	-	-	1.3	
		LSEDRV[1:0]=11 higher driving capability	-	-	1.6	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5	-	-	µA/V
		LSEDRV[1:0]=10 medium low driving capability	8	-	-	
		LSEDRV[1:0]=01 medium high driving capability	15	-	-	
		LSEDRV[1:0]=11 higher driving capability	25	-	-	
$t_{SU(LSE)}$[3]	Startup time	V_{DD} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 23. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 53*. Otherwise the reset will not be taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.
4. Place the external capacitor 0.1u F on NRST as close as possible to the chip.

6.3.16 High-resolution timer (HRTIM)

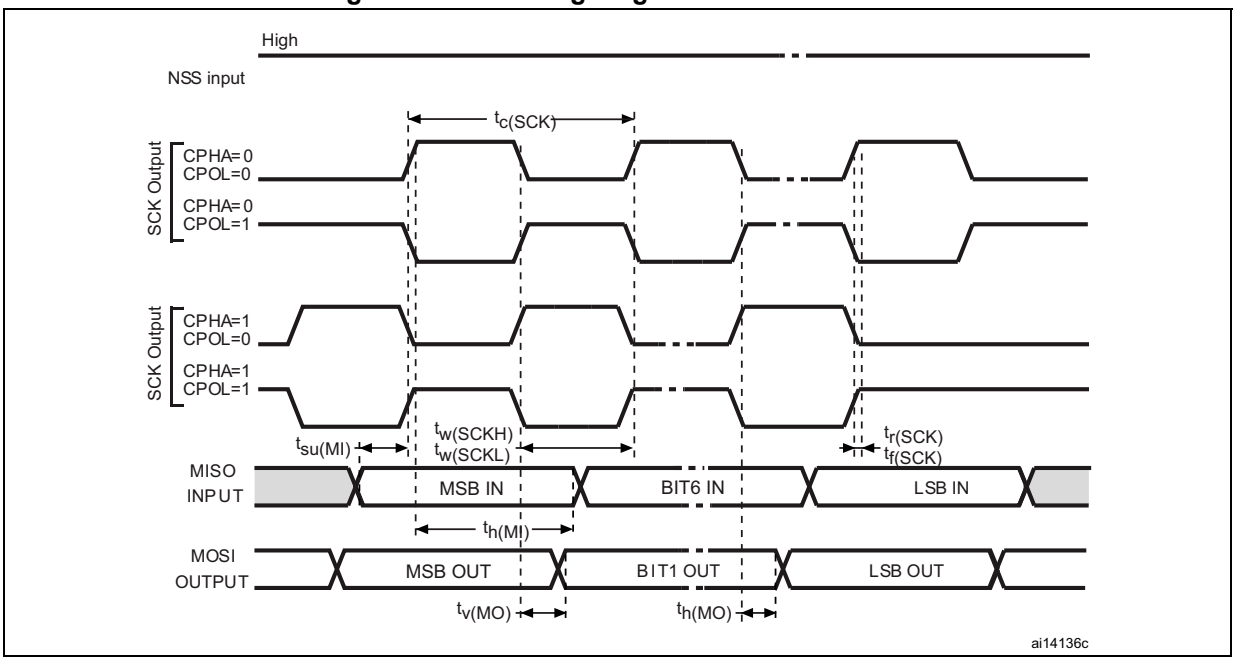
The parameters given in *Table 54* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19*.

Table 54. HRTIM1 characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_A	Timer ambient temperature range	f_{HRTIM}=144MHz (1)	-40	-	105	°C
		f_{HRTIM}=128MHz (2)	-10	-	105	°C
f_{HRTIM}	HRTIM input clock for DLL calibration	As per T_A conditions	128	-	144	MHz
t_{HRTIM}			6.9	-	7.8	ns
$t_{RES(HRTIM)}$	Timer resolution time	f_{HRTIM}=144MHz (1), TA from -40 to 105°C	-	217	-	ps
		f_{HRTIM}=128MHz (2),TA from -10 to 105°C	-	244	-	ps
Res_{HRTIM}	Timer resolution	-	-	-	16	bit
t_{DTG}	Dead time generator clock period	-	0.125	-	16	t_{HRTIM}
		f_{HRTIM}=144MHz (1)	0.868	-	111.10	ns
$\|t_{DTR}\| / \|t_{DTF}\|$ max	Dead time range (absolute value)	-	-	-	511	t_{DTG}
		f_{HRTIM}=144MHz (1)	-	-	56.77	µs
f_{CHPFRQ}	Chopper stage clock frequency	-	1/256	-	1/16	f_{HRTIM}
		f_{HRTIM}=144MHz (1)	0.562	-	9	MHz
t_{1STPW}	Chopper first pulse length	-	16	-	256	t_{HRTIM}
		f_{HRTIM}=144MHz (1)	0.111	-	1.77	µs

1. Using HSE with 8MHz XTAL as clock source, configuring PLL to get PLLCLK=144MHz, and selecting PLLCLKx2 as HRTIM clock source. (Refer to Reset and clock control section in RM0364.)
2. Using HSI (internal 8MHz RC oscillator), configuring PLL to get PLLCLK=128MHz, and selecting PLLCLKx2 as HRTIM clock source. (Refer to Reset and clock control section in RM0364.

Figure 26. SPI timing diagram - master mode(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

6.3.19 ADC characteristics

Unless otherwise specified, the parameters given in *Table 64* to *Table 67* are guaranteed by design, with conditions summarized in *Table 19*.

Table 64. ADC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage for ADC	-	2	-	3.6	V
I_{DDA}	ADC current consumption (*Figure 27*)	Single ended mode, 5 MSPS,	-	1011.3	1172.0	µA
		Single ended mode, 1 MSPS	-	214.7	322.3	
		Single ended mode, 200 KSPS	-	54.7	81.1	
		Differential mode,5 MSPS,	-	1061.5	1243.6	
		Differential mode, 1 MSPS	-	246.6	337.6	
		Differential mode, 200 KSPS	-	56.4	83.0	

6.3.23 Temperature sensor (TS) characteristics

Table 72. Temperature sensor (TS) characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(1)	Startup time	4	-	10	µs
T_{S_temp}(1)(2)	ADC sampling time when reading the temperature	2.2	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

Table 73. Temperature sensor (TS) calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

6.3.24 V_{BAT} monitoring characteristics

Table 74. V_{BAT} monitoring characteristics

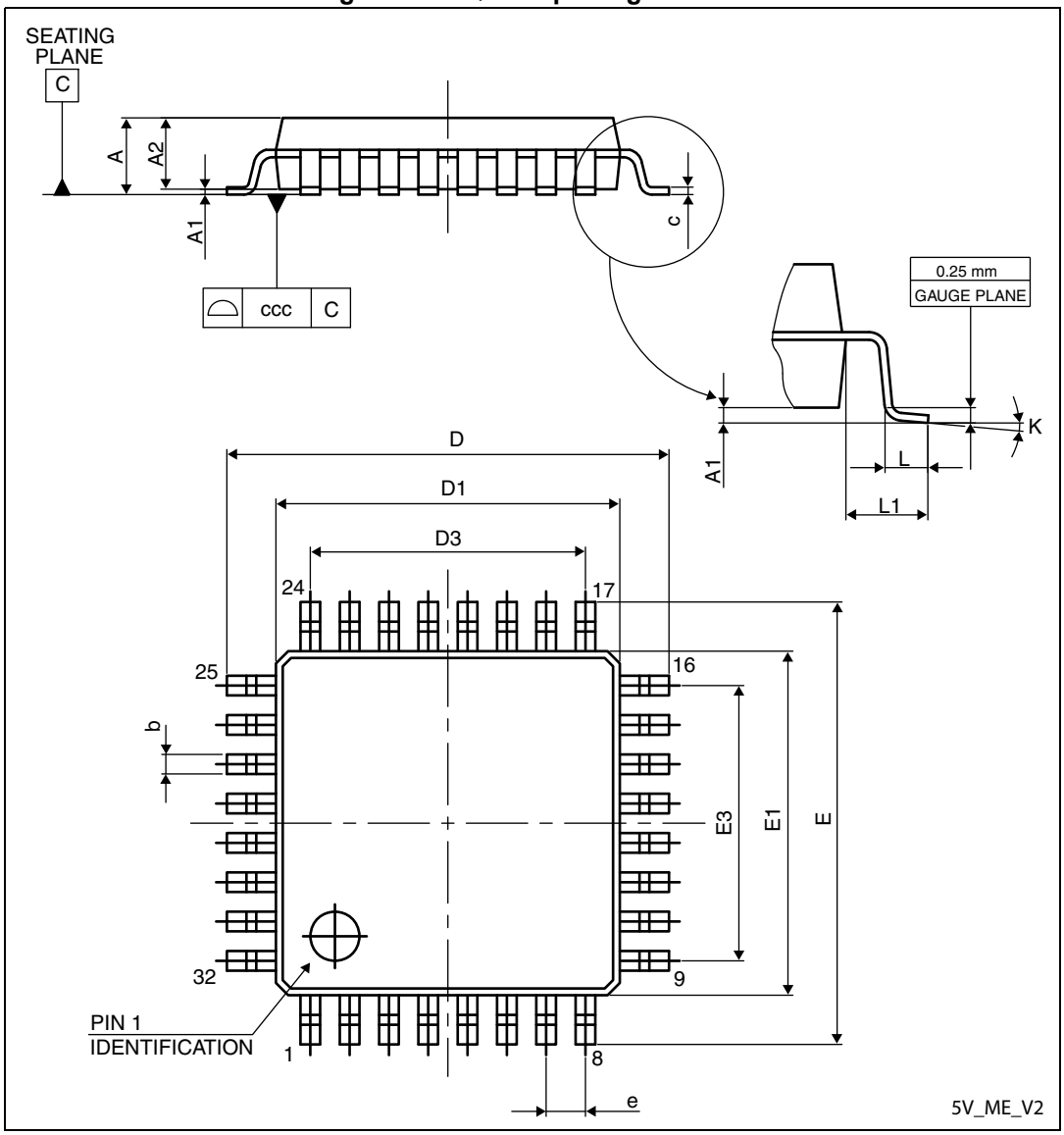
Symbol	Parameter	Min.	Typ.	Max.	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	-
Er(1)	Error on Q	-1	-	+1	%
T_{S_vbat}(1)(2)	ADC sampling time when reading the V_{BAT} 1mV accuracy	2.2	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

7.2 LQFP32 package information

LQFP32 is a 32-pin, 7 x 7mm low-profile quad flat package.

Figure 33. LQFP32 package outline



1. Drawing is not to scale.

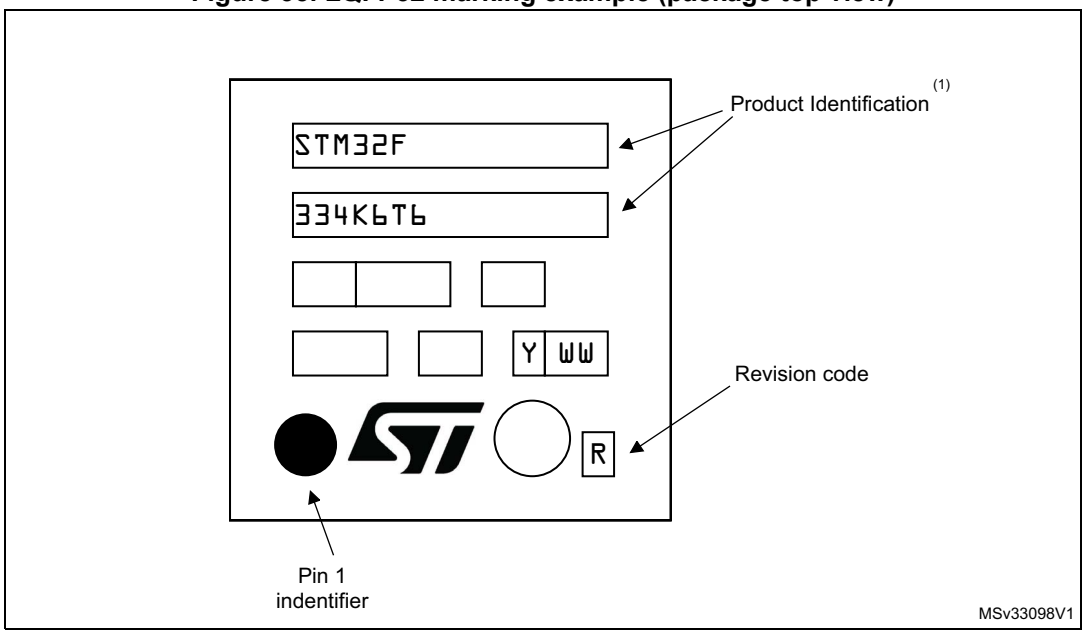
Table 75. LQFP32 mechanical data

Symbol	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571

Device marking for LQFP32

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 35. LQFP32 marking example (package top view)



1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.