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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 21x12b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f334r8t7tr

2 Description

The STM32F334x4/6/8 family incorporates the high-performance ARM® Cortex®-M4 32-bit RISC core operating at up to 72 MHz frequency embedding a floating point unit (FPU), high-speed embedded memories (up to 64 Kbytes of Flash memory, up to 12 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The STM32F334x4/6/8 microcontrollers offer two fast 12-bit ADCs (5 Msps), up to three ultra-fast comparators, an operational amplifier, three DAC channels, a low-power RTC, one high-resolution timer, one general-purpose 32-bit timer, one timer dedicated to motor control, and four general-purpose 16-bit timers. They also feature standard and advanced communication interfaces: one I^2C, one SPI, up to three USARTs and one CAN.

The STM32F334x4/6/8 family operates in the –40 to +85 °C and –40 to +105 °C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F334x4/6/8 family offers devices in 32, 48 and 64-pin packages.

Depending on the device chosen, different sets of peripherals are included.

Table 2. STM32F334x4/6/8 family device features and peripheral counts

Peripheral		STM32F334Kx			STM32F334Cx			STM32F334Rx		
Flash memory (Kbyte)		16	32	64	16	32	64	16	32	64
SRAM on data bus (Kbyte)		12								
Core coupled memory SRAM on instruction bus (CCM SRAM) (Kbyte)		4								
Timers	High-resolution timer	1 (16-bit / 10 channels)								
	Advanced control	1 (16-bit)								
	General purpose	4 (16-bit) 1 (32 bit)								
	Basic	2 (16-bit)								
	SysTick timer	1								
	Watchdog timers (independent, window)	2								
	PWM channels (all)(1)	20			26			28		
	PWM channels (except complementary)	14			20			22		

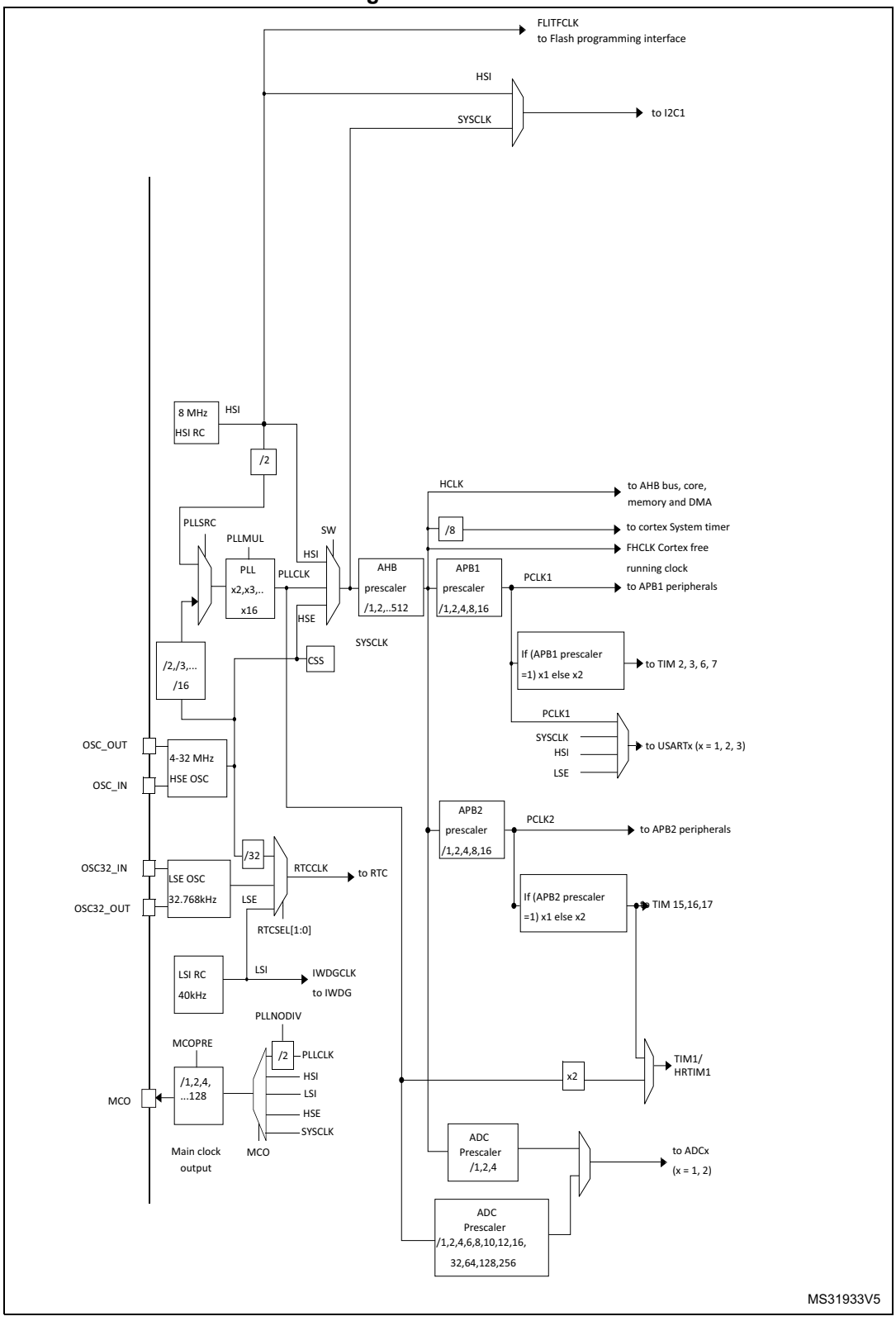
3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

TIM1and HRTIM1 maximum frequency is 144 MHz.

Figure 2. Clock tree



independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 51 GPIOs can be connected to the 16 external interrupt lines.

3.10 Fast analog-to-digital converter (ADC)

Two 5 MSPS fast analog-to-digital converters, with selectable resolution between 12 and 6 bit, are embedded in the STM32F334x4/6/8 family devices. The ADCs have up to 21 external channels. Some of the external channels are shared between ADC1 and ADC2, performing conversions in single-shot or scan modes. The channels can be configured to be either single-ended input or differential input. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADCs also have internal channels: temperature sensor connected to ADC1 channel 16, $V_{BAT}/2$ connected to ADC1 channel 17, voltage reference V_{REFINT} connected to both ADC1 and ADC2 channel 18 and VOPAMP2 connected to ADC2 channel 17.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single-shunt phase current reading techniques.

Three analog watchdogs are available per ADC. The ADC can be served by the DMA controller.

The analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIM2, TIM3, TIM6, TIM15), the advanced-control timer (TIM1) and the High-resolution timer (HRTIM1) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

3.10.2 Internal voltage reference (VREFINT)

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC and Comparators. VREFINT is internally connected to the ADC1_IN18 and ADC2_IN18

3.13 Ultra-fast comparators (COMP)

The STM32F334x4/6/8 devices embed three ultra-fast rail-to-rail comparators (COMP2/4/6) which offer the features below:

- Programmable internal or external reference voltage
- Selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to *Table 23: Embedded internal reference voltage* for values and parameters of the internal reference voltage.

All comparators can wake up from STOP mode, generate interrupts and breaks for the timers.

3.14 Timers and watchdogs

The STM32F334x4/6/8 includes advanced control timer, 5 general-purpose timers, basic timer, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare Channels	Complementary outputs
High-resolution timer	HRTIM1(1)	16-bit	Up	/1 /2 /4 (x2 x4 x8 x16 x32, with DLL)	Yes	10	Yes
Advanced control	TIM1(1)	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	Yes
General-purpose	TIM2	32-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

1. TIM1 can be clocked from the PLL x 2 running at 144 MHz .

Table 9. STM32F334x4/6/8 SPI implementation (continued)

SPI features(1)	SPI1
NSS pulse mode	X
TI mode	X

1. X = supported.

3.16.4 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

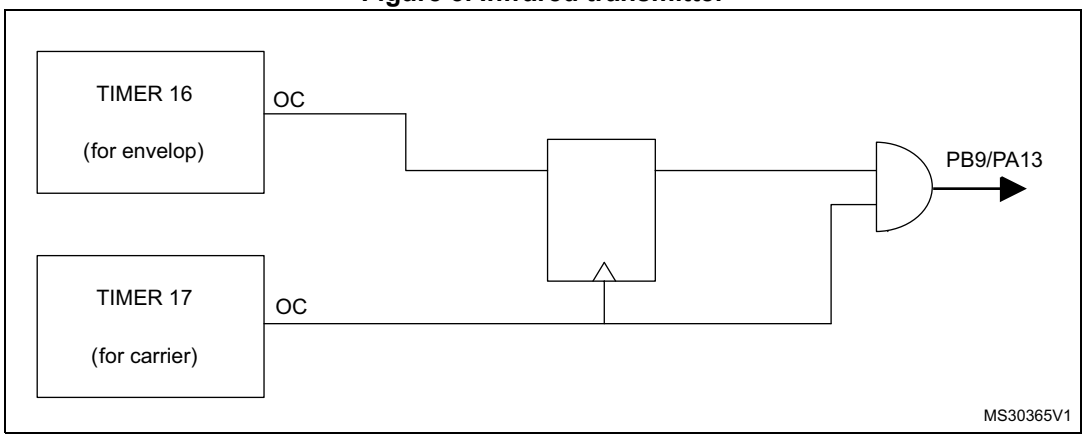
3.17 Infrared transmitter

The STM32F334x4/6/8 devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

Figure 3. Infrared transmitter



3.18 Touch sensing controller (TSC)

The STM32F334x4/6/8 devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 18 capacitive sensing channels distributed over 6 analog I/Os group.

Capacitive sensing technology is able to detect the presence of a finger near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of

3.19 Development support

3.19.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Table 13. STM32F334x4/6/8 pin definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Pin functions	
LQFP 32	LQFP 48	LQFP 64				Alternate functions	Additional functions
23	34	46	PA13	I/O	FT	JTMS/SWDAT, TIM16_CH1N, TSC_G4_IO3, IR_OUT, USART3_CTS, EVENTOUT	-
-	35	47	VSS	S	-	-	-
-	36	48	VDD	S	-	-	-
24	37	49	PA14	I/O	FTf	JTCK/SWCLK, TSC_G4_IO4, I2C1_SDA, TIM1_BKIN, USART2_TX, EVENTOUT	-
25	38	50	PA15	I/O	FTf	JTDI, TIM2_CH1/TIM2_ETR, TSC_SYNC, I2C1_SCL, SPI1_NSS, USART2_RX, TIM1_BKIN, HRTIM1_FLT2, EVENTOUT	-
-	-	51	PC10	I/O	FT	EVENTOUT, USART3_TX	-
-	-	52	PC11	I/O	FT	EVENTOUT, HRTIM1_EEV2, USART3_RX	-
-	-	53	PC12	I/O	FT	EVENTOUT, HRTIM1_EEV1, USART3_CK	-
-	-	54	PD2	I/O	FT	EVENTOUT, TIM3_ETR	-
26	39	55	PB3	I/O	FT	JTDO/TRACE SWO, TIM2_CH2, TSC_G5_IO1, SPI1_SCK, USART2_TX, TIM3_ETR, HRTIM1_SCOUT, HRTIM1_EEV9, EVENTOUT	-
27	40	56	PB4	I/O	FT	NJTRST, TIM16_CH1, TIM3_CH1, TSC_G5_IO2, SPI1_MISO, USART2_RX, TIM17_BKIN, HRTIM1_EEV7, EVENTOUT	-

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 16: Voltage characteristics*, *Table 17: Current characteristics*, and *Table 18: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 16. Voltage characteristics(1)

Symbol	Ratings	Min.	Max.	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{BAT} and V_{DD})	-0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	
V_{IN}(2)	Input voltage on FT and FTf pins	V_{SS} −0.3	V_{DD} + 4.0	
	Input voltage on TTa and TT pins	V_{SS} −0.3	4.0	
	Input voltage on any other pin	V_{SS} −0.3	4.0	
	Input voltage on Boot0 pin	0	9	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins(3)	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12: Electrical sensitivity characteristics*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range. The following relationship must be respected between V_{DDA} and V_{DD}:
V_{DDA} must power on before or at the same time as V_{DD} in the power up sequence.
V_{DDA} must be greater than or equal to V_{DD}.
2. V_{IN} maximum must always be respected. Refer to *Table 17: Current characteristics* for the maximum allowed injected current values.
3. Include V_{REF-} pin.

Table 17. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD_x power lines (source)(1)	140	mA
ΣI_{VSS}	Total current out of sum of all VSS_x ground lines (sink)(1)	-140	
I_{VDD}	Maximum current into each V_{DD_x} power line (source)(1)	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	80	
	Total output current sourced by sum of all I/Os and control pins(2)	-80	
$I_{INJ(PIN)}$	Injected current on TT, FT, FTf and B pins(3)	-5 /+0	
	Injected current on TC and RST pin(4)	±5	
	Injected current on TTa pins(5)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS} and V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins.The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 16: Voltage characteristics* for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. I_{INJ}(PIN) must never be exceeded. Refer also to *Table 16: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note 2. below *Table 64*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 18. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

Table 25. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6V

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ.	Max. @ T_A(1)			Typ.	Max. @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, executing from Flash	External clock (HSE bypass)	72 MHz	71.4	77.9	79.1	80.0	27.1	32.2	32.4	32.4	mA
			64 MHz	63.9	70.6	71.3	71.5	24.2	27.0	27.5	27.7	
			48 MHz	49.5	56.6	57.1	57.7	18.7	21.4	21.6	21.9	
			32 MHz	34.0	38.6	38.9	39.2	12.9	14.6	14.9	15.9	
			24 MHz	25.9	30.2	30.4	30.6	10.0	11.1	11.2	12.3	
			8 MHz	9.3	14.1	14.3	14.4	3.3	4.0	4.4	5.1	
			1 MHz	3.5	8.9	9.1	9.5	0.7	0.9	1.0	1.2	
		Internal clock (HSI)	64 MHz	61.6	68.1	68.8	70.1	24.1	27.0	27.1	27.2	
			48 MHz	48.1	54.6	54.8	55.1	18.6	21.6	21.7	21.9	
			32 MHz	33.3	37.8	37.9	38.0	12.7	14.4	14.9	16.0	
			24 MHz	25.7	29.8	29.8	30.0	10.0	11.1	11.2	12.3	
			8 MHz	9.7	12.2	12.3	12.8	3.4	3.8	4.2	5.0	
	Supply current in Run mode, executing from RAM	External clock (HSE bypass)	72 MHz	71.3	77.8(2)	78.7	78.9(2)	27.6	32.1(2)	32.2	32.3(2)	
			64 MHz	63.8	70.5	70.7	70.9	24.5	27.2	27.6	27.7	
			48 MHz	49.3	56.5	56.9	57.4	18.1	21.6	21.8	21.8	
			32 MHz	33.9	37.7	37.9	38.0	12.9	14.9	14.9	15.9	
			24 MHz	25.8	28.8	29.0	29.2	9.8	11.1	11.3	11.5	
			8 MHz	9.0	13.2	13.3	13.8	3.2	3.6	4.0	4.6	
			1 MHz	3.2	7.6	7.8	8.0	0.3	0.4	0.8	1.2	
		Internal clock (HSI)	64 MHz	61.3	66.9	67.3	67.8	24.1	26.9	27.0	27.1	
			48 MHz	48.0	52.4	52.6	53.1	19.1	21.6	21.6	22.1	
			32 MHz	33.1	35.6	35.8	36.6	12.6	14.8	14.9	15.9	
			24 MHz	25.6	28.5	28.7	28.8	9.8	11.1	11.3	11.5	
			8 MHz	9.7	11.6	11.6	11.7	3.0	3.1	4.1	4.7	
I_{DD}	Supply current in Sleep mode, executing from Flash or RAM	External clock (HSE bypass)	72 MHz	55.5	58.7(2)	61.1	61.9(2)	7.0	7.3(2)	8.4	8.5(2)	mA
			64 MHz	49.8	52.7	54.5	54.8	6.3	6.7	7.0	7.8	
			48 MHz	38.5	40.6	41.7	41.8	4.6	5.1	5.6	5.9	
			32 MHz	26.9	28.8	29.2	29.5	3.0	3.3	4.0	4.5	
			24 MHz	19.1	23.2	23.7	23.9	2.4	2.5	3.2	3.8	
			8 MHz	7.1	11.5	11.7	11.9	0.6	0.9	1.2	2.1	
			1 MHz	3.0	7.4	7.7	7.9	0.3	0.3	0.4	1.2	
		Internal clock (HSI)	64 MHz	47.7	52.4	52.6	52.8	5.4	6.5	6.8	7.5	
			48 MHz	35.0	40.4	40.6	40.8	4.3	4.7	5.2	5.7	
			32 MHz	23.7	27.7	28.3	28.8	2.9	3.1	3.2	4.4	
			24 MHz	18.5	23.8	24.0	24.2	1.3	1.7	2.2	2.7	
			8 MHz	7.5	9.6	9.7	9.7	0.5	0.7	1.1	2.0	

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production with code executing from RAM.

Table 28. Typical and maximum V_{DDA} consumption in Stop and Standby modes

Symbol	Parameter	Conditions		Typ. @V_{DD} (V_{DD} = V_{DDA})						Max.(1)			Unit
				2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DDA}	Supply current in Stop mode	V_{DDA} supervisor ON	Regulator in run/low-power mode, all oscillators OFF	1.67	1.79	1.91	2.04	2.19	2.35	2.5	5.9	6.2	µA
	Supply current in Standby mode		LSI ON and IWDG ON	2.06	2.24	2.41	2.60	2.80	3.04	-	-	-	
			LSI OFF and IWDG OFF	1.54	1.68	1.78	1.92	2.06	2.22	2.6	3.0	3.8	
	Supply current in Stop mode	V_{DDA} supervisor OFF	Regulator in run/low-power mode, all oscillators OFF	0.97	0.99	1.03	1.07	1.14	1.22	-	-	-	
	Supply current in Standby mode		LSI ON and IWDG ON	1.36	1.44	1.52	1.62	1.76	1.91	-	-	-	
			LSI OFF and IWDG OFF	0.86	0.88	0.91	0.95	1.03	1.09	-	-	-	

1. Data based on characterization results, not tested in production.

Table 29. Typical and maximum current consumption from V_{BAT} supply

Symbol	Parameter	Conditions(1)	Typ.@V_{BAT}								Max. @V_{BAT}= 3.6V(2)			Unit
			1.65 V	1.8V	2V	2.4V	2.7V	3V	3.3V	3.6V	T_A= 25°C	T_A= 85°C	T_A= 105°C	
I_{DD_VBAT}	Backup domain supply current	LSE & RTC ON; “Xtal mode” lower driving capability; LSEDRV[1:0] = '00'	0.42	0.44	0.47	0.54	0.60	0.66	0.74	0.82	-	-	-	µA
		LSE & RTC ON; “Xtal mode” higher driving capability; LSEDRV[1:0] = '11'	0.71	0.74	0.77	0.85	0.91	0.98	1.06	1.16	-	-	-	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values.
2. Data based on characterization results, not tested in production.

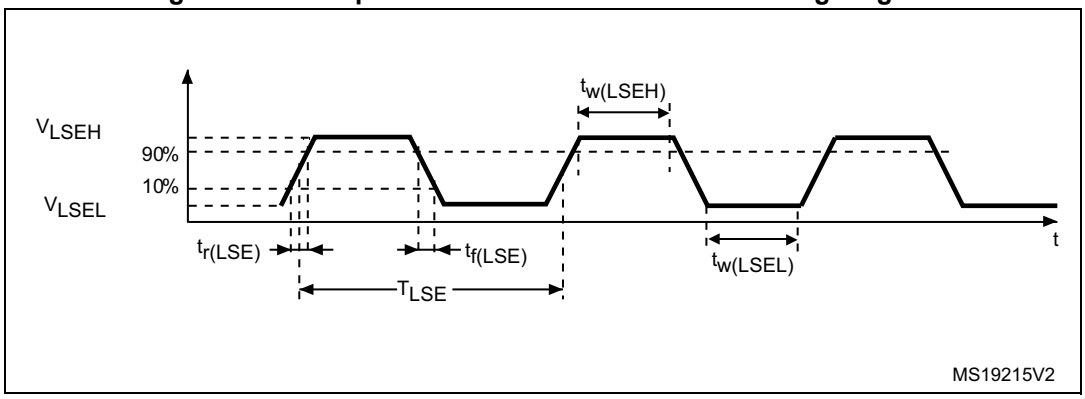
The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 32. Switching output I/O current consumption

Symbol	Parameter	Conditions(1)	I/O toggling frequency (f_{SW})	Typ.	Unit
I_{SW}	I/O current consumption	V_{DD} = 3.3 V C_{ext} = 0 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.90	mA
			4 MHz	0.93	
			8 MHz	1.16	
			18 MHz	1.60	
			36 MHz	2.51	
		V_{DD} = 3.3 V C_{ext} = 10 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.93	
			4 MHz	1.06	
			8 MHz	1.47	
			18 MHz	2.26	
			36 MHz	3.39	
		V_{DD} = 3.3 V C_{ext} = 22 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.03	
			4 MHz	1.30	
			8 MHz	1.79	
			18 MHz	3.01	
			36 MHz	5.99	
		V_{DD} = 3.3 V C_{ext} = 33 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.10	
			4 MHz	1.31	
			8 MHz	2.06	
			18 MHz	3.47	
			36 MHz	8.35	
		V_{DD} = 3.3 V C_{ext} = 47 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.20	
			4 MHz	1.54	
			8 MHz	2.46	
			18 MHz	4.51	
			36 MHz	9.98	

1. CS = 5 pF (estimated value).

Figure 14. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

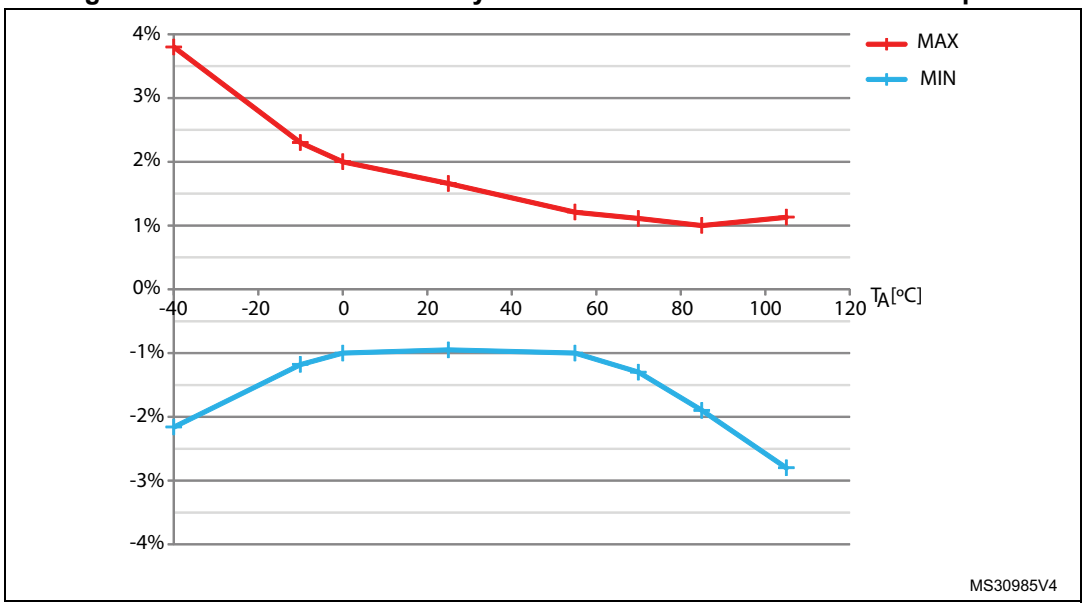
The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 38*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 38. HSE oscillator characteristics

Symbol	Parameter	Conditions(1)	Min.(2)	Typ.	Max.(2)	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
I_{DD}	HSE current consumption	During startup(3)	-	-	8.5	mA
		V_{DD}= 3.3 V, Rm= 30Ω, CL=10 pF@8 MHz	-	0.4	-	
		V_{DD}= 3.3 V, Rm= 45Ω, CL=10 pF@8 MHz	-	0.5	-	
		V_{DD}= 3.3 V, Rm= 30Ω, CL=5 pF@32 MHz	-	0.8	-	
		V_{DD}= 3.3 V, Rm= 30Ω, CL=10 pF@32 MHz	-	1	-	
		V_{DD}= 3.3 V, Rm= 30Ω, CL=20 pF@32 MHz	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 17. HSI oscillator accuracy characterization results for soldered parts



Low-speed internal (LSI) RC oscillator

Table 41. LSI oscillator characteristics(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in *Table 42* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19*.

Table 42. PLL characteristics

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
f_{PLL_IN}	PLL input clock(1)	1(2)	-	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	72	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
Jitter	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design, not tested in production.

Figure 19. TC and TTa I/O input characteristics - TTL port

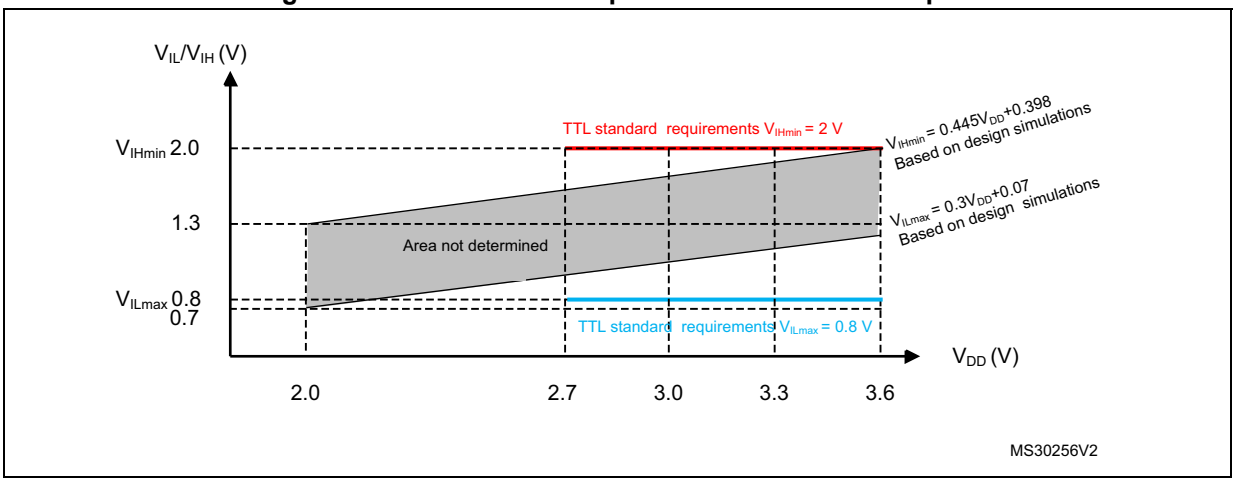


Figure 20. Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port

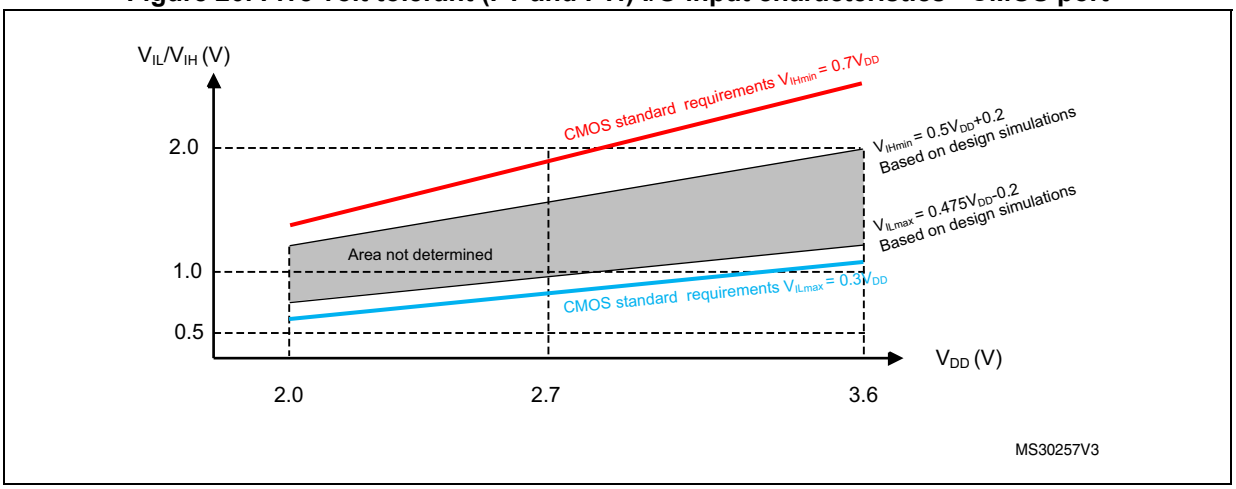


Figure 21. Five volt tolerant (FT and FTf) I/O input characteristics - TTL port

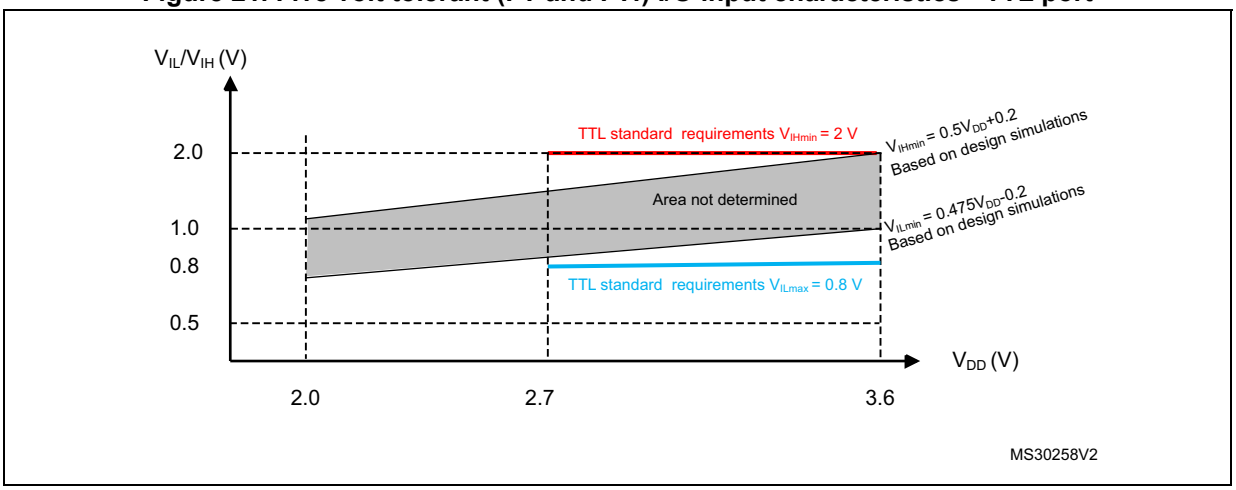


Table 57. HRTIM output response to external events 1 to 10 (Synchronous mode [1])

Symbol	Parameter	Conditions	Min.	Typ.	Max. (2)	Unit
$T_{PROP(HRTIM)}$	External event response latency in HRTIM	HRTIM internal propagation delay [3]	6	-	7	t_{HRTIM}
$t_{LAT(DEEV)}$	Digital external event response latency	Propagation delay from HRTIM1_EEVx digital input to HRTIM_CHxy output pin (30pF load) [4]	-	61	72	ns
$t_{LAT(AEEV)}$	Analog external event response latency	Propagation delay from COMPx_INP input pin to HRTIM_CHxy output pin (30pF load) [4]	-	81	94	ns
$t_{W(FLT)}$	Minimum external event pulse width	-	12.5	-	-	ns
$T_{JIT(EEV)}$	External event response jitter	Jitter of the delay from HRTIM1_EEVx digital input or COMPx_INP to HRTIM_CHxy output pin	-	-	1	t_{HRTIM} (5)
$T_{JIT(PW)}$	Jitter on output pulse width in response to an external event	-	-	-	0	t_{HRTIM} (5)

1. EExFAST bit in HRTIM_EECR1 or HRTIM_EECR2 register is cleared (synchronous mode). External event filtering is disabled, i.e. EExF[3:0]=0000 in HRTIM_EECR2 register. Refer to Latency to external events paragraph in HRTIM section of RM0364.
2. Data based on characterization results, not tested in production.
3. This parameter does not take into account latency introduced by GPIO or comparator. Refer to DEERL or SACRL parameter for complete latency.
4. This parameter is given for f_{HRTIM} = 144 MHz.
5. T_{HRTIM} = 1 / f_{HRTIM} with f_{HRTIM}= 144 MHz or f_{HRTIM} = 128 MHZ depending on the clock controller configuration. (Refer to Reset and clock control section in RM0364.)

Table 58. HRTIM synchronization input / output[1]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{W(SYNCIN)}$	Minimum pulse width on SYNCIN inputs, including HRTIM1_SCIN	-	2	-	-	t_{HRTIM}
$t_{LAT(DF)}$	Response time to external synchronization request	-	-	-	1	t_{HRTIM}
$t_{LAT(AF)}$	Pulse width on HRTIM1_SCOUT output	-	-	16	-	t_{HRTIM}
		f_{HRTIM}=144 MHz	-	111.1	-	ns

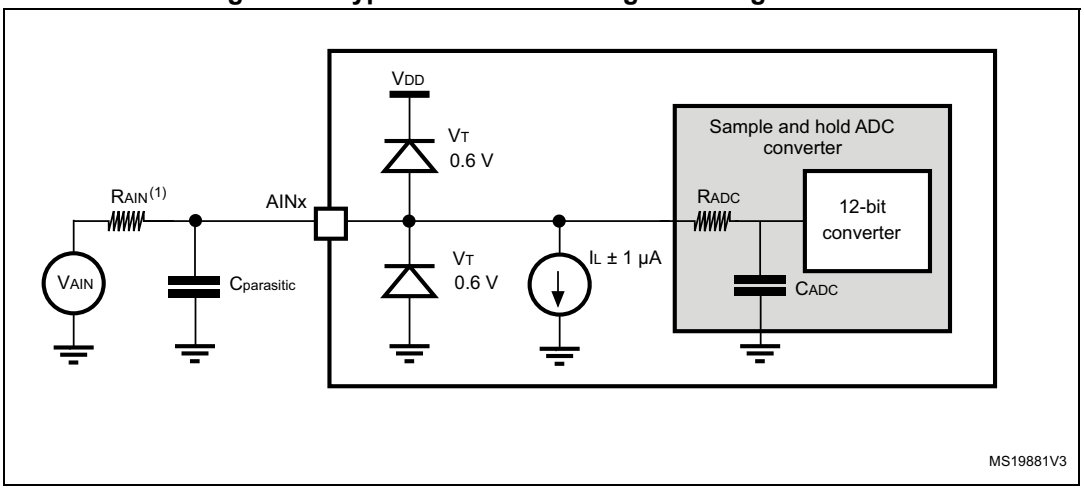
1. Guaranteed by design, not tested in production.

Table 67. ADC accuracy (1)(2)(3) (continued)

Symbol	Parameter	Conditions			Min(4)	Max (4)	Unit
EL	Integral linearity error	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps 2.0 V ≤ V_{DDA} ≤ 3.6 V	Single ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3.5	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2.5	
ENOB (5)	Effective number of bits		Single ended	Fast channel 5.1 Ms	10.4	-	bits
				Slow channel 4.8 Ms	10.4	-	
			Differential	Fast channel 5.1 Ms	10.8	-	
				Slow channel 4.8 Ms	10.8	-	
SINAD (5)	Signal-to-noise and distortion ratio		Single ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	63	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
SNR(5)	Signal-to-noise ratio	ADC clock freq. ≤ 72 MHz, Sampling freq ≤ 5 Msps, 2.0 V ≤ V_{DDA} ≤ 3.6 V	Single ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	64	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
THD(5)	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-75	
				Slow channel 4.8 Ms	-	-75	
			Differential	Fast channel 5.1 Ms	-	-79	
				Slow channel 4.8 Ms	-	-78	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.
5. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Figure 29. Typical connection diagram using the ADC



1. Refer to *Table 64* for the values of R_{AIN}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 10: Power-supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.20 DAC electrical specifications

Table 69. DAC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage	-	2.4	-	3.6	V
R_{LOAD}(1)	Resistive load	DAC output buffer ON (to V_{SSA})	5	-	-	kΩ
R_{LOAD}(1)	Resistive load	DAC output buffer ON (to V_{DDA})	25	-	-	kΩ
R_O(1)	Output impedance	DAC output buffer OFF	-	-	15	kΩ
C_{LOAD}(1)	Capacitive load	DAC output buffer ON	-	-	50	pF
V_{DAC_OUT}(1)	Voltage on DAC_OUT output	Corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{DDA} = 3.6 V and (0x155) and (0xEAB) at V_{DDA} = 2.4 V	0.2	-	V_{DDA} – 0.2	V
		DAC output buffer OFF	-	0.5	-	mV
			-	-	V_{DDA}– 1LSB	V
I_{DDA}(3)	DAC DC current consumption in quiescent mode(2)	With no load, middle code (0x800) on the input	-	-	380	µA
		With no load, worst code (0xF1C) on the input.	-	-	480	µA

Table 71. Operational amplifier characteristics(1) (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
en	Voltage noise density	@ 1KHz, Output loaded with 4 KΩ	-	109	-	$\frac{nV}{\sqrt{Hz}}$
		@ 10KHz, Output loaded with 4 KΩ	-	43	-	

1. Guaranteed by design, not tested in production.
2. The saturation voltage can also be limited by the I_{load}.
3. R2 is the internal resistance between OPAMP output and OPAMP inverting input.
   R1 is the internal resistance between OPAMP inverting input and ground.
   The PGA gain =1+R2/R1
4. Mostly TTa I/O leakage, when used in analog mode.

Figure 32. OPAMP Voltage Noise versus Frequency