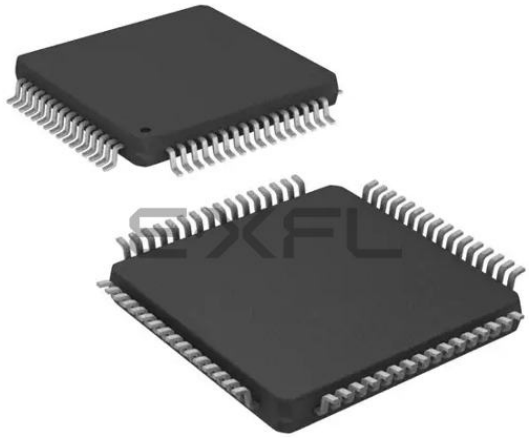

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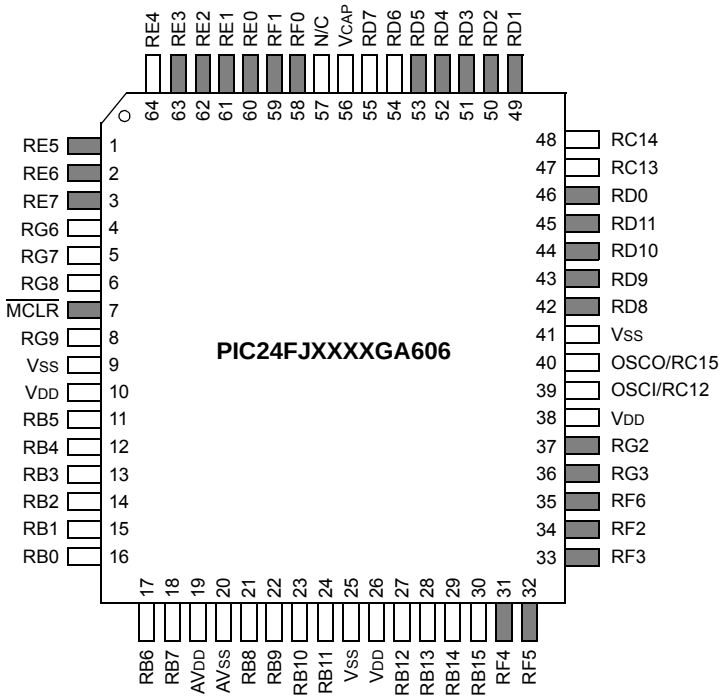
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, HLVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	1MB (341.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj1024ga606-i-pt

Pin Diagrams(2)

64-Pin TQFP
64-Pin QFN(1)



Legend: See Table 2 for a complete description of pin functions. Pinouts are subject to change.
Note 1: It is recommended to connect the metal pad on the bottom of the 64-pin QFN package to VSS.
2: Gray shading indicates 5.5V tolerant input pins.

TABLE 4: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJXXXGA610 TQFP)

Pin	Function	Pin	Function
1	OCM1C/CTED3/RG15	51	**RP16**/RF3
2	VDD	52	**RP30**/RF2
3	IC4/CTED4/PMD5/RE5	53	**RP15**/RF8
4	SCL3/IC5/PMD6/RE6	54	RF7
5	SDA3/IC6/PMD7/RE7	55	INT0/RF6
6	**RPI38**/OCM1D/RC1	56	SDA1/RG3
7	**RPI39**/OCM2C/RC2	57	SCL1/RG2
8	**RPI40**/OCM2D/RC3	58	PMPCS1/SCL2/RA2
9	AN16/**RPI41**/OCM3C/PMCS2/RC4	59	SDA2/PMA20/RA3
10	AN17/C1IND/**RP21**/ICM1/OCM1A/PMA5/RG6	60	TDI/PMA21/RA4
11	AN18/C1INC/**RP26**/OCM1B/PMA4/RG7	61	TDO/RA5
12	AN19/C2IND/**RP19**/ICM2/OCM2A/PMA3/RG8	62	VDD
13	$\overline{\text{MCLR}}$	63	OSCI/CLKI/RC12
14	AN20/C1INC/C2INC/C3INC/**RP27**/OCM2B/PMA2/PMALU/RG9	64	OSCO/CLKO/RC15
15	VSS	65	VSS
16	VDD	66	**RPI36**/PMA22/RA14
17	TMS/OCM3D/RA0	67	**RPI35**/PMBE1/RA15
18	**RPI33**/PMCS1/RE8	68	CLC4OUT/**RP2**/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/RD8
19	AN21/**RPI34**/PMA19/RE9	69	**RP4**/PMACK2/RD9
20	PGEC3/AN5/C1INA/**RP18**/ICM3/OCM3A/RB5	70	**RP3**/PMA15/PMCS2/RD10
21	PGED3/AN4/C1INB/**RP28**/OCM3B/RB4	71	**RP12**/PMA14/PMCS1/RD11
22	AN3/C2INA/RB3	72	CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/RD0
23	AN2/CTCMP/C2INB/**RP13**/CTED13/RB2	73	SOSCI/C3IND/RC13
24	PGEC1/ALTCVREF-/ALTVREF-/AN1/**RP1**/CTED12/RB1	74	SOSCO/C3INC/**RPI37**/PWRLCLK/RC14
25	PGED1/ALTCVREF+/ALTVREF+/AN0/**RP0**/RB0	75	VSS
26	PGEC2/AN6/**RP6**/RB6	76	**RP24**/U5TX/ICM4/RD1
27	PGED2/AN7/**RP7**/U6TX/RB7	77	**RP23**/PMACK1/RD2
28	CVREF-/VREF-/PMA7/RA9	78	**RP22**/ICM7/PMBE0/RD3
29	CVREF+/VREF+/PMA6/RA10	79	**RPI42**/OCM3E/PMD12/RD12
30	AVDD	80	OCM3F/PMD13/RD13
31	AVSS	81	**RP25**/PMWR/PMENB/RD4
32	AN8/**RP8**/PWRGT/RB8	82	**RP20**/PMRD/$\overline{\text{PMWR}}$/RD5
33	AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/RB9	83	C3INB/U5RX/OC4/PMD14/RD6
34	CVREF/AN10/PMA13/RB10	84	C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/PMD15/RD7
35	AN11/REFI/PMA12/RB11	85	VCAP
36	VSS	86	N/C
37	VDD	87	$\overline{\text{U5CTS}}$/OC6/PMD11/RF0
38	TCK/RA1	88	PMD10/RF1
39	**RP31**/RF13	89	PMD9/RG1
40	**RPI32**/CTED7/PMA18/RF12	90	PMD8/RG0
41	AN12/U6RX/CTED2/PMA11/RB12	91	AN23/OCM1E/RA6
42	AN13/CTED1/PMA10/RB13	92	AN22/OCM1F/PMA17/RA7
43	AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/RB14	93	PMD0/RE0
44	AN15/**RP29**/CTED6/PMA0/PMALL/RB15	94	PMD1/RE1
45	VSS	95	CTED11/PMA16/RG14
46	VDD	96	OCM2E/RG12
47	**RPI43**/RD14	97	OCM2F/CTED10/RG13
48	**RP5**/RD15	98	PMD2/RE2
49	**RP10**/PMA9/RF4	99	CTED9/PMD3/RE3
50	**RP17**/PMA8/RF5	100	HLVDIN/CTED8/PMD4/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.

1.2 DMA Controller

PIC24FJ1024GA610/GB610 family devices have a Direct Memory Access (DMA) Controller. This module acts in concert with the CPU, allowing data to move between data memory and peripherals without the intervention of the CPU, increasing data throughput and decreasing execution time overhead. Eight independently programmable channels make it possible to service multiple peripherals at virtually the same time, with each channel peripheral performing a different operation. Many types of data transfer operations are supported.

1.3 Other Special Features

- **Peripheral Pin Select:** The Peripheral Pin Select (PPS) feature allows most digital peripherals to be mapped over a fixed set of digital I/O pins. Users may independently map the input and/or output of any one of the many digital peripherals to any one of the I/O pins.
- **Configurable Logic Cell:** The Configurable Logic Cell (CLC) module allows the user to specify combinations of signals as inputs to a logic function and to use the logic output to control other peripherals or I/O pins.
- **Timing Modules:** The PIC24FJ1024GA610/GB610 family provides five independent, general purpose, 16-bit timers (four of which can be combined into two 32-bit timers). The devices also include 3 multiple output and 4 single output advanced Capture/Compare/PWM/Timer peripherals, and 6 independent legacy Input Capture and 6 independent legacy Output Compare modules.
- **Communications:** The PIC24FJ1024GA610/GB610 family incorporates a range of serial communication peripherals to handle a range of application requirements. There are 3 independent I^2C modules that support both Master and Slave modes of operation. Devices also have, through the PPS feature, 6 independent UARTs with built-in IrDA® encoders/decoders and 3 SPI modules.
- **Analog Features:** All members of the PIC24FJ1024GA610/GB610 family include the new 12-bit A/D Converter (A/D) module and a triple comparator module. The A/D module incorporates a range of new features that allow the converter to assess and make decisions on incoming data, reducing CPU overhead for routine A/D conversions. The comparator module includes three analog comparators that are configurable for a wide range of operations.
- **CTMU Interface:** In addition to their other analog features, members of the PIC24FJ1024GA610/GB610 family include the CTMU interface module. This provides a convenient method for precision time measurement and pulse generation, and can serve as an interface for capacitive sensors.
- **Enhanced Parallel Master/Parallel Slave Port:** This module allows rapid and transparent access to the microcontroller data bus, and enables the CPU to directly address external data memory. The parallel port can function in Master or Slave mode, accommodating data widths of 4, 8 or 16 bits and address widths of up to 23 bits in Master modes.
- **Real-Time Clock and Calendar (RTCC):** This module implements a full-featured clock and calendar with alarm functions in hardware, freeing up timer resources and program memory space for use of the core application.

1.4 Details on Individual Family Members

Devices in the PIC24FJ1024GA610/GB610 family are available in 64-pin, 100-pin and 121-pin packages. The general block diagram for all devices is shown in Figure 1-1.

The devices are differentiated from each other in six ways:

1. Flash program memory (128 Kbytes for PIC24FJ128GX6XX devices, 256 Kbytes for PIC24FJ256GX6XX devices, 512 Kbytes for PIC24FJ512GX6XX devices and 1024 Kbytes for PIC24FJ1024GX6XX devices).
2. Available I/O pins and ports (53 pins on 6 ports for 64-pin devices and 85 pins on 7 ports for 100-pin and 121-pin devices).
3. Available Interrupt-on-Change Notification (IOC) inputs (53 on 64-pin devices and 85 on 100-pin and 121-pin devices).
4. Available remappable pins (29 pins on 64-pin devices, 44 pins on 100-pin and 121-pin devices).
5. Available USB peripheral (available on PIC24FJXXXGB6XX devices; not available on PIC24FJXXXGA6XX devices).
6. Analog input channels (16 channels for 64-pin devices and 24 channels for 100-pin and 121-pin devices).

All other features for devices in this family are identical. These are summarized in Table 1-1, Table 1-2 and Table 1-3.

A list of the pin features available on the PIC24FJ1024GA610/GB610 family devices, sorted by function, is shown in Table 1-3. Note that this table shows the pin location of individual peripheral features and not how they are multiplexed on the same pin. This information is provided in the pinout diagrams in the beginning of this data sheet. Multiplexed features are sorted by the priority given to a feature, with the highest priority peripheral being listed first.

TABLE 1-1: DEVICE FEATURES FOR THE PIC24FJ1024GA606/GB606: 64-PIN DEVICES

Features	PIC24FJ128GX606	PIC24FJ256GX606	PIC24FJ512GX606	PIC24FJ1024GX606
Operating Frequency	DC – 32 MHz			
Program Memory (bytes)	128K	256K	512K	1024K
Program Memory (instructions)	44,032	88,064	176,128	352,256
Data Memory (bytes)	32K			
Interrupt Sources (soft vectors/ NMI traps)	103 (97/6)			
I/O Ports	Ports B, C, D, E, F, G			
Total I/O Pins	53			
Remappable Pins	29 (28 I/O, 1 input only)			
Timers: Total Number (16-bit)	5(1)			
32-Bit (from paired 16-bit timers)	2			
Input Capture Channels	6(1)			
Output Compare/PWM Channels	6(1)			
Input Change Notification Interrupt	53			
Serial Communications: UART	6(1)			
SPI (3-wire/4-wire)	3(1)			
I^2C	3			
Configurable Logic Cell (CLC)	4(1)			
Parallel Communications (EPMP/PSP)	Yes			
Capture/Compare/PWM/Timer Modules	3 Multiple Outputs and 4 Single Outputs			
JTAG Boundary Scan	Yes			
12/10-Bit Analog-to-Digital Converter (A/D) Module (input channels)	16			
Analog Comparators	3			
CTMU Interface	Yes			
Universal Serial Bus Controller	Yes (PIC24FJ1024GB606 devices only)			
Resets (and Delays)	Core POR, VDD POR, BOR, RESET Instruction, $\overline{MCLR}$, WDT, Illegal Opcode, REPEAT Instruction, Hardware Traps, Configuration Word Mismatch (OST, PLL Lock)			
Instruction Set	76 Base Instructions, Multiple Addressing Mode Variations			
Packages	64-Pin TQFP and QFN			

Note 1: Some peripherals are accessible through remappable pins.

EXAMPLE 6-1: ERASING A PROGRAM MEMORY BLOCK ('C' LANGUAGE CODE)

```
// C example using MPLAB XC16
    unsigned long progAddr = 0xXXXXXX;          // Address of row to write
    unsigned int  offset;
//Set up pointer to the first memory location to be written
    NVMADRU = progAddr>>16;                     // Initialize PM Page Boundary SFR
    NVMADR = progAddr & 0xFFFF;                 // Initialize lower word of address
    NVMCON = 0x4003;                            // Initialize NVMCON
    asm("DISI #5");                             // Block all interrupts with priority <7
                                                // for next 5 instructions
    __builtin_write_NVM();                      // check function to perform unlock
                                                // sequence and set WR
```

EXAMPLE 6-2: INITIATING A PROGRAMMING SEQUENCE

```
        DISI    #5                      ; Block all interrupts with priority <7
                                        ; for next 5 instructions
        MOV.B   #0x55, W0
        MOV     W0, NVMKEY              ; Write the 0x55 key
        MOV.B   #0xAA, W1               ;
        MOV     W1, NVMKEY              ; Write the 0xAA key
        BSET    NVMCON, #WR             ; Start the programming sequence
        NOP                             ; Required delays
        NOP
        BTSC    NVMCON, #15             ; and wait for it to be
        BRA     $-2                     ; completed
```

TABLE 8-2: INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	IRQ #	IVT Address	Interrupt Bit Location		
			Flag	Enable	Priority
OC5 – Output Compare 5	41	000066h	IFS2<9>	IEC2<9>	OC5Interrupt
OC6 – Output Compare 6	42	000068h	IFS2<10>	IEC2<10>	OC6Interrupt
CCT3 – Capture/Compare Timer3	43	00006Ah	IFS2<11>	IEC2<11>	CCT3Interrupt
CCT4 – Capture/Compare Timer4	44	00006Ch	IFS2<12>	IEC2<12>	CCT4Interrupt
PMP – Parallel Master Port	45	00006Eh	IFS2<13>	IEC2<13>	PMPInterrupt
DMA4 – Direct Memory Access 4	46	000070h	IFS2<14>	IEC2<14>	DMA4Interrupt
CCT5 – Capture/Compare Timer5	47	000072h	IFS2<15>	IEC2<15>	CCT5Interrupt
CCT6 – Capture/Compare Timer6	48	000074h	IFS3<0>	IEC3<0>	CCT6Interrupt
SI2C2 – I2C2 Slave Events	49	000076h	IFS3<1>	IEC3<1>	SI2C2Interrupt
MI2C2 – I2C2 Master Events	50	000078h	IFS3<2>	IEC3<2>	MI2C2Interrupt
CCT7 – Capture/Compare Timer7	51	00007Ah	IFS3<3>	IEC3<3>	CCT7Interrupt
—	52	—	—	—	—
INT3 – External Interrupt 3	53	00007Eh	IFS3<5>	IEC3<5>	INT3Interrupt
INT4 – External Interrupt 4	54	000080h	IFS3<6>	IEC3<6>	INT4Interrupt
—	55	—	—	—	—
—	56	—	—	—	—
—	57	—	—	—	—
SPI1RX – SPI1 Receive Done	58	000088h	IFS3<10>	IEC3<10>	SPI1RXInterrupt
SPI2RX – SPI2 Receive Done	59	00008Ah	IFS3<11>	IEC3<11>	SPI2RXInterrupt
SPI3RX – SPI3 Receive Done	60	00008Ch	IFS3<12>	IEC3<12>	SPI3RXInterrupt
DMA5 – Direct Memory Access 5	61	00008Eh	IFS3<13>	IEC3<13>	DMA5Interrupt
RTCC – Real-Time Clock and Calendar	62	000090h	IFS3<14>	IEC3<14>	RTCCInterrupt
CCP1 – Capture/Compare 1	63	000092h	IFS3<15>	IEC3<15>	CCP1Interrupt
CCP2 – Capture/Compare 2	64	000094h	IFS4<0>	IEC4<0>	CCP2Interrupt
U1E – UART1 Error	65	000096h	IFS4<1>	IEC4<1>	U1ErrInterrupt
U2E – UART2 Error	66	000098h	IFS4<2>	IEC4<2>	U2ErrInterrupt
CRC – Cyclic Redundancy Check	67	00009Ah	IFS4<3>	IEC4<3>	CRCInterrupt
DMA6 – Direct Memory Access 6	68	00009Ch	IFS4<4>	IEC4<4>	DMA6Interrupt
DMA7 – Direct Memory Access 7	69	00009Eh	IFS4<5>	IEC4<5>	DMA7Interrupt
SI2C3 – I2C3 Slave Events	70	0000A0h	IFS4<6>	IEC4<6>	SI2C3Interrupt
MI2C3 – I2C3 Master Events	71	0000A2h	IFS4<7>	IEC4<7>	MI2C3Interrupt
HLVD – High/Low-Voltage Detect	72	0000A4h	IFS4<8>	IEC4<8>	HLVDInterrupt
CCP7 – Capture/Compare 7	73	0000A6h	IFS4<9>	IEC4<9>	CCP7Interrupt
—	74	74	—	—	—
—	75	75	—	—	—
—	76	76	—	—	—
CTMU – Interrupt	77	0000AEh	IFS4<13>	IEC4<13>	CTMUInterrupt
—	78	78	—	—	—
—	79	79	—	—	—
—	80	80	—	—	—
U3E – UART3 Error	81	0000B6h	IFS5<1>	IEC5<1>	U3ErrInterrupt
U3RX – UART3 Receiver	82	0000B8h	IFS5<2>	IEC5<2>	U3RXInterrupt
U3TX – UART3 Transmitter	83	0000BAh	IFS5<3>	IEC5<3>	U3TXInterrupt

TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	FNOSC<2:0>	Notes
Oscillator with Frequency Division (OSCFDIV)	Internal/External	111	**1, 2, 3**
Digitally Controlled Oscillator (DCO)	Internal	110	**3**
Low-Power RC Oscillator (LPRC)	Internal	101	**3**
Secondary (Timer1) Oscillator (SOSC)	Secondary	100	**3**
Primary Oscillator (XT, HS or EC) with PLL Module	Primary	011	**4**
Primary Oscillator (XT, HS or EC)	Primary	010	**4**
Fast RC Oscillator with PLL Module (FRCPLL)	Internal	001	**3**
Fast RC Oscillator (FRC)	Internal	000	**3**

Note 1: The input oscillator to the OSCFDIV Clock mode is determined by the RCDIV<2:0> (CLKDIV<10:8) bits. At POR, the default value selects the FRC module.

2: This is the default oscillator mode for an unprogrammed (erased) device.

3: OSCO pin function is determined by the OSCIOFCN Configuration bit.

4: The POSCMD<1:0> Configuration bits select the oscillator driver mode (XT, HS or EC).

9.3 Control Registers

The operation of the oscillator is controlled by five Special Function Registers:

- OSCCON
- CLKDIV
- OSCTUN
- OSCDIV
- OSCFDIV

In addition, two registers are used to control the DCO:

- DCOCON
- DCOTUN

The OSCCON register (Register 9-1) is the main control register for the oscillator. It controls clock source switching and allows the monitoring of clock sources. OSCCON is protected by a write lock to prevent inadvertent clock switches. See **Section 9.4 “Clock Switching Operation”** for more information.

The CLKDIV register (Register 9-2) controls the features associated with Doze mode, as well as the postscalers for the OSCFDIV Clock mode and the PLL module.

The OSCTUN register (Register 9-3) allows the user to fine-tune the FRC Oscillator over a range of approximately ±1.5%. It also controls the FRC self-tuning features described in **Section 9.5 “FRC Active Clock Tuning”**.

The OSCDIV and OSCFDIV registers provide control for the system Oscillator Frequency Divider.

9.3.1 DCO OVERVIEW

The DCO (Digitally Controlled Oscillator) is a low-power alternative to the FRC. It can generate a wider selection of operating frequencies and can be trimmed to correct process variations if an exact frequency is required. However, the DCO is not designed for use with USB applications and cannot meet USB timing restrictions.

REGISTER 9-2: CLKDIV: CLOCK DIVIDER REGISTER

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
ROI	DOZE2	DOZE1	DOZE0	DOZEN(1)	RCDIV2	RCDIV1	RCDIV0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
CPDIV1	CPDIV0	PLLEN	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ROI:** Recover on Interrupt bit
1 = Interrupts clear the DOZEN bit and reset the CPU peripheral clock ratio to 1:1
0 = Interrupts have no effect on the DOZEN bit

bit 14-12 **DOZE<2:0>:** CPU Peripheral Clock Ratio Select bits
111 = 1:128
110 = 1:64
101 = 1:32
100 = 1:16
011 = 1:8 (default)
010 = 1:4
001 = 1:2
000 = 1:1

bit 11 **DOZEN:** Doze Enable bit(1)
1 = DOZE<2:0> bits specify the CPU peripheral clock ratio
0 = CPU peripheral clock ratio is set to 1:1

bit 10-8 **RCDIV<2:0>:** System Frequency Divider Clock Source Select bits
000 = Fast RC Oscillator (FRC)
001 = Fast RC Oscillator (FRC) with PLL module (FRCPLL)
010 = Primary Oscillator (XT, HS, EC)
011 = Primary Oscillator (XT, HS, EC) with PLL module (XTPLL, HSPLL, ECPLL)
100 = Secondary Oscillator (SOSC)
101 = Low-Power RC Oscillator (LPRC)
110 = Digitally Controlled Oscillator (DCO)
111 = Reserved; do not use

bit 7-6 **CPDIV<1:0>:** System Clock Select bits (postscaler select from 96 MHz PLL, 32 MHz clock branch)
11 = 4 MHz (divide-by-8)(2)
10 = 8 MHz (divide-by-4)(2)
01 = 16 MHz (divide-by-2)
00 = 32 MHz (divide-by-1)

bit 5 **PLLEN:** USB PLL Enable bit
1 = PLL is always active
0 = PLL is only active when a PLL Oscillator mode is selected (OSCCON<14:12> = 011 or 001)

bit 4-0 **Unimplemented:** Read as '0'

Note 1: This bit is automatically cleared when the ROI bit is set and an interrupt occurs.
2: This setting is not allowed while the USB module is enabled.

REGISTER 11-28: RPINR20: PERIPHERAL PIN SELECT INPUT REGISTER 20

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SCK1R5	SCK1R4	SCK1R3	SCK1R2	SCK1R1	SCK1R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SDI1R5	SDI1R4	SDI1R3	SDI1R2	SDI1R1	SDI1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **SCK1R<5:0>:** Assign SPI1 Clock Input (SCK1IN) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **SDI1R<5:0>:** Assign SPI1 Data Input (SDI1) to Corresponding RPn or RPIn Pin bits

REGISTER 11-29: RPINR21: PERIPHERAL PIN SELECT INPUT REGISTER 21

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	U3CTSR5	U3CTSR4	U3CTSR3	U3CTSR2	U3CTSR1	U3CTSR0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SS1R5	SS1R4	SS1R3	SS1R2	SS1R1	SS1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **U3CTSR<5:0>:** Assign UART3 Clear-to-Send ($\overline{\text{U3CTS}}$) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **SS1R<5:0>:** Assign SPI1 Slave Select Input (SS1IN) to Corresponding RPn or RPIn Pin bits

REGISTER 16-1: CCPxCON1L: CCPx CONTROL 1 LOW REGISTERS (CONTINUED)

bit 4 **CCSEL:** Capture/Compare Mode Select bit
1 = Input capture peripheral
0 = Output compare/PWM/timer peripheral (exact function is selected by the MOD<3:0> bits)

bit 3-0 **MOD<3:0>:** CCPx Mode Select bits
For CCSEL = 1 (Input Capture modes):
1xxx = Reserved
011x = Reserved
0101 = Capture every 16th rising edge
0100 = Capture every 4th rising edge
0011 = Capture every rising and falling edge
0010 = Capture every falling edge
0001 = Capture every rising edge
0000 = Capture every rising and falling edge (Edge Detect mode)
For CCSEL = 0 (Output Compare/Timer modes):
1111 = External Input mode: Pulse generator is disabled, source is selected by ICS<2:0>
1110 = Reserved
110x = Reserved
10xx = Reserved
0111 = Variable Frequency Pulse mode
0110 = Center-Aligned Pulse Compare mode, buffered
0101 = Dual Edge Compare mode, buffered
0100 = Dual Edge Compare mode
0011 = 16-Bit/32-Bit Single Edge mode, toggles output on compare match
0010 = 16-Bit/32-Bit Single Edge mode, drives output low on compare match
0001 = 16-Bit/32-Bit Single Edge mode, drives output high on compare match
0000 = 16-Bit/32-Bit Timer mode, output functions are disabled

NOTES:

REGISTER 17-2: SPIxCON1H: SPIx CONTROL REGISTER 1 HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AUDEN(1)	SPISGNEXT	IGNROV	IGNTUR	AUDMONO(2)	URDTEN(3)	AUDMOD1(4)	AUDMOD0(4)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT2	FRMCNT1	FRMCNT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **AUDEN:** Audio Codec Support Enable bit(1)
- 1 = Audio protocol is enabled; MSTEN controls the direction of both the SCKx and Frame (a.k.a. LRC), and this module functions as if FRMEN = 1, FRMSYNC = MSTEN, FRMCNT<2:0> = 001 and SMP = 0, regardless of their actual values
- 0 = Audio protocol is disabled

bit 14 **SPISGNEXT:** SPIx Sign-Extend RX FIFO Read Data Enable bit
- 1 = Data from RX FIFO is sign-extended
- 0 = Data from RX FIFO is not sign-extended

bit 13 **IGNROV:** Ignore Receive Overflow bit
- 1 = A Receive Overflow (ROV) is NOT a critical error; during ROV, data in the FIFO is not overwritten by the receive data
- 0 = A ROV is a critical error that stops SPI operation

bit 12 **IGNTUR:** Ignore Transmit Underrun bit
- 1 = A Transmit Underrun (TUR) is NOT a critical error and data indicated by URDTEN is transmitted until the SPIxTXB is not empty
- 0 = A TUR is a critical error that stops SPI operation

bit 11 **AUDMONO:** Audio Data Format Transmit bit(2)
- 1 = Audio data is mono (i.e., each data word is transmitted on both left and right channels)
- 0 = Audio data is stereo

bit 10 **URDTEN:** Transmit Underrun Data Enable bit(3)
- 1 = Transmits data out of SPIxURDTL/H register during Transmit Underrun conditions
- 0 = Transmits the last received data during Transmit Underrun conditions

bit 9-8 **AUDMOD<1:0>:** Audio Protocol Mode Selection bits(4)
- 11 = PCM/DSP mode
- 10 = Right Justified mode: This module functions as if SPIFE = 1, regardless of its actual value
- 01 = Left Justified mode: This module functions as if SPIFE = 1, regardless of its actual value
- 00 = I^2S mode: This module functions as if SPIFE = 0, regardless of its actual value

bit 7 **FRMEN:** Framed SPIx Support bit
- 1 = Framed SPIx support is enabled ($\overline{SSx}$ pin is used as the FSYNC input/output)
- 0 = Framed SPIx support is disabled

Note 1: AUDEN can only be written when the SPIEN bit = 0.
2: AUDMONO can only be written when the SPIEN bit = 0 and is only valid for AUDEN = 1.
3: URDTEN is only valid when IGNTUR = 1.
4: AUDMOD<1:0> bits can only be written when the SPIEN bit = 0 and are only valid when AUDEN = 1. When NOT in PCM/DSP mode, this module functions as if FRMSYPW = 1, regardless of its actual value.

18.2 Setting Baud Rate When Operating as a Bus Master

To compute the Baud Rate Generator reload value, use Equation 18-1.

EQUATION 18-1: COMPUTING BAUD RATE RELOAD VALUE(1,2,3)

$$FSCL = \frac{FCY}{(I2CxBRG + 2) * 2}$$

or:

$$I2CxBRG = \left[\frac{FCY}{(FSCL * 2)} - 2 \right]$$

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

2: These clock rate values are for guidance only. The actual clock rate can be affected by various system-level parameters. The actual clock rate should be measured in its intended application.

3: BRG values of 0 and 1 are forbidden.

18.3 Slave Address Masking

The I2CxMSK register (Register 18-4) designates address bit positions as “don’t care” for both 7-Bit and 10-Bit Addressing modes. Setting a particular bit location (= 1) in the I2CxMSK register causes the slave module to respond, whether the corresponding address bit value is a ‘0’ or a ‘1’. For example, when I2CxMSK is set to ‘0010000000’, the slave module will detect both addresses, ‘0000000000’ and ‘0010000000’.

To enable address masking, the Intelligent Peripheral Management Interface (IPMI) must be disabled by clearing the STRICT bit (I2CxCONL<11>).

Note: As a result of changes in the I^2C protocol, the addresses in Table 18-2 are reserved and will not be Acknowledged in Slave mode. This includes any address mask settings that include any of these addresses.

TABLE 18-1: I2Cx CLOCK RATES(1,2)

Required System FSCL	FCY	I2CxBRG Value		Actual FSCL
		(Decimal)	(Hexadecimal)	
100 kHz	16 MHz	78	4E	100 kHz
100 kHz	8 MHz	38	26	100 kHz
100 kHz	4 MHz	18	12	100 kHz
400 kHz	16 MHz	18	12	400 kHz
400 kHz	8 MHz	8	8	400 kHz
400 kHz	4 MHz	3	3	400 kHz
1 MHz	16 MHz	6	6	1.000 MHz
1 MHz	8 MHz	2	2	1.000 MHz

Note 1: Based on FCY = FOSC/2; Doze mode and PLL are disabled.

2: These clock rate values are for guidance only. The actual clock rate can be affected by various system-level parameters. The actual clock rate should be measured in its intended application.

TABLE 18-2: I2Cx RESERVED ADDRESSES(1)

Slave Address	R/$\overline{W}$ Bit	Description
0000 000	0	General Call Address(2)
0000 000	1	Start Byte
0000 001	x	CBus Address
0000 01x	x	Reserved
0000 1xx	x	HS Mode Master Code
1111 0xx	x	10-Bit Slave Upper Byte(3)
1111 1xx	x	Reserved

Note 1: The address bits listed here will never cause an address match independent of address mask settings.

2: This address will be Acknowledged only if GCEN = 1.

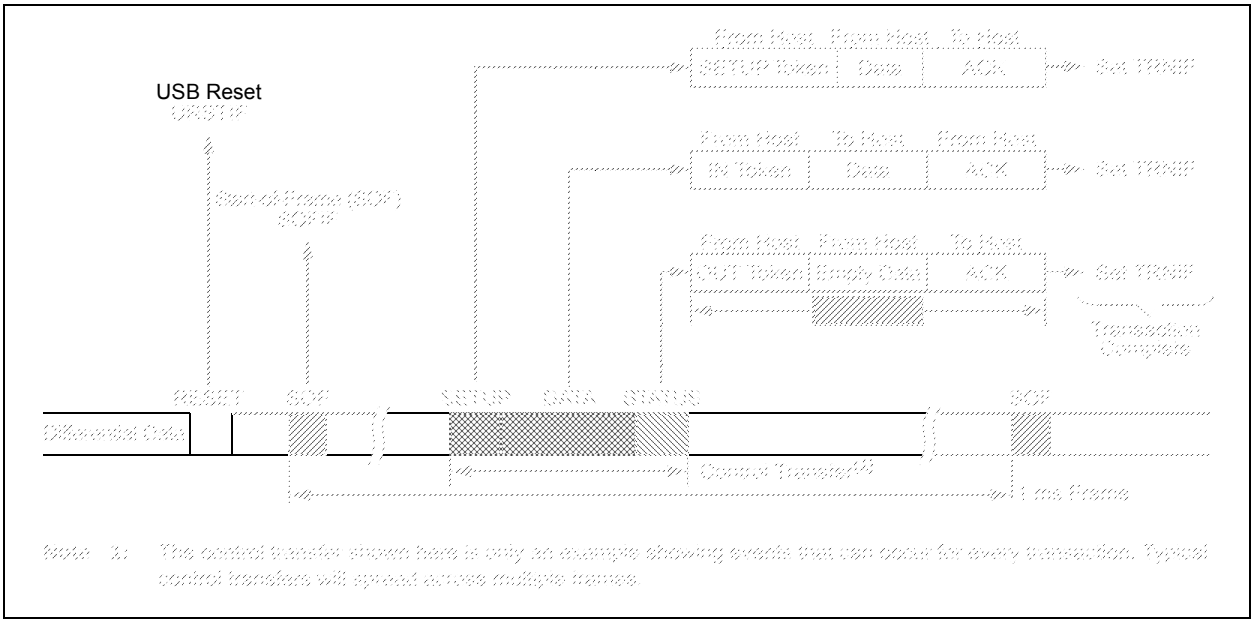
3: A match on this address can only occur on the upper byte in 10-Bit Addressing mode.

20.3.1 CLEARING USB OTG INTERRUPTS

Unlike device-level interrupts, the USB OTG interrupt status flags are not freely writable in software. All USB OTG flag bits are implemented as hardware set only bits. Additionally, these bits can only be cleared in software by writing a '1' to their locations (i.e., performing a MOV type instruction). Writing a '0' to a flag bit (i.e., a BCLR instruction) has no effect.

Note:	Throughout this data sheet, a bit that can only be cleared by writing a '1' to its location is referred to as "Write '1' to Clear". In register descriptions; this function is indicated by the descriptor, "K".

FIGURE 20-9: EXAMPLE OF A USB TRANSACTION AND INTERRUPT EVENTS



20.4 Device Mode Operation

The following section describes how to perform a common Device mode task. In Device mode, USB transfers are performed at the transfer level. The USB module automatically performs the status phase of the transfer.

20.4.1 ENABLING DEVICE MODE

1. Reset the Ping-Pong Buffer Pointers by setting, then clearing, the Ping-Pong Buffer Reset bit, PPBRST (U1CON<1>).
2. Disable all interrupts (U1IE and U1EIE = 00h).
3. Clear any existing interrupt flags by writing FFh to U1IR and U1EIR.
4. Verify that VBUS is present (non-OTG devices only).
5. Enable the USB module by setting the USBEN bit (U1CON<0>).
6. Set the OTGEN bit (U1OTGCON<2>) to enable OTG operation.
7. Enable the Endpoint 0 buffer to receive the first setup packet by setting the EPRXEN and EPHSHK bits for Endpoint 0 (U1EP0<3,0> = 1).
8. Power up the USB module by setting the USBPWR bit (U1PWRC<0>).
9. Enable the D+ pull-up resistor to signal an attach by setting the DPPULUP bit (U1OTGCON<7>).

REGISTER 21-3: PMCON3: EPMP CONTROL REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTWREN	PTRDEN	PTBE1EN	PTBE0EN	—	AWAITM1	AWAITM0	AWAITE
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PTWREN:** Write/Enable Strobe Port Enable bit
1 = PMWR/PMENB port is enabled
0 = PMWR/PMENB port is disabled

bit 14 **PTRDEN:** Read/Write Strobe Port Enable bit
1 = PMRD/$\overline{\text{PMWR}}$ port is enabled
0 = PMRD/$\overline{\text{PMWR}}$ port is disabled

bit 13 **PTBE1EN:** High Nibble/Byte Enable Port Enable bit
1 = PMBE1 port is enabled
0 = PMBE1 port is disabled

bit 12 **PTBE0EN:** Low Nibble/Byte Enable Port Enable bit
1 = PMBE0 port is enabled
0 = PMBE0 port is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-9 **AWAITM<1:0>:** Address Latch Strobe Wait States bits
11 = Wait of 3½ TCY
10 = Wait of 2½ TCY
01 = Wait of 1½ TCY
00 = Wait of ½ TCY

bit bit 8 **AWAITE:** Address Hold After Address Latch Strobe Wait States bits
1 = Wait of 1¼ TCY
0 = Wait of ¼ TCY

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 24-1: CLCxCONL: CLCx CONTROL REGISTER (LOW) (CONTINUED)

bit 2-0 **MODE<2:0>:** CLCx Mode bits
111 = Cell is a 1-input transparent latch with S and R
110 = Cell is a JK flip-flop with R
101 = Cell is a 2-input D flip-flop with R
100 = Cell is a 1-input D flip-flop with S and R
011 = Cell is an SR latch
010 = Cell is a 4-input AND
001 = Cell is an OR-XOR
000 = Cell is a AND-OR

REGISTER 24-2: CLCxCONH: CLCx CONTROL REGISTER (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	G4POL	G3POL	G2POL	G1POL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3 **G4POL:** Gate 4 Polarity Control bit
1 = The output of Channel 4 logic is inverted when applied to the logic cell
0 = The output of Channel 4 logic is not inverted

bit 2 **G3POL:** Gate 3 Polarity Control bit
1 = The output of Channel 3 logic is inverted when applied to the logic cell
0 = The output of Channel 3 logic is not inverted

bit 1 **G2POL:** Gate 2 Polarity Control bit
1 = The output of Channel 2 logic is inverted when applied to the logic cell
0 = The output of Channel 2 logic is not inverted

bit 0 **G1POL:** Gate 1 Polarity Control bit
1 = The output of Channel 1 logic is inverted when applied to the logic cell
0 = The output of Channel 1 logic is not inverted

REGISTER 25-1: AD1CON1: A/D CONTROL REGISTER 1 (CONTINUED)

bit 1 **SAMP:** A/D Sample Enable bit
1 = A/D Sample-and-Hold amplifiers are sampling
0 = A/D Sample-and-Hold amplifiers are holding

bit 0 **DONE:** A/D Conversion Status bit
1 = A/D conversion cycle has completed
0 = A/D conversion cycle has not started or is in progress

Note 1: This bit is only available when Extended DMA and buffer features are available (DMAEN = 1).

NOTES:

26.0 TRIPLE COMPARATOR MODULE

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Scalable Comparator Module"** (DS39734), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

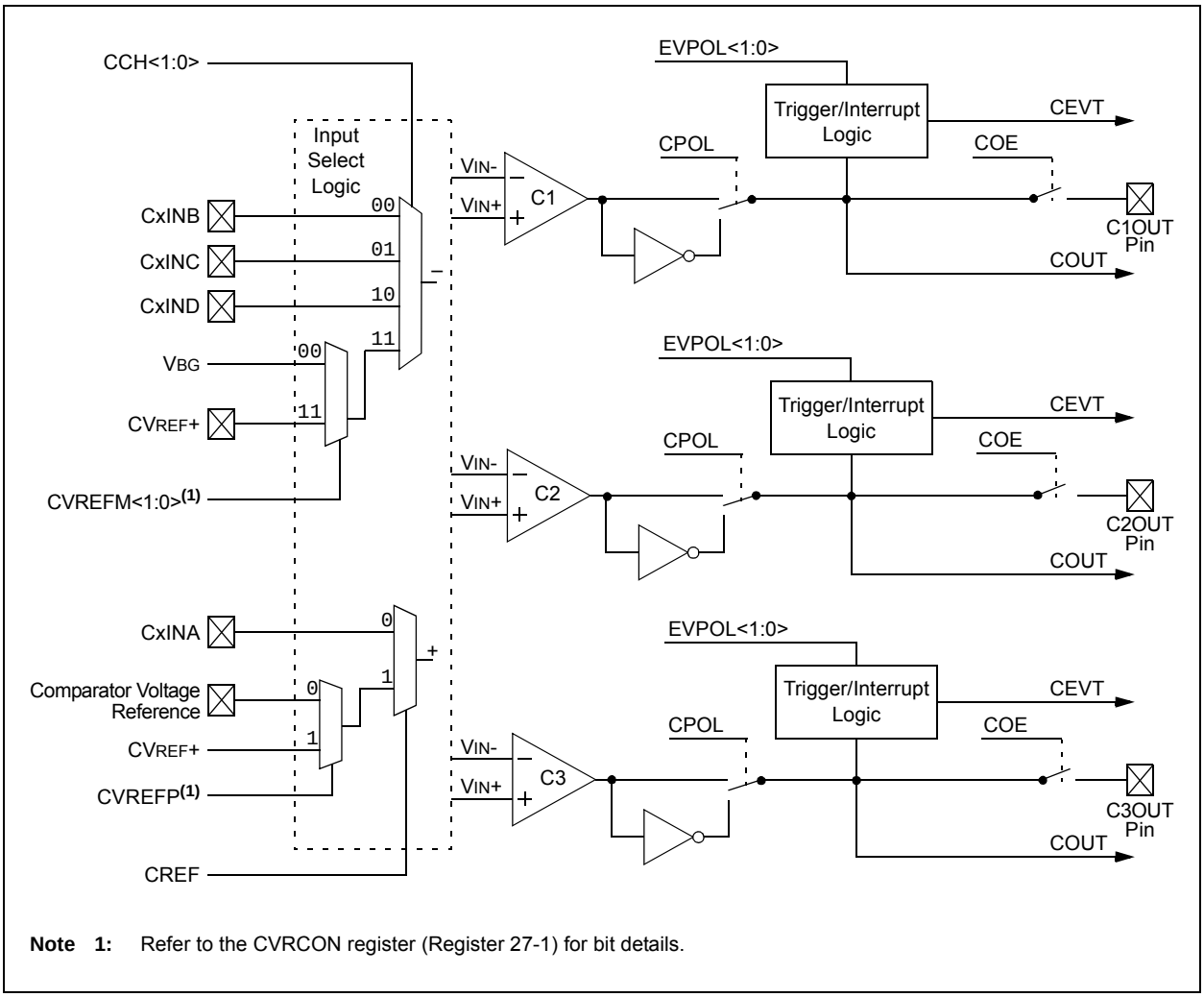
The triple comparator module provides three dual input comparators. The inputs to the comparator can be configured to use any one of five external analog inputs (CxINA, CxINB, CxINC, CxIND and CVREF+) and a voltage reference input from one of the internal band gap references or the comparator voltage reference generator (VBG and CVREF).

The comparator outputs may be directly connected to the CxOUT pins. When the respective COE bit equals '1', the I/O pad logic makes the unsynchronized output of the comparator available on the pin.

A simplified block diagram of the module in shown in Figure 26-1. Diagrams of the possible individual comparator configurations are shown in Figure 26-2 through Figure 26-4.

Each comparator has its own control register, CMxCON (Register 26-1), for enabling and configuring its operation. The output and event status of all three comparators is provided in the CMSTAT register (Register 26-2).

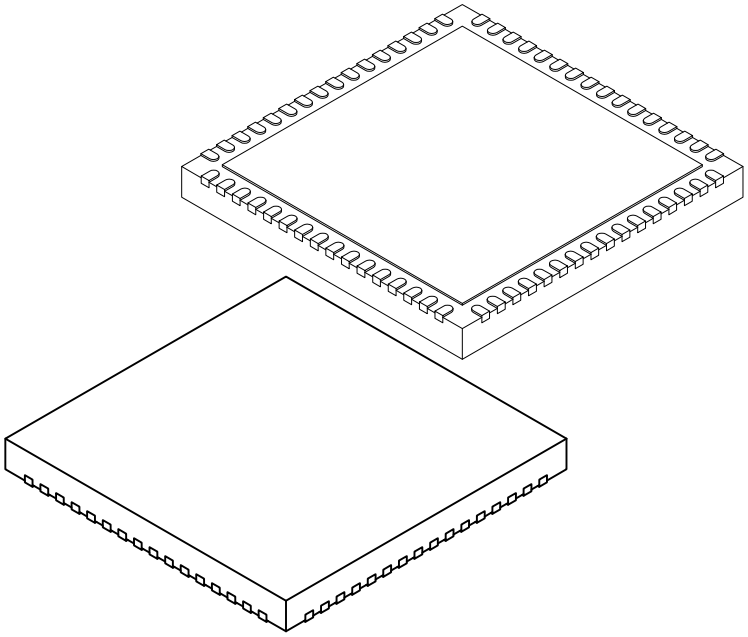
FIGURE 26-1: TRIPLE COMPARATOR MODULE BLOCK DIAGRAM



Note 1: Refer to the CVRCON register (Register 27-1) for bit details.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 7.70 x 7.70 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	7.60	7.70	7.80
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	7.60	7.70	7.80
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-213B Sheet 2 of 2