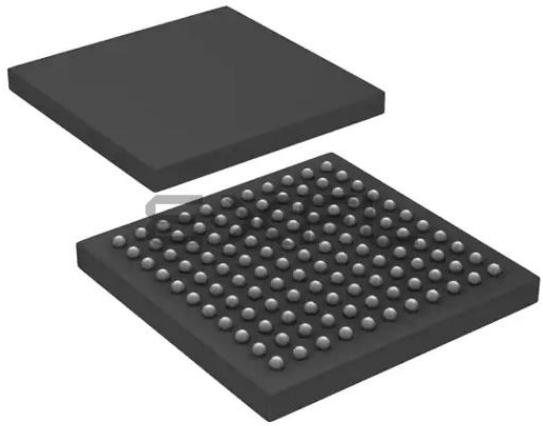
Microchip Technology - PIC24FJ1024GA610T-I/BG Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, HLVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	1MB (341.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj1024ga610t-i-bg

TABLE 2: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJXXXGA606)

Pin	Function	Pin	Function
1	IC4/CTED4/PMD5/RE5	33	**RP16**/RF3
2	SCL3/IC5/PMD6/RE6	34	**RP30**/RF2
3	SDA3/IC6/PMD7/RE7	35	INT0/RF6
4	C1IND/**RP21**/ICM1/OCM1A/PMA5/RG6	36	SDA1/RG3
5	C1INC/**RP26**/OCM1B/PMA4/RG7	37	SCL1/RG2
6	C2IND/**RP19**/ICM2/OCM2A/PMA3/RG8	38	VDD
7	$\overline{\text{MCLR}}$	39	OSCI/CLKI/RC12
8	C1INC/C2INC/C3INC/**RP27**/OCM2B/PMA2/PMALU/RG9	40	OSCO/CLKO/RC15
9	VSS	41	VSS
10	VDD	42	CLC4OUT/**RP2**/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/RD8
11	PGEC3/AN5/C1INA/**RP18**/ICM3/OCM3A/RB5	43	**RP4**/PMACK2/RD9
12	PGED3/AN4/C1INB/**RP28**/OCM3B/RB4	44	**RP3**/PMA15/PMCS2/RD10
13	AN3/C2INA/RB3	45	**RP12**/PMA14/PMCS1/RD11
14	AN2/CTCMP/C2INB/**RP13**/CTED13/RB2	46	CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/RD0
15	PGEC1/ALTCVREF-/ALTVREF-/AN1/**RP1**/CTED12/RB1	47	SOSCI/C3IND/RC13
16	PGED1/ALTCVREF+/ALTVREF+/AN0/**RP0**/PMA6/RB0	48	SOSCO/C3INC/**RPI37**/PWRLCLK/RC14
17	PGEC2/AN6/**RP6**/RB6	49	**RP24**/U5TX/ICM4/RD1
18	PGED2/AN7/**RP7**/U6TX/RB7	50	**RP23**/PMACK1/RD2
19	AVDD	51	**RP22**/ICM7/PMBE0/RD3
20	AVSS	52	**RP25**/PMWR/PMENB/RD4
21	AN8/**RP8**/PWRGT/RB8	53	**RP20**/PMRD/$\overline{\text{PMWR}}$/RD5
22	AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/PMA7/RB9	54	C3INB/U5RX/OC4/RD6
23	TMS/CVREF/AN10/PMA13/RB10	55	C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/RD7
24	TDO/AN11/REFI/PMA12/RB11	56	VCAP
25	VSS	57	N/C
26	VDD	58	$\overline{\text{U5CTS}}$/OC6/RF0
27	TCK/AN12/U6RX/CTED2/PMA11/RB12	59	RF1
28	TDI/AN13/CTED1/PMA10/RB13	60	PMD0/RE0
29	AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/RB14	61	PMD1/RE1
30	AN15/**RP29**/CTED6/PMA0/PMALL/RB15	62	PMD2/RE2
31	**RP10**/SDA2/PMA9/RF4	63	CTED9/PMD3/RE3
32	**RP17**/SCL2/PMA8/RF5	64	HLVDIN/CTED8/PMD4/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.

2.4 Voltage Regulator Pin (VCAP)

Note: This section applies only to PIC24FJ devices with an on-chip voltage regulator.

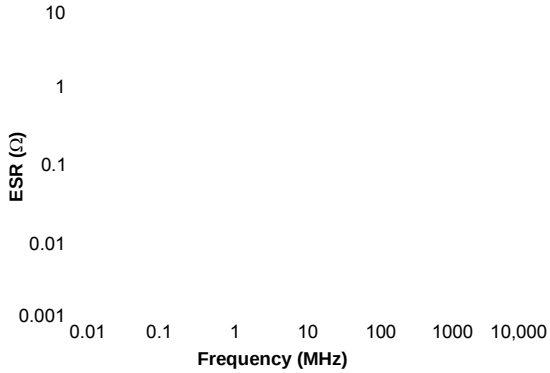
Refer to **Section 30.3 "On-Chip Voltage Regulator"** for details on connecting and using the on-chip regulator.

A low-ESR (< 5Ω) capacitor is required on the VCAP pin to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specifications can be used.

Designers may use Figure 2-3 to evaluate the ESR equivalence of candidate devices.

The placement of this capacitor should be close to VCAP. It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 33.0 "Electrical Characteristics"** for additional information.

FIGURE 2-3: FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP



Note: Typical data measurement at +25°C, 0V DC bias.

TABLE 2-1: SUITABLE CAPACITOR EQUIVALENTS (0805 CASE SIZE)

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage
TDK	C2012X5R1E106K085AC	10 µF	±10%	25V
TDK	C2012X5R1C106K085AC	10 µF	±10%	16V
Kemet	C0805C106M4PACTU	10 µF	±10%	16V
Murata	GRM21BR61E106KA3L	10 µF	±10%	25V
Murata	GRM21BR61C106KE15	10 µF	±10%	16V

6.6.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

The user can program one row of Flash program memory at a time. To do this, it is necessary to erase the 8-row erase block containing the desired row. The general process is:

1. Read eight rows of program memory (1024 instructions) and store in data RAM.
2. Update the program data in RAM with the desired new data.
3. Erase the block (see Example 6-1):
   a) Set the NVMOP<3:0> bits (NVMCON<3:0>) to '0011' to configure for block erase. Set the WREN (NVMCON<14>) bit.
   b) Write the starting address of the block to be erased into the NVMADRU/NVMADR registers.
   c) Write 55h to NVMKEY.
   d) Write AAh to NVMKEY.
   e) Set the WR bit (NVMCON<15>). The erase cycle begins and the CPU stalls for the duration of the erase cycle. When the erase is done, the WR bit is cleared automatically.
4. Update the TBLPAG register to point to the programming latches on the device. Update the NVMADRU/NVMADR registers to point to the destination in the program memory.
5. Write the first 128 instructions from data RAM into the program memory buffers (see Table 6-1).
6. Write the program block to Flash memory:
   a) Set the NVMOPx bits to '0010' to configure for row programming. Set the WREN bit.
   b) Write 55h to NVMKEY.
   c) Write AAh to NVMKEY.
   d) Set the WR bit. The programming cycle begins and the CPU stalls for the duration of the write cycle. When the write to Flash memory is done, the WR bit is cleared automatically.
7. Repeat Steps 4 through 6 using the next available 128 instructions from the block in data RAM, by incrementing the value in NVMADRU/NVMADR, until all 1024 instructions are written back to Flash memory.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPs, as shown in Example 6-2.

TABLE 6-1: EXAMPLE PAGE ERASE

Step 1: Set the NVMCON register to erase a page.
`MOV #0x4003, W0` `MOV W0, NVMCON`
Step 2: Load the address of the page to be erased into the NVMADR register pair.

`MOV #PAGE_ADDR_LO, W0`
`MOV W0, NVMADR`
`MOV #PAGE_ADDR_HI, W0`
`MOV W0, NVMADRU`

Step 3: Set the WR bit.

`MOV #0x55, W0`
`MOV W0, NVMKEY`
`MOV #0xAA, W0`
`MOV W0, NVMKEY`
`BSET NVMCON, #WR`
`NOP`
`NOP`
`NOP`

8.0 INTERRUPT CONTROLLER

Note 1: This data sheet summarizes the features of the PIC24FJ1024GA610/GB610 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Interrupts"** (DS70000600) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The PIC24FJ1024GA610/GB610 family interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the PIC24FJ1024GA610/GB610 family CPU.

The interrupt controller has the following features:

- Up to Eight Processor Exceptions and Software Traps
- Seven User-Selectable Priority Levels
- Interrupt Vector Table (IVT) with a Unique Vector for Each Interrupt or Exception Source
- Fixed Priority within a Specified User Priority Level
- Fixed Interrupt Entry and Return Latencies

8.1 Interrupt Vector Table

The PIC24FJ1024GA610/GB610 family Interrupt Vector Table (IVT), shown in Figure 8-1, resides in program memory starting at location, 000004h. The IVT contains 6 non-maskable trap vectors and up to 118 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

8.1.1 ALTERNATE INTERRUPT VECTOR TABLE

The Alternate Interrupt Vector Table (AIVT) is located after the IVT, as shown in Figure 8-1. The AIVTEN (INTCON2<8>) control bit provides access to the AIVT. If the AIVTEN bit is set, all interrupt and exception processes will use the alternate vectors instead of the default vectors. The alternate vectors are organized in the same manner as the default vectors.

The AIVT is available only if the Boot Segment has been defined and the AIVT has been enabled. To enable the AIVT, both the Configuration bit, AIVTDIS (FSEC<15>), and the AIVTEN bit (INTCON2<8> in the SFR), have to be set. When the AIVT is enabled, all interrupts and exception processes use the alternate vectors instead of the default vectors. The AIVT begins at the start of the last page of the Boot Segment (BS) defined by the BSLIM<12:0> bits. The AIVT address is: (BSLIM<12:0> – 1) x 0x800.

8.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The PIC24FJ1024GA610/GB610 family devices clear their registers in response to a Reset, which forces the PC to zero. The device then begins program execution at location, 0x000000. A GOTO instruction at the Reset address can redirect program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

9.8 Secondary Oscillator

9.8.1 BASIC SOSC OPERATION

PIC24FJ1024GA610/GB610 family devices do not have to set the SOSCEN bit to use the Secondary Oscillator. Any module requiring the SOSC (such as RTCC or Timer1) will automatically turn on the SOSC when the clock signal is needed. The SOSC, however, has a long start-up time (as long as 1 second). To avoid delays for peripheral start-up, the SOSC can be manually started using the SOSCEN bit.

To use the Secondary Oscillator, the SOSCSEL bit (FOSC<3>) must be set to '1'. Programming the SOSCSEL bit to '0' configures the SOSC pins for Digital mode, enabling digital I/O functionality on the pins.

9.8.2 CRYSTAL SELECTION

The 32.768 kHz crystal used for the SOSC must have the following specifications in order to properly start up and run at the correct frequency when in High-Power mode:

- 12.5 pF loading capacitance
- 1.0 pF shunt capacitance
- A typical ESR of 35K; 50K maximum

In addition, the two external crystal loading capacitors should be in the range of 18-22 pF, which will be based on the PC board layout. The capacitors should be C0G, 5% tolerance and rated 25V or greater.

The accuracy and duty cycle of the SOSC can be measured on the REFO pin, and is recommended to be in the range of 40-60% and accurate to ±0.65 Hz.

9.8.3 LOW-POWER SOSC OPERATION

The Secondary Oscillator can operate in two distinct levels of power consumption based on device configuration. In Low-Power mode, the oscillator operates in a low drive strength, low-power state. By default, the oscillator uses a higher drive strength, and therefore, requires more power. Low-Power mode is selected by Configuration bit, SOSCHP (FDEVOPT1<3>). The lower drive strength of this mode makes the SOSC more sensitive to noise and requires a longer start-up time. This mode can be used with lower load capacitance crystals (6 pF-9 pF) having higher ESR ratings (50K-80K) to reduce Sleep current in the RTCC. When Low-Power mode is used, care must be taken in the design and layout of the SOSC circuit to ensure that the oscillator starts up and oscillates properly. PC board layout issues, stray capacitance and other factors will need to be carefully controlled in order for the crystal to operate.

10.0 POWER-SAVING FEATURES

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Power-Saving Features"** (DS39698), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

The PIC24FJ1024GA610/GB610 family of devices provides the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of circuits being clocked constitutes lower consumed power. All PIC24F devices manage power consumption in four different ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software-Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption, while still maintaining critical application features, such as timing-sensitive communications.

10.1 Clock Frequency and Clock Switching

PIC24F devices allow for a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSC<2:0> bits. The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 "Oscillator Configuration"**.

10.2 Instruction-Based Power-Saving Modes

PIC24F devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution; Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembly syntax of the PWRSAV instruction is shown in Example 10-1.

The XC16 C compiler offers "built-in" functions for the power-saving modes as follows:

```
Idle();          // places part in Idle
Sleep();         // places part in Sleep
```

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

Note: SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.

10.2.1 SLEEP MODE

Sleep mode has these features:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption will be reduced to a minimum provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate during Sleep mode since the system clock source is disabled.
- The LPRC clock will continue to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals may continue to operate in Sleep mode. This includes items, such as the Input Change Notification (ICN) on the I/O ports or peripherals that use an external clock input. Any peripheral that requires the system clock source for its operation will be disabled in Sleep mode.

The device will wake-up from Sleep mode on any of the these events:

- On any interrupt source that is individually enabled
- On any form of device Reset
- On a WDT time-out

On wake-up from Sleep, the processor will restart with the same clock source that was active when Sleep mode was entered.

EXAMPLE 10-1: PWRSAV INSTRUCTION SYNTAX

```
PWRSAV    #SLEEP_MODE            ; Put the device into SLEEP mode
PWRSAV    #IDLE_MODE             ; Put the device into IDLE mode
```

REGISTER 11-22: RPINR12: PERIPHERAL PIN SELECT INPUT REGISTER 12

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	TCKIBR5	TCKIBR4	TCKIBR3	TCKIBR2	TCKIBR1	TCKIBR0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	TCKIAR5	TCKIAR4	TCKIAR3	TCKIAR2	TCKIAR1	TCKIAR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **TCKIBR<5:0>:** Assign MCCP/SCCP Clock Input B to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **TCKIAR<5:0>:** Assign MCCP/SCCP Clock Input A to Corresponding RPn or RPIn Pin bits

REGISTER 11-23: RPINR14: PERIPHERAL PIN SELECT INPUT REGISTER 14

U-0	U-0	r-1	r-1	r-1	r-1	r-1	r-1
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	r-1	r-1	r-1	r-1	r-1	r-1
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

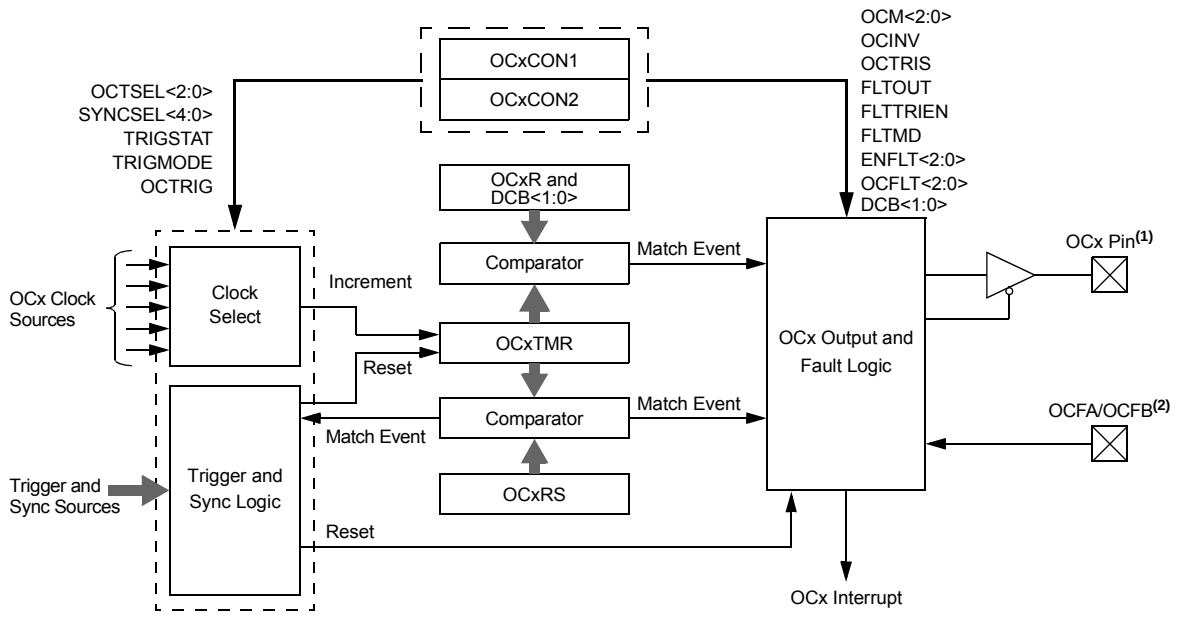
bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **Reserved**: Maintain as ‘1’

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **Reserved**: Maintain as ‘1’

FIGURE 15-1: OUTPUT COMPARE x BLOCK DIAGRAM (16-BIT MODE)



Note 1: The OCx outputs must be assigned to an available RPn pin before use. See **Section 11.4 "Peripheral Pin Select (PPS)"** for more information.

2: The OCFA/OCFB Fault inputs must be assigned to an available RPn/RPIn pin before use. See **Section 11.4 "Peripheral Pin Select (PPS)"** for more information.

15.2 Compare Operations

In Compare mode (Figure 15-1), the output compare module can be configured for Single-Shot or Continuous mode pulse generation. It can also repeatedly toggle an output pin on each timer event.

To set up the module for compare operations:

1. Configure the OCx output for one of the available Peripheral Pin Select pins if available on the OCx module you are using. Otherwise, configure the dedicated OCx output pins.
2. Calculate the required values for the OCxR and (for Double Compare modes) OCxRS Duty Cycle registers:
   a) Determine the instruction clock cycle time. Take into account the frequency of the external clock to the timer source (if one is used) and the timer prescaler settings.
   b) Calculate the time to the rising edge of the output pulse relative to the timer start value (0000h).
   c) Calculate the time to the falling edge of the pulse based on the desired pulse width and the time to the rising edge of the pulse.
3. Write the rising edge value to OCxR and the falling edge value to OCxRS.
4. Set the Timer Period register, PRy, to a value equal to or greater than the value in OCxRS.
5. Set the OCM<2:0> bits for the appropriate compare operation (= `0xx`).
6. For Trigger mode operations, set OCTRIG to enable Trigger mode. Set or clear TRIGMODE to configure Trigger operation and TRIGSTAT to select a hardware or software Trigger. For Synchronous mode, clear OCTRIG.
7. Set the SYNCSEL<4:0> bits to configure the Trigger or Sync source. If free-running timer operation is required, set the SYNCSELx bits to '`00000`' (no Sync/Trigger source).
8. Select the time base source with the OCTSEL<2:0> bits. If necessary, set the TON bit for the selected timer, which enables the compare time base to count. Synchronous mode operation starts as soon as the time base is enabled; Trigger mode operation starts after a Trigger source event occurs.

17.0 SERIAL PERIPHERAL INTERFACE (SPI)

Note: This data sheet summarizes the features of the PIC24FJ1024GA610/GB610 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Serial Peripheral Interface (SPI) with Audio Codec Support"** (DS70005136), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

The Serial Peripheral Interface (SPI) module is a synchronous serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D Converters, etc. The SPI module is compatible with the Motorola® SPI and SIOP interfaces. All devices in the PIC24FJ1024GA610/GB610 family include three SPI modules.

The module supports operation in two buffer modes. In Standard mode, data is shifted through a single serial buffer. In Enhanced Buffer mode, data is shifted through a FIFO buffer. The FIFO level depends on the configured mode.

Variable length data can be transmitted and received from 2 to 32 bits.

Note: Do not perform Read-Modify-Write operations (such as bit-oriented instructions) on the SPIxBUF register in either Standard or Enhanced Buffer mode.

The module also supports a basic framed SPI protocol while operating in either Master or Slave mode. A total of four framed SPI configurations are supported.

The module also supports Audio modes. Four different Audio modes are available.

- I^2S mode
- Left Justified
- Right Justified
- PCM/DSP

In each of these modes, the serial clock is free-running and audio data is always transferred.

If an audio protocol data transfer takes place between two devices, then usually one device is the master and the other is the slave. However, audio data can be transferred between two slaves. Because the audio protocols require free-running clocks, the master can be a third party controller. In either case, the master generates two free-running clocks: SCKx and LRC (Left, Right Channel Clock/$\overline{SS}$x/FSYNC).

The SPI serial interface consists of four pins:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- SCKx: Shift Clock Input or Output
- $\overline{SS}$x: Active-Low Slave Select or Frame Synchronization I/O Pulse

The SPI module can be configured to operate using 2, 3 or 4 pins. In the 3-pin mode, $\overline{SS}$x is not used. In the 2-pin mode, both SDOx and $\overline{SS}$x are not used.

The SPI module has the ability to generate three interrupts reflecting the events that occur during the data communication. The following types of interrupts can be generated:

1. Receive interrupts are signalled by SPIxRXIF. This event occurs when:
   - RX watermark interrupt
   - SPIROV = 1
   - SPIRBF = 1
   - SPIRBE = 1

   provided the respective mask bits are enabled in SPIxIMSKL/H.
2. Transmit interrupts are signalled by SPIxTXIF. This event occurs when:
   - TX watermark interrupt
   - SPITUR = 1
   - SPITBF = 1
   - SPITBE = 1

   provided the respective mask bits are enabled in SPIxIMSKL/H.
3. General interrupts are signalled by SPIxIF. This event occurs when
   - FRMERR = 1
   - SPIBUSY = 1
   - SRMT = 1

   provided the respective mask bits are enabled in SPIxIMSKL/H.

A block diagram of the module in Enhanced Buffer mode is shown in Figure 17-1.

Note: In this section, the SPI modules are referred to together as SPIx, or separately as SPI1, SPI2 or SPI3. Special Function Registers will follow a similar notation. For example, SPIxCON1 and SPIxCON2 refer to the control registers for any of the three SPI modules.

REGISTER 20-16: U1IR: USB INTERRUPT STATUS REGISTER (DEVICE MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/K-0, HS	U-0	R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS
STALLIF	—	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	K = Write '1' to Clear bit	HS = Hardware Settable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **STALLIF:** STALL Handshake Interrupt bit
- 1 = A STALL handshake was sent by the peripheral during the handshake phase of the transaction in Device mode
- 0 = A STALL handshake has not been sent

bit 6 **Unimplemented:** Read as '0'

bit 5 **RESUMEIF:** Resume Interrupt bit
- 1 = A K-state is observed on the D+ or D- pin for 2.5 μs (differential '1' for low speed, differential '0' for full speed)
- 0 = No K-state is observed

bit 4 **IDLEIF:** Idle Detect Interrupt bit
- 1 = Idle condition is detected (constant Idle state of 3 ms or more)
- 0 = No Idle condition is detected

bit 3 **TRNIF:** Token Processing Complete Interrupt bit
- 1 = Processing of the current token is complete; read the U1STAT register for endpoint information
- 0 = Processing of the current token is not complete; clear the U1STAT register or load the next token from STAT (clearing this bit causes the STAT FIFO to advance)

bit 2 **SOFIF:** Start-of-Frame Token Interrupt bit
- 1 = A Start-of-Frame token is received by the peripheral or the Start-of-Frame threshold is reached by the host
- 0 = No Start-of-Frame token is received or threshold reached

bit 1 **UERRIF**: USB Error Condition Interrupt bit
- 1 = An unmasked error condition has occurred; only error states enabled in the U1EIE register can set this bit
- 0 = No unmasked error condition has occurred

bit 0 **URSTIF:** USB Reset Interrupt bit
- 1 = Valid USB Reset has occurred for at least 2.5 μs; Reset state must be cleared before this bit can be reasserted
- 0 = No USB Reset has occurred; individual bits can only be cleared by writing a '1' to the bit position as part of a word write operation on the entire register. Using Boolean instructions or bitwise operations to write to a single bit position will cause all set bits, at the moment of the write, to become cleared

Note: Individual bits can only be cleared by writing a '1' to the bit position as part of a word write operation on the entire register. Using Boolean instructions or bitwise operations to write to a single bit position will cause all set bits, at the moment of the write, to become cleared.

20.7.3 USB ENDPOINT MANAGEMENT REGISTERS

REGISTER 20-21: U1EPn: USB ENDPOINT n CONTROL REGISTERS (n = 0 TO 15)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LSPD(1)	RETRYDIS(1)	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **LSPD:** Low-Speed Direct Connection Enable bit (U1EP0 only)(1)
1 = Direct connection to a low-speed device is enabled
0 = Direct connection to a low-speed device is disabled

bit 6 **RETRYDIS:** Retry Disable bit (U1EP0 only)(1)
1 = Retry NAK transactions are disabled
0 = Retry NAK transactions are enabled; retry is done in hardware

bit 5 **Unimplemented:** Read as '0'

bit 4 **EPCONDIS:** Bidirectional Endpoint Control bit
If EPTXEN and EPRXEN = 1:
1 = Disables Endpoint n from control transfers; only TX and RX transfers are allowed
0 = Enables Endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed
For All Other Combinations of EPTXEN and EPRXEN:
This bit is ignored.

bit 3 **EPRXEN:** Endpoint Receive Enable bit
1 = Endpoint n receive is enabled
0 = Endpoint n receive is disabled

bit 2 **EPTXEN:** Endpoint Transmit Enable bit
1 = Endpoint n transmit is enabled
0 = Endpoint n transmit is disabled

bit 1 **EPSTALL:** Endpoint STALL Status bit
1 = Endpoint n was stalled
0 = Endpoint n was not stalled

bit 0 **EPHSHK:** Endpoint Handshake Enable bit
1 = Endpoint handshake is enabled
0 = Endpoint handshake is disabled (typically used for isochronous endpoints)

Note 1: These bits are available only for U1EP0 and only in Host mode. For all other U1EPn registers, these bits are always unimplemented and read as '0'.

22.3 Registers

22.3.1 RTCC CONTROL REGISTERS

REGISTER 22-1: RTCCON1L: RTCC CONTROL REGISTER 1 (LOW)

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
RTCEN	—	—	—	WRLOCK	PWCEN	PWCPOL	PWCPOE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
RTCOE	OUTSEL2	OUTSEL1	OUTSEL0	—	—	—	TSAEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **RTCEN:** RTCC Enable bit
1 = RTCC is enabled and counts from selected clock source
0 = RTCC is not enabled

bit 14-12 **Unimplemented:** Read as ‘0’

bit 11 **WRLOCK:** RTCC Register Write Lock
1 = RTCC registers are locked
0 = RTCC registers may be written to by user

bit 10 **PWCEN:** Power Control Enable bit
1 = Power control is enabled
0 = Power control is disabled

bit 9 **PWCPOL:** Power Control Polarity bit
1 = Power control output is active-high
0 = Power control output is active-low

bit 8 **PWCPOE:** Power Control Output Enable bit
1 = Power control output pin is enabled
0 = Power control output pin is disabled

bit 7 **RTCOE:** RTCC Output Enable bit
1 = RTCC output is enabled
0 = RTCC output is disabled

bit 6-4 **OUTSEL<2:0>:** RTCC Output Signal Selection bits
111 = Unused
110 = Unused
101 = Unused
100 = Timestamp A event
011 = Power control
010 = RTCC input clock
001 = Second clock
000 = Alarm event

bit 3-1 **Unimplemented:** Read as ‘0’

bit 0 **TSAEN:** Timestamp A Enable bit
1 = Timestamp event will occur when a low pulse is detected on the $\overline{\text{TMPR}}$ pin
0 = Timestamp is disabled

REGISTER 22-5: RTCCON3L: RTCC CONTROL REGISTER 3 (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWCSAMP7	PWCSAMP6	PWCSAMP5	PWCSAMP4	PWCSAMP3	PWCSAMP2	PWCSAMP1	PWCSAMP0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWCSTAB7	PWCSTAB6	PWCSTAB5	PWCSTAB4	PWCSTAB3	PWCSTAB2	PWCSTAB1	PWCSTAB0
bit 7							bit 0

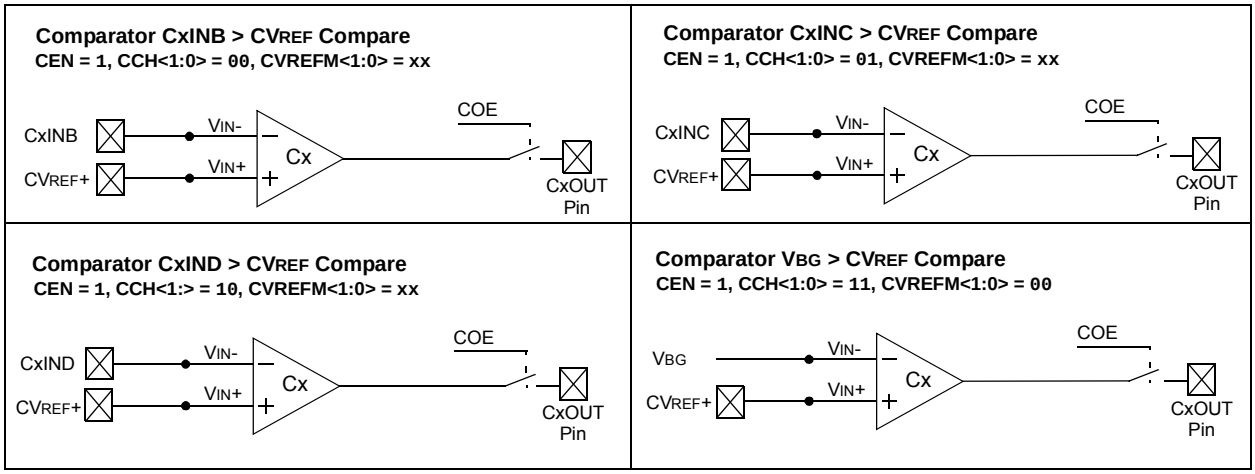
Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **PWCSAMP<7:0>:** Power Control Sample Window Timer bits
11111111 = Sample window is always enabled, even when PWCEN = 0
11111110 = Sample window is 254 TPWCCLK clock periods
•
•
•
00000001 = Sample window is 1 TPWCCLK clock period
00000000 = No sample window

bit 7-0 **PWCSTAB<7:0>:** Power Control Stability Window Timer bits(1)
11111111 = Stability window is 255 TPWCCLK clock periods
11111110 = Stability window is 254 TPWCCLK clock periods
•
•
•
00000001 = Stability window is 1 TPWCCLK clock period
00000000 = No stability window; sample window starts when the alarm event triggers

Note 1: The sample window always starts when the stability window timer expires, except when its initial value is 00h.

FIGURE 26-4: INDIVIDUAL COMPARATOR CONFIGURATIONS WHEN CREF = 1 AND CVREFP = 1



REGISTER 28-3: CTMUCON2L: CTMU CONTROL REGISTER 2 LOW

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	IRSTEN	—	DSCHS2	DSCHS1	DSCHS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4 **IRSTEN:** CTMU Current Source Reset Enable bit
1 = Signal selected by DSCHS<2:0> bits or IDISSEN control bit will reset CTMU edge detect logic
0 = CTMU edge detect logic will not occur

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **DSCHS<2:0>:** Discharge Source Select bits
111 = CLC2 out
110 = CLC1 out
101 = Disabled
100 = A/D end of conversion
011 = MCCP3 auxiliary output
010 = MCCP2 auxiliary output
001 = MCCP1 auxiliary output
000 = Disabled

REGISTER 30-4: FBSLIM CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	U-1	U-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
—	—	—	BSLIM<12:8>				
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
BSLIM<7:0>							
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘1’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-13 **Unimplemented:** Read as ‘1’

bit 12-0 **BSLIM<12:0>:** Active Boot Segment Code Flash Page Address Limit (Inverted) bits

This bit field contains the last active Boot Segment Page + 1 (i.e., first page address of GS). The value is stored as an inverted page address, such that programming additional ‘0’s can only increase the size of BS. If BSLIM<12:0> is set to all ‘1’s (unprogrammed default), active Boot Segment size is zero.

REGISTER 30-11: FDEVOPT1 CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 15							bit 8

U-1	U-1	U-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	U-1
—	—	—	ALTVREF	SOSCHP(1)	TMPRPIN	ALTCMPI	—
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-5 **Unimplemented:** Read as '1'

bit 4 **ALTVREF:** Alternate Voltage Reference Location Enable bit (100-pin and 121-pin devices only)
1 = VREF+ and CVREF+ on RA10, VREF- and CVREF- on RA9
0 = VREF+ and CVREF+ on RB0, VREF- and CVREF- on RB1

bit 3 **SOSCHP:** SOSC High-Power Enable bit (valid only when SOSCSEL = 1)(1)
1 = SOSC High-Power mode is enabled
0 = SOSC Low-Power mode is enabled

bit 2 **TMPRPIN:** Tamper Pin Enable bit
1 = $\overline{\text{TMPR}}$ pin function is disabled
0 = $\overline{\text{TMPR}}$ pin function is enabled

bit 1 **ALTCMPI:** Alternate Comparator Input Enable bit
1 = C1INC, C2INC and C3INC are on their standard pin locations
0 = C1INC, C2INC and C3INC are on RG9

bit 0 **Unimplemented:** Read as '1'

Note 1: High-Power mode is for crystals with 35K ESR (typical). Low-Power mode is for crystals with more than 65K ESR.

TABLE 33-9: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	VOL	**Output Low Voltage**					
DO10		I/O Ports	—	—	0.4	V	IOL = 6.6 mA, VDD = 3.6V
			—	—	0.8	V	IOL = 18 mA, VDD = 3.6V
			—	—	0.35	V	IOL = 5.0 mA, VDD = 2V
DO16		OSCO/CLKO	—	—	0.18	V	IOL = 6.6 mA, VDD = 3.6V
			—	—	0.2	V	IOL = 5.0 mA, VDD = 2V
	VOH	**Output High Voltage**					
DO20		I/O Ports	3.4	—	—	V	IOH = -3.0 mA, VDD = 3.6V
			3.25	—	—	V	IOH = -6.0 mA, VDD = 3.6V
			2.8	—	—	V	IOH = -18 mA, VDD = 3.6V
			1.65	—	—	V	IOH = -1.0 mA, VDD = 2V
			1.4	—	—	V	IOH = -3.0 mA, VDD = 2V
DO26		OSCO/CLKO	3.3	—	—	V	IOH = -6.0 mA, VDD = 3.6V
			1.85	—	—	V	IOH = -1.0 mA, VDD = 2V

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 33-10: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
		Program Flash Memory					
D130	EP	Cell Endurance	10000	—	—	E/W	-40°C to +85°C
D131	VPR	VDD for Read	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D132B		VDD for Self-Timed Write	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D133A	TIW	Self-Timed Word Write Cycle Time	—	20	—	µs	
		Self-Timed Row Write Cycle Time	—	1.5	—	ms	
D133B	TIE	Self-Timed Page Erase Time	20	—	40	ms	
D134	TRETD	Characteristic Retention	20	—	—	Year	If no other specifications are violated
D135	IDDP	Supply Current during Programming	—	5	—	mA	

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated.

FIGURE 33-5: INL vs. CODE (10-BIT MODE)

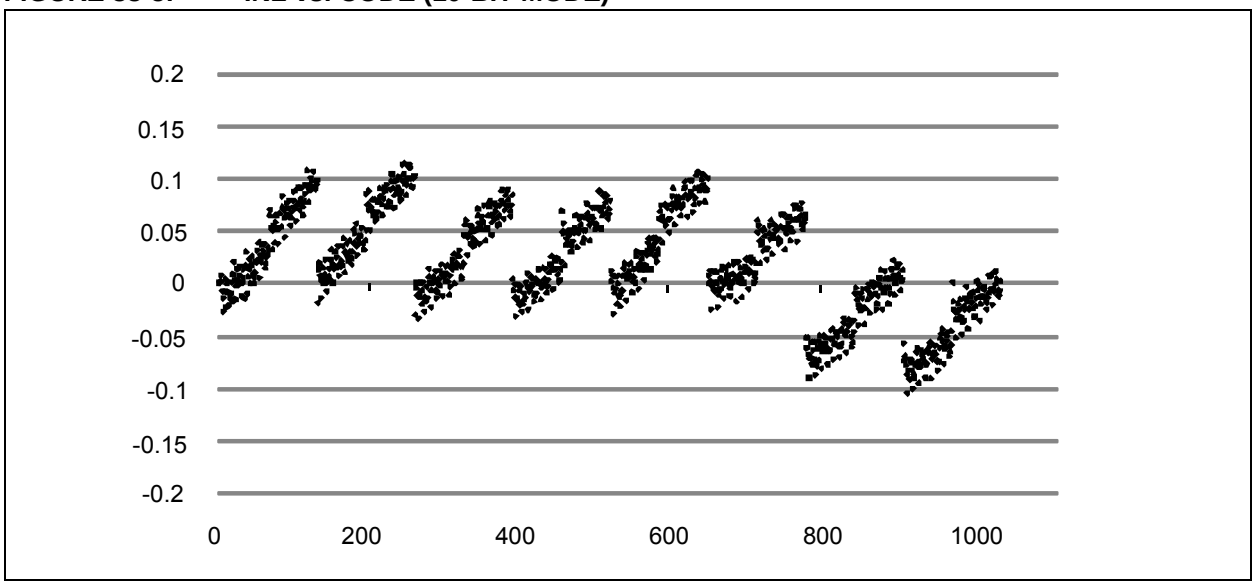


FIGURE 33-6: DNL vs. CODE (10-BIT MODE)