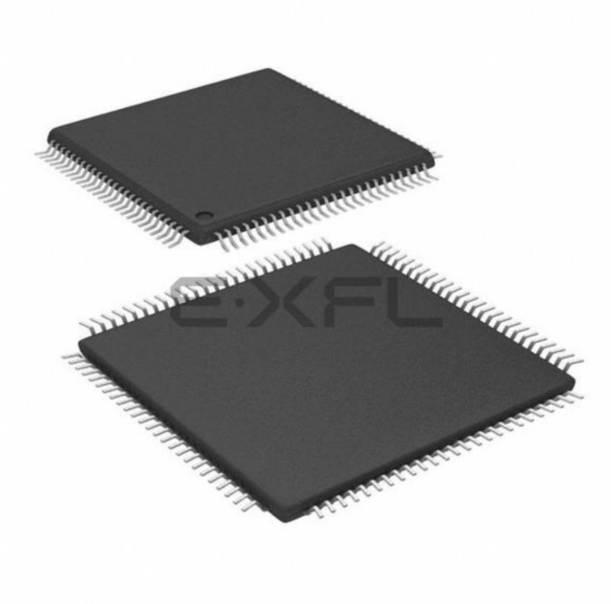
Microchip Technology - PIC24FJ1024GB610T-I/PT Datasheet



What is "Embedded - Microcontrollers"?

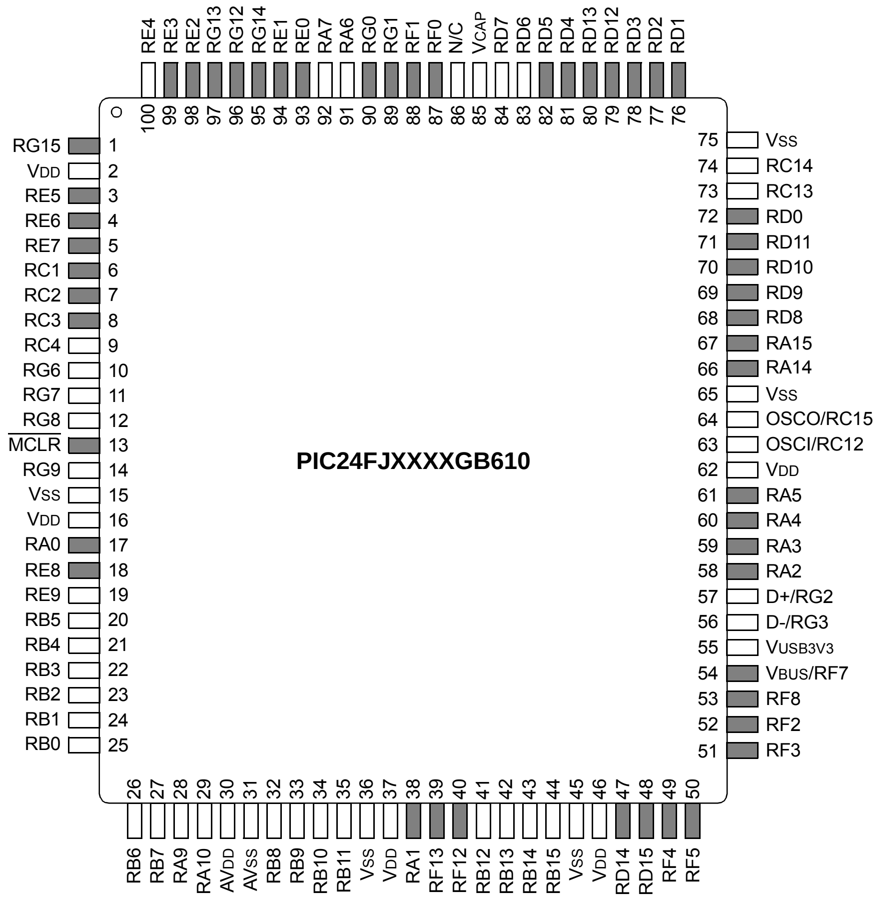
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	1MB (341.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj1024gb610t-i-pt

Pin Diagrams[1] (Continued)

100-Pin TQFP



Legend: See Table 5 for a complete description of pin functions. Pinouts are subject to change.

Note 1: Gray shading indicates 5.5V tolerant input pins.

Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33/PIC24 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

> **Note 1:** To access the documents listed below, browse to the documentation section of the PIC24FJ1024GA610/GB610 product page of the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.
>
> In addition to parameters, features and other documentation, the resulting page provides links to the related family reference manual sections.

- **"CPU with Extended Data Space (EDS)"** (DS39732)
- **"Data Memory with Extended Data Space (EDS)"** (DS39733)
- **"Direct Memory Access Controller (DMA)"** (DS39742)
- **"PIC24F Flash Program Memory"** (DS30009715)
- **"Reset"** (DS39712)
- **"Interrupts"** (DS70000600)
- **"Power-Saving Features"** (DS39698)
- **"I/O Ports with Peripheral Pin Select (PPS)"** (DS39711)
- **"Timers"** (DS39704)
- **"Input Capture with Dedicated Timer"** (DS70000352)
- **"Output Compare with Dedicated Timer"** (DS70005159)
- **"Capture/Compare/PWM/Timer (MCCP and SCCP)"** (DS33035A)
- **"Serial Peripheral Interface (SPI) with Audio Codec Support"** (DS70005136)
- **"Inter-Integrated Circuit (I^2C)"** (DS70000195)
- **"UART"** (DS39708)
- **"USB On-The-Go (OTG)"** (DS39721)
- **"Enhanced Parallel Master Port (EPMP)"** (DS39730)
- **"RTCC with Timestamp"** (DS70005193)
- **"RTCC with External Power Control"** (DS39745)
- **"32-Bit Programmable Cyclic Redundancy Check (CRC)"** (DS30009729)
- **"12-Bit A/D Converter with Threshold Detect"** (DS39739)
- **"Scalable Comparator Module"** (DS39734)
- **"Dual Comparator Module"** (DS39710)
- **"Charge Time Measurement Unit (CTMU) and CTMU Operation with Threshold Detect"** (DS30009743)
- **"High-Level Integration with Programmable High/Low-Voltage Detect (HLVD)"** (DS39725)
- **"Watchdog Timer (WDT)"** (DS39697)
- **"CodeGuard™ Intermediate Security"** (DS70005182)
- **"High-Level Device Integration"** (DS39719)
- **"Programming and Diagnostics"** (DS39716)
- **"Dual Partition Flash Program Memory"** (DS70005156)

TABLE 4-8: SFR MAP: 0400h BLOCK

File Name	Address	All Resets	File Name	Address	All Resets
SPI (CONTINUED)			**CONFIGURABLE LOGIC CELL (CLC) (CONTINUED)**		
SPI1BUFL	0400	0000	CLC3CONL	047C	0000
SPI1BUFH	0402	0000	CLC3CONH	047E	0000
SPI1BRGL	0404	xxxx	CLC3SELL	0480	0000
SPI1IMSK1	0408	0000	CLC3GLSL	0484	0000
SPI1IMSK2	040A	0000	CLC3GLSH	0486	0000
SPI1URDTL	040C	0000	CLC4CONL	0488	0000
SPI1URDTH	040E	0000	CLC4CONH	048A	0000
SPI2CON1	0410	0x00	CLC4SELL	048C	0000
SPI2CON2	0412	0000	CLC4GLSL	0490	0000
SPI2CON3	0414	0000	CLC4GLSH	0492	0000
SPI2STATL	0418	0028	**I^2C**		
SPI2STATH	041A	0000	I2C1RCV	0494	0000
SPI2BUFL	041C	0000	I2C1TRN	0496	00FF
SPI2BUFH	041E	0000	I2C1BRG	0498	0000
SPI2BRGL	0420	xxxx	I2C1CON1	049A	1000
SPI2IMSK1	0424	0000	I2C1CON2	049C	0000
SPI2IMSK2	0426	0000	I2C1STAT	049E	0000
SPI2URDTL	0428	0000	I2C1ADD	04A0	0000
SPI2URDTH	042A	0000	I2C1MSK	04A2	0000
SPI3CON1	042C	0x00	I2C2RCV	04A4	0000
SPI3CON2	042E	0000	I2C2TRN	04A6	00FF
SPI3CON3	0430	0000	I2C2BRG	04A8	0000
SPI3STATL	0434	0028	I2C2CON1	04AA	1000
SPI3STATH	0436	0000	I2C2CON2	04AC	0000
SPI3BUFL	0438	0000	I2C2STAT	04AE	0000
SPI3BUFH	043A	0000	I2C2ADD	04B0	0000
SPI3BRGL	043C	xxxx	I2C2MSK	04B2	0000
SPI3IMSK1	0440	0000	I2C3RCV	04B4	0000
SPI3IMSK2	0442	0000	I2C3TRN	04B6	00FF
SPI3URDTL	0444	0000	I2C3BRG	04B8	0000
SPI3URDTH	0446	0000	I2C3CON1	04BA	1000
CONFIGURABLE LOGIC CELL (CLC)			I2C3CON2	04BC	0000
CLC1CONL	0464	0000	I2C3STAT	04BE	0000
CLC1CONH	0466	0000	I2C3ADD	04C0	0000
CLC1SELL	0468	0000	I2C3MSK	04C2	0000
CLC1GLSL	046C	0000	**DMA**		
CLC1GLSH	046E	0000	DMACON	04C4	0000
CLC2CONL	0470	0000	DMABUF	04C6	0000
CLC2CONH	0472	0000	DMAL	04C8	0000
CLC2SELL	0474	0000	DMAH	04CA	0000
CLC2GLSL	0478	0000	DMACH0	04CC	0000
CLC2GLSH	047A	0000	DMAINT0	04CE	0000

Legend: — = unimplemented, read as ‘0’; x = undefined. Reset values are shown in hexadecimal.

TABLE 4-11: SFR MAP: 0700h BLOCK

File Name	Address	All Resets	File Name	Address	All Resets
A/D			**PERIPHERAL PIN SELECT**		
ADC1BUF0	0712	xxxx	RPINR0	0790	3F3F
ADC1BUF1	0714	xxxx	RPINR1	0792	3F3F
ADC1BUF2	0716	xxxx	RPINR2	0794	3F3F
ADC1BUF3	0718	xxxx	RPINR3	0796	3F3F
ADC1BUF4	071A	xxxx	RPINR4	0798	3F3F
ADC1BUF5	071C	xxxx	RPINR5	079A	3F3F
ADC1BUF6	071E	xxxx	RPINR6	079C	3F3F
ADC1BUF7	0720	xxxx	RPINR7	079E	3F3F
ADC1BUF8	0722	xxxx	RPINR8	07A0	003F
ADC1BUF9	0724	xxxx	RPINR11	07A6	3F3F
ADC1BUF10	0726	xxxx	RPINR12	07A8	3F3F
ADC1BUF11	0728	xxxx	RPINR14	07AC	3F3F
ADC1BUF12	072A	xxxx	RPINR15	07AE	003F
ADC1BUF13	072C	xxxx	RPINR17	07B2	3F00
ADC1BUF14	072E	xxxx	RPINR18	07B4	3F3F
ADC1BUF15	0730	xxxx	RPINR19	07B6	3F3F
ADC1BUF16	0732	xxxx	RPINR20	07B8	3F3F
ADC1BUF17	0734	xxxx	RPINR21	07BA	3F3F
ADC1BUF18	0736	xxxx	RPINR22	07BC	3F3F
ADC1BUF19	0738	xxxx	RPINR23	07BE	3F3F
ADC1BUF20	073A	xxxx	RPINR25	07C2	3F3F
ADC1BUF21	073C	xxxx	RPINR27	07C6	3F3F
ADC1BUF22	073E	xxxx	RPINR28	07C8	3F3F
ADC1BUF23	0740	xxxx	RPINR29	07CA	003F
ADC1BUF24	0742	xxxx	RPOR0	07D4	0000
ADC1BUF25	0744	xxxx	RPOR1	07D6	0000
AD1CON1	0746	0000	RPOR2	07D8	0000
AD1CON2	0748	0000	RPOR3	07DA	0000
AD1CON3	074A	0000	RPOR4	07DC	0000
AD1CHS	074C	0000	RPOR5	07DE	0000
AD1CSSH	074E	0000	RPOR6	07E0	0000
AD1CSSL	0750	0000	RPOR7	07E2	0000
AD1CON4	0752	0000	RPOR8	07E4	0000
AD1CON5	0754	0000	RPOR9	07E6	0000
AD1CHITH	0756	0000	RPOR10	07E8	0000
AD1CHITL	0758	0000	RPOR11	07EA	0000
AD1CTMENH	075A	0000	RPOR12	07EC	0000
AD1CTMENL	075C	0000	RPOR13	07EE	0000
AD1RESDMA	075E	0000	RPOR14	07F0	0000
NVM			RPOR15	07F2	0000
NVMCON	0760	0000			
NVMADR	0762	xxxx			
NVMADRU	0764	00xx			
NVMKEY	0766	0000			

Legend: — = unimplemented, read as '0'; x = undefined. Reset values are shown in hexadecimal.

REGISTER 5-1: DMACON: DMA ENGINE CONTROL REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
DMAEN	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PRSSEL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **DMAEN:** DMA Module Enable bit
1 = Enables module
0 = Disables module and terminates all active DMA operation(s)

bit 14-1 **Unimplemented:** Read as ‘0’

bit 0 **PRSSEL:** Channel Priority Scheme Selection bit
1 = Round-robin scheme
0 = Fixed priority scheme

6.0 FLASH PROGRAM MEMORY

> **Note:** This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"PIC24F Flash Program Memory"** (DS30009715), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

The PIC24FJ1024GA610/GB610 family of devices contains internal Flash program memory for storing and executing application code. The program memory is readable, writable and erasable. The Flash memory can be programmed in four ways:

- In-Circuit Serial Programming™ (ICSP™)
- Run-Time Self-Programming (RTSP)
- JTAG
- Enhanced In-Circuit Serial Programming (Enhanced ICSP)

ICSP allows a PIC24FJ1024GA610/GB610 family device to be serially programmed while in the end application circuit. This is simply done with two lines for the programming clock and programming data (named PGECx and PGEDx, respectively), and three other lines for power (VDD), ground (VSS) and Master Clear ($\overline{MCLR}$). This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using `TBLRD` (Table Read) and `TBLWT` (Table Write) instructions. With RTSP, the user may write program memory data in blocks of 128 instructions (384 bytes) at a time and erase program memory in blocks of 1024 instructions (3072 bytes) at a time.

The device implements a 7-bit Error Correcting Code (ECC). The NVM block contains a logic to write and read ECC bits to and from the Flash memory. The Flash is programmed at the same time as the corresponding ECC parity bits. The ECC provides improved resistance to Flash errors. ECC single bit errors can be transparently corrected. ECC Double-Bit Errors (ECCDBE) result in a trap.

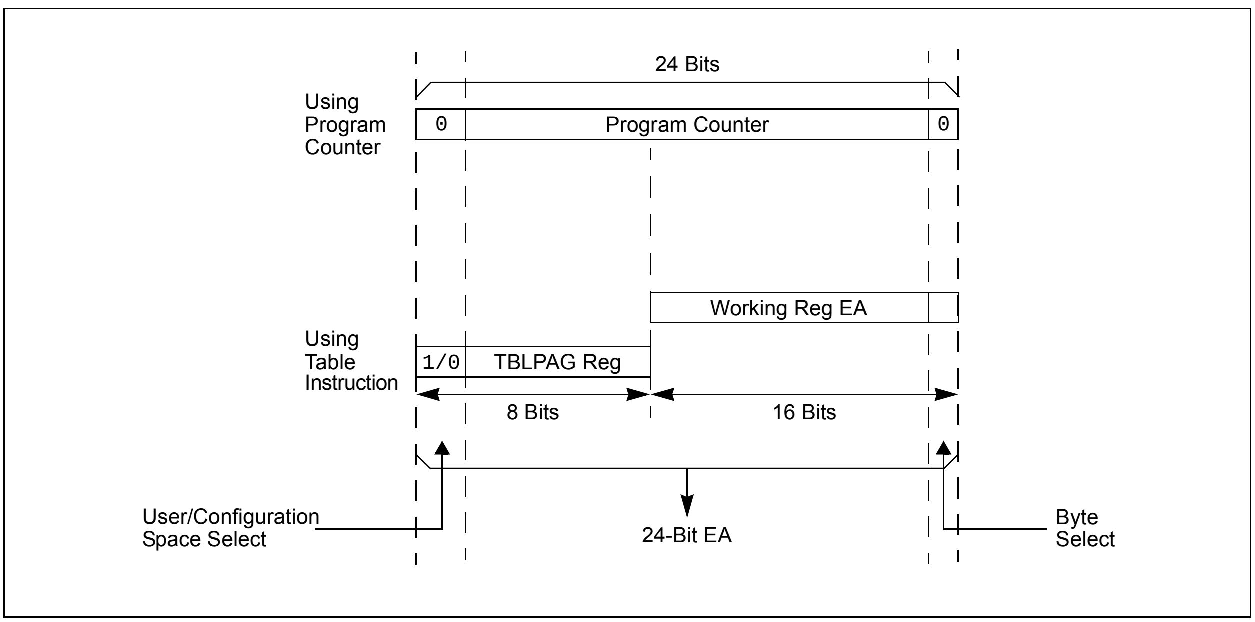
6.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the Table Read and Table Write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using the TBLPAG<7:0> bits and the Effective Address (EA) from a W register, specified in the table instruction, as shown in Figure 6-1.

The `TBLRDL` and the `TBLWTL` instructions are used to read or write to bits<15:0> of program memory. `TBLRDL` and `TBLWTL` can access program memory in both Word and Byte modes.

The `TBLRDH` and `TBLWTH` instructions are used to read or write to bits<23:16> of program memory. `TBLRDH` and `TBLWTH` can also access program memory in Word or Byte mode.

FIGURE 6-1: ADDRESSING FOR TABLE REGISTERS



REGISTER 7-1: RCON: RESET CONTROL REGISTER

R/W-0	R/W-0	R/W-1	R/W-0	U-0	U-0	R/W-0	R/W-0
TRAPR(1)	IOPUWR(1)	SBOREN	RETEN(2)	—	—	CM(1)	VREGS(3)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR(1)	SWR(1)	SWDTEN(4)	WDTO(1)	SLEEP(1)	IDLE(1)	BOR(1)	POR(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **TRAPR:** Trap Reset Flag bit(1)
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit(1)
1 = An illegal opcode detection, an illegal address mode or Uninitialized W register is used as an Address Pointer and caused a Reset
0 = An illegal opcode or Uninitialized W register Reset has not occurred

bit 13 **SBOREN:** Software Enable/Disable of BOR bit
1 = BOR is turned on in software
0 = BOR is turned off in software

bit 12 **RETEN:** Retention Mode Enable bit(2)
1 = Retention mode is enabled while device is in Sleep modes (1.2V regulator enabled)
0 = Retention mode is disabled

bit 11-10 **Unimplemented:** Read as ‘0’

bit 9 **CM:** Configuration Word Mismatch Reset Flag bit(1)
1 = A Configuration Word Mismatch Reset has occurred
0 = A Configuration Word Mismatch Reset has not occurred

bit 8 **VREGS:** Fast Wake-up from Sleep bit(3)
1 = Fast wake-up is enabled (uses more power)
0 = Fast wake-up is disabled (uses less power)

bit 7 **EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin bit(1)
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset (Instruction) Flag bit(1)
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed

Note 1: All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
2: If the $\overline{\text{LPCFG}}$ Configuration bit is ‘1’ (unprogrammed), the retention regulator is disabled and the RETEN bit has no effect. Retention mode preserves the SRAM contents during Sleep.
3: Re-enabling the regulator after it enters Standby mode will add a delay, T_{VREG}, when waking up from Sleep. Applications that do not use the voltage regulator should set this bit to prevent this delay from occurring.
4: If the FWDTEN<1:0> Configuration bits are ‘11’ (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

9.6.1 CONSIDERATIONS FOR USB OPERATION

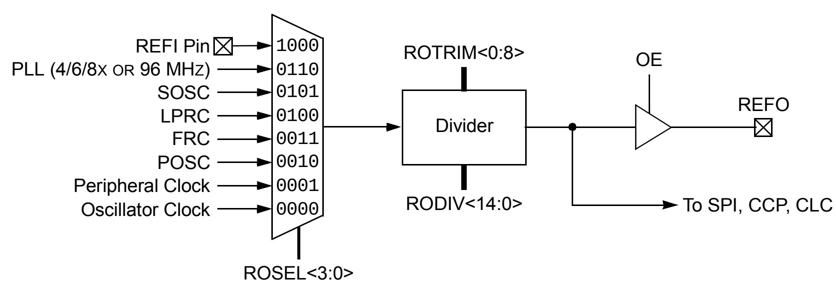
When using the USB On-The-Go module in PIC24FJ1024GA610/GB610 devices, users must always observe these rules in configuring the system clock:

- The system clock frequency must be 16 MHz or 32 MHz. System clock frequencies below 16 MHz are not allowed for USB module operation.
- The Oscillator modes listed in Table 9-3 are the only oscillator configurations that permit USB operation. There is no provision to provide a separate external clock source to the USB module.
- For USB operation, the selected clock source (EC, HS or XT) must meet the USB clock tolerance requirements.
- When the FRCPLL Oscillator mode is used for USB applications, the FRC self-tune system should be used as well. While the FRC is accurate, the only two ways to ensure the level of accuracy, required by the *"USB 2.0 Specification"* throughout the application's operating range, are either the self-tune system or manually changing the TUN<5:0> bits.
- The user must always ensure that the FRC source is configured to provide a frequency of 4 MHz or 8 MHz (RCDIV<2:0> = `001` or `000`) and that the USB PLL prescaler is configured appropriately.
- All other Oscillator modes are available; however, USB operation is not possible when these modes are selected. They may still be useful in cases where other power levels of operation are desirable and the USB module is not needed (e.g., the application is Sleeping and waiting for a bus attachment).

9.7 Reference Clock Output

In addition to the CLKO output (FOSC/2), the PIC24FJ1024GA610/GB610 family devices can be configured to provide a reference clock output signal to a port pin. This feature is available in all oscillator configurations and allows the user to select a greater range of clock submultiples to drive external devices in the application. CLKO is enabled by Configuration bit, OSCIOFCN, and is independent of the REFO reference clock. REFO is mappable to any I/O pin that has mapped output capability. Refer to Table 11-4 for more information. The REFO module block diagram is shown on Figure 9-3.

FIGURE 9-3: REFERENCE CLOCK GENERATOR



REGISTER 11-28: RPINR20: PERIPHERAL PIN SELECT INPUT REGISTER 20

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SCK1R5	SCK1R4	SCK1R3	SCK1R2	SCK1R1	SCK1R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SDI1R5	SDI1R4	SDI1R3	SDI1R2	SDI1R1	SDI1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **SCK1R<5:0>:** Assign SPI1 Clock Input (SCK1IN) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **SDI1R<5:0>:** Assign SPI1 Data Input (SDI1) to Corresponding RPn or RPIn Pin bits

REGISTER 11-29: RPINR21: PERIPHERAL PIN SELECT INPUT REGISTER 21

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	U3CTSR5	U3CTSR4	U3CTSR3	U3CTSR2	U3CTSR1	U3CTSR0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SS1R5	SS1R4	SS1R3	SS1R2	SS1R1	SS1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **U3CTSR<5:0>:** Assign UART3 Clear-to-Send ($\overline{\text{U3CTS}}$) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **SS1R<5:0>:** Assign SPI1 Slave Select Input (SS1IN) to Corresponding RPn or RPIn Pin bits

14.1.2 CASCADED (32-BIT) MODE

By default, each module operates independently with its own 16-bit timer. To increase resolution, adjacent even and odd modules can be configured to function as a single 32-bit module. (For example, Modules 1 and 2 are paired, as are Modules 3 and 4, and so on.) The odd numbered module (ICx) provides the Least Significant 16 bits of the 32-bit register pairs and the even numbered module (ICy) provides the Most Significant 16 bits. Wrap-arounds of the ICx registers cause an increment of their corresponding ICy registers.

Cascaded operation is configured in hardware by setting the IC32 bits (ICxCON2<8>) for both modules.

14.2 Capture Operations

The input capture module can be configured to capture timer values and generate interrupts on rising edges on ICx or all transitions on ICx. Captures can be configured to occur on all rising edges or just some (every 4^{th} or 16^{th}). Interrupts can be independently configured to generate on each event or a subset of events.

To set up the module for capture operations:

1. Configure the ICx input for one of the available Peripheral Pin Select pins.
2. If Synchronous mode is to be used, disable the Sync source before proceeding.
3. Make sure that any previous data has been removed from the FIFO by reading ICxBUF until the ICBNE bit (ICxCON1<3>) is cleared.
4. Set the SYNCSELx bits (ICxCON2<4:0>) to the desired Sync/Trigger source.
5. Set the ICTSELx bits (ICxCON1<12:10>) for the desired clock source.
6. Set the ICIx bits (ICxCON1<6:5>) to the desired interrupt frequency.
7. Select Synchronous or Trigger mode operation:
   a) Check that the SYNCSELx bits are not set to '00000'.
   b) For Synchronous mode, clear the ICTRIG bit (ICxCON2<7>).
   c) For Trigger mode, set ICTRIG and clear the TRIGSTAT bit (ICxCON2<6>).
8. Set the ICMx bits (ICxCON1<2:0>) to the desired operational mode.
9. Enable the selected Sync/Trigger source.

For 32-bit cascaded operations, the setup procedure is slightly different:

1. Set the IC32 bits for both modules (ICyCON2<8> and ICxCON2<8>), enabling the even numbered module first. This ensures the modules will start functioning in unison.
2. Set the ICTSELx and SYNCSELx bits for both modules to select the same Sync/Trigger and time base source. Set the even module first, then the odd module. Both modules must use the same ICTSELx and SYNCSELx bits settings.
3. Clear the ICTRIG bit of the even module (ICyCON2<7>). This forces the module to run in Synchronous mode with the odd module, regardless of its Trigger setting.
4. Use the odd module's ICIx bits (ICxCON1<6:5>) to set the desired interrupt frequency.
5. Use the ICTRIG bit of the odd module (ICxCON2<7>) to configure Trigger or Synchronous mode operation.

> **Note:** For Synchronous mode operation, enable the Sync source as the last step. Both input capture modules are held in Reset until the Sync source is enabled.

6. Use the ICMx bits of the odd module (ICxCON1<2:0>) to set the desired Capture mode.

The module is ready to capture events when the time base and the Sync/Trigger source are enabled. When the ICBNE bit (ICxCON1<3>) becomes set, at least one capture value is available in the FIFO. Read input capture values from the FIFO until the ICBNE clears to '0'.

For 32-bit operation, read both the ICxBUF and ICyBUF for the full 32-bit timer value (ICxBUF for the lsw, ICyBUF for the msw). At least one capture value is available in the FIFO buffer when the odd module's ICBNE bit (ICxCON1<3>) becomes set. Continue to read the buffer registers until ICBNE is cleared (performed automatically by hardware).

NOTES:

REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1 (CONTINUED)

bit 4	**OCFLT0:** PWM Fault 0 (OCFA pin) Condition Status bit(2,4) 1 = PWM Fault 0 has occurred 0 = No PWM Fault 0 has occurred
bit 3	**TRIGMODE:** Trigger Status Mode Select bit 1 = TRIGSTAT (OCxCON2<6>) is cleared when OCxRS = OCxTMR or in software 0 = TRIGSTAT is only cleared by software
bit 2-0	**OCM<2:0>:** Output Compare x Mode Select bits(1) 111 = Center-Aligned PWM mode on OCx(2) 110 = Edge-Aligned PWM mode on OCx(2) 101 = Double Compare Continuous Pulse mode: Initialize the OCx pin low; toggle the OCx state continuously on alternate matches of OCxR and OCxRS 100 = Double Compare Single-Shot mode: Initialize the OCx pin low; toggle the OCx state on matches of OCxR and OCxRS for one cycle 011 = Single Compare Continuous Pulse mode: Compare events continuously toggle the OCx pin 010 = Single Compare Single-Shot mode: Initialize OCx pin high; compare event forces the OCx pin low 001 = Single Compare Single-Shot mode: Initialize OCx pin low; compare event forces the OCx pin high 000 = Output compare channel is disabled

Note 1: The OCx output must also be configured to an available RPn pin. For more information, see **Section 11.4 "Peripheral Pin Select (PPS)"**.

2: The Fault input enable and Fault status bits are valid when OCM<2:0> = 111 or 110.

3: The Comparator 1 output controls the OC1-OC3 channels, Comparator 2 output controls the OC4-OC6 channels, Comparator 3 output controls the OC7-OC9 channels.

4: The OCFA/OCFB Fault inputs must also be configured to an available RPn/RPIn pin. For more information, see **Section 11.4 "Peripheral Pin Select (PPS)"**.

REGISTER 18-2: I2CxCONH: I2Cx CONTROL REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PCIE	SCIE	BOEN	SDAHT(1)	SBCDE	AHEN	DHEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **PCIE:** Stop Condition Interrupt Enable bit (I^2C Slave mode only)
1 = Enables interrupt on detection of Stop condition
0 = Stop detection interrupts are disabled

bit 5 **SCIE:** Start Condition Interrupt Enable bit (I^2C Slave mode only)
1 = Enables interrupt on detection of Start or Restart conditions
0 = Start detection interrupts are disabled

bit 4 **BOEN:** Buffer Overwrite Enable bit (I^2C Slave mode only)
1 = I2CxRCV is updated and an ACK is generated for a received address/data byte, ignoring the state of the I2COV bit only if RBF bit = 0
0 = I2CxRCV is only updated when I2COV is clear

bit 3 **SDAHT:** SDAx Hold Time Selection bit(1)
1 = Minimum of 300 ns hold time on SDAx after the falling edge of SCLx
0 = Minimum of 100 ns hold time on SDAx after the falling edge of SCLx

bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I^2C Slave mode only)
If, on the rising edge of SCLx, SDAx is sampled low when the module is outputting a high state, the BCL bit is set and the bus goes Idle. This Detection mode is only valid during data and ACK transmit sequences.
1 = Enables slave bus collision interrupts
0 = Slave bus collision interrupts are disabled

bit 1 **AHEN:** Address Hold Enable bit (I^2C Slave mode only)
1 = Following the 8th falling edge of SCLx for a matching received address byte; SCLREL bit (I2CxCONL<12>) will be cleared and SCLx will be held low
0 = Address holding is disabled

bit 0 **DHEN:** Data Hold Enable bit (I^2C Slave mode only)
1 = Following the 8th falling edge of SCLx for a received data byte; slave hardware clears the SCLREL bit (I2CxCONL<12>) and SCLx is held low
0 = Data holding is disabled

Note 1: This bit must be set to '0' for 1 MHz operation.

20.7.1 USB OTG MODULE CONTROL REGISTERS

REGISTER 20-3: U1OTGSTAT: USB OTG STATUS REGISTER (HOST MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0, HSC	U-0	R-0, HSC	U-0	R-0, HSC	R-0, HSC	U-0	R-0, HSC
ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD
bit 7							bit 0

Legend:	U = Unimplemented bit, read as ‘0’		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7 **ID:** ID Pin State Indicator bit
1 = No plug is attached or a Type B cable has been plugged into the USB receptacle
0 = A Type A plug has been plugged into the USB receptacle

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **LSTATE:** Line State Stable Indicator bit
1 = The USB line state (as defined by SE0 and JSTATE) has been stable for the previous 1 ms
0 = The USB line state has not been stable for the previous 1 ms

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **SESVD:** Session Valid Indicator bit
1 = The V_{BUS} voltage is above $V_{A\_SESS\_VLD}$ (as defined in the *“USB 2.0 Specification”*) on the A or B-device
0 = The V_{BUS} voltage is below $V_{A\_SESS\_VLD}$ on the A or B-device

bit 2 **SESEND:** B Session End Indicator bit
1 = The V_{BUS} voltage is below $V_{B\_SESS\_END}$ (as defined in the *“USB 2.0 Specification”*) on the B-device
0 = The V_{BUS} voltage is above $V_{B\_SESS\_END}$ on the B-device

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **VBUSVD:** A V_{BUS} Valid Indicator bit
1 = The V_{BUS} voltage is above $V_{A\_VBUS\_VLD}$ (as defined in the *“USB 2.0 Specification”*) on the A-device
0 = The V_{BUS} voltage is below $V_{A\_VBUS\_VLD}$ on the A-device

TABLE 24-1: MODULE-SPECIFIC INPUT DATA SOURCES

Bit Field Value		Input Source			
		CLC1	CLC2	CLC3	CLC4
DS4<2:0>	011	SDI1	SDI2	SDI3	Unimplemented
	001	CLC2 Output	CLC1 Output	CLC4 Output	CLC3 Output
DS3<2:0>	100	U1RX	U2RX	U3RX	U4RX
	011	SDO1	SDO2	SDO3	Unimplemented
	001	CLC1 Output	CLC2 Output	CLC3 Output	CLC4 Output
DS2<2:0>	011	U1TX	U2TX	U3TX	U4TX
	001	CLC2 Output	CLC1 Output	CLC4 Output	CLC3 Output

REGISTER 24-4: CLCxGLSL: CLCx GATE LOGIC INPUT SELECT LOW REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **G2D4T:** Gate 2 Data Source 4 True Enable bit
1 = The Data Source 4 signal is enabled for Gate 2
0 = The Data Source 4 signal is disabled for Gate 2

bit 14 **G2D4N:** Gate 2 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 2
0 = The Data Source 4 inverted signal is disabled for Gate 2

bit 13 **G2D3T:** Gate 2 Data Source 3 True Enable bit
1 = The Data Source 3 signal is enabled for Gate 2
0 = The Data Source 3 signal is disabled for Gate 2

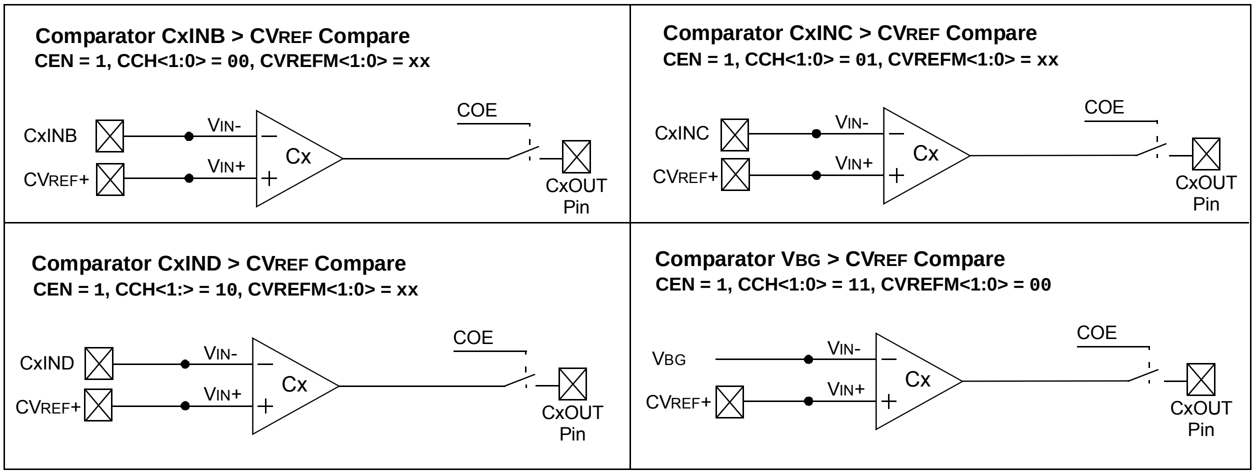
bit 12 **G2D3N:** Gate 2 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 2
0 = The Data Source 3 inverted signal is disabled for Gate 2

bit 11 **G2D2T:** Gate 2 Data Source 2 True Enable bit
1 = The Data Source 2 signal is enabled for Gate 2
0 = The Data Source 2 signal is disabled for Gate 2

bit 10 **G2D2N:** Gate 2 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 2
0 = The Data Source 2 inverted signal is disabled for Gate 2

bit 9 **G2D1T:** Gate 2 Data Source 1 True Enable bit
1 = The Data Source 1 signal is enabled for Gate 2
0 = The Data Source 1 signal is disabled for Gate 2

FIGURE 26-4: INDIVIDUAL COMPARATOR CONFIGURATIONS WHEN CREF = 1 AND CVREFP = 1



28.4 Measuring Die Temperature

The CTMU can be configured to use the A/D to measure the die temperature using dedicated A/D Channel 24. Perform the following steps to measure the diode voltage:

- The internal current source must be set for either 5.5 µA (IRNG<1:0> = 0x2) or 55 µA (IRNG<1:0> = 0x3).
- In order to route the current source to the diode, the EDG1STAT and EDG2STAT bits must be equal (either both '0' or both '1').
- The CTMREQ bit (AD1CON5<13>) must be set to '1'.
- The A/D Channel Select bits must be 24 (0x18) using a single-ended measurement.

The voltage of the diode will vary over temperature according to the graphs shown below (Figure 28-4). Note that the graphs are different, based on the magnitude of the current source selected. The slopes are nearly linear over the range of -40ºC to +100ºC and the temperature can be calculated as follows:

EQUATION 28-2:

For 5.5 µA Current Source:

$$Tdie = \frac{710\ mV - Vdiode}{1.8}$$

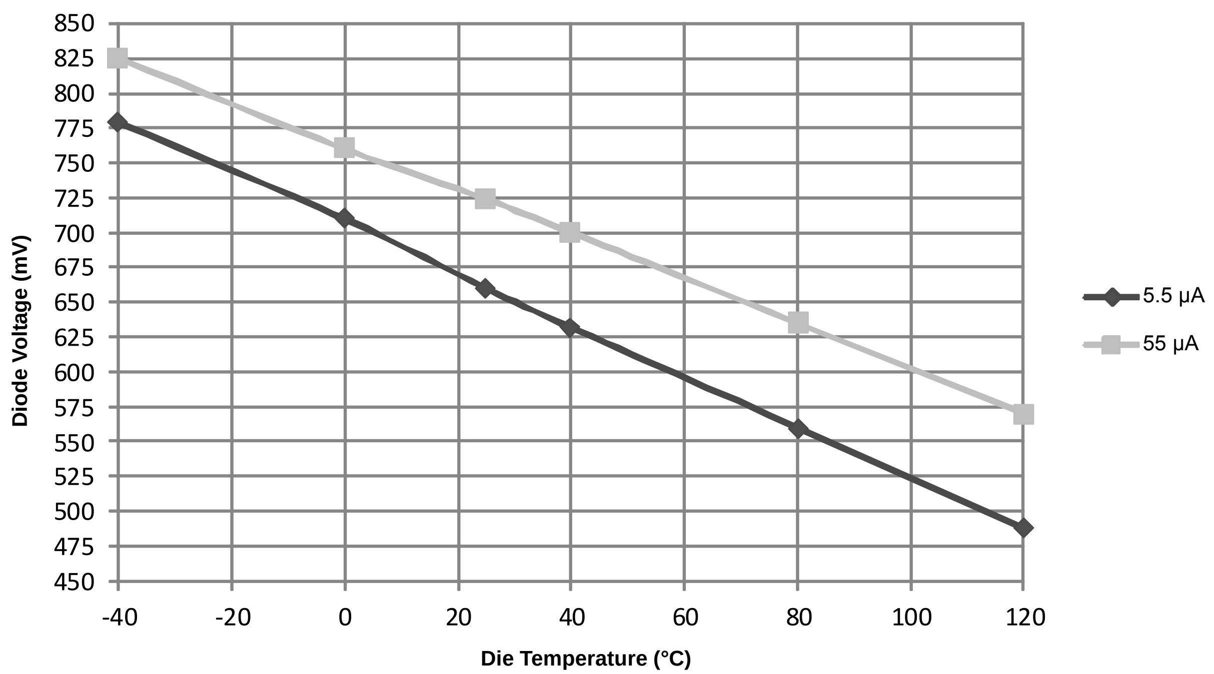
where $Vdiode$ is in mV, $Tdie$ is in ºC

For 55 µA Current Source:

$$Tdie = \frac{760\ mV - Vdiode}{1.55}$$

where $Vdiode$ is in mV, $Tdie$ is in ºC

FIGURE 28-4: DIODE VOLTAGE (mV) vs. DIE TEMPERATURE (TYPICAL)



31.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

31.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

31.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

31.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

31.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

32.0 INSTRUCTION SET SUMMARY

Note:	This chapter is a brief summary of the PIC24F Instruction Set Architecture (ISA) and is not intended to be a comprehensive reference source.

The PIC24F instruction set adds many enhancements to the previous PIC® MCU instruction sets, while maintaining an easy migration from previous PIC MCU instruction sets. Most instructions are a single program memory word. Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction. The instruction set is highly orthogonal and is grouped into four basic categories:

- Word or byte-oriented operations
- Bit-oriented operations
- Literal operations
- Control operations

Table 32-1 shows the general symbols used in describing the instructions. The PIC24F instruction set summary in Table 32-2 lists all the instructions, along with the status flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have three operands:

- The first source operand, which is typically a register, 'Wb', without any address modifier
- The second source operand, which is typically a register, 'Ws', with or without an address modifier
- The destination of the result, which is typically a register, 'Wd', with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- The file register specified by the value, 'f'
- The destination, which could either be the file register, 'f', or the W0 register, which is denoted as 'WREG'

Most bit-oriented instructions (including simple rotate/shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of 'Ws' or 'f')
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register, 'Wb')

The literal instructions that involve data movement may use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by the value of 'k')
- The W register or file register where the literal value is to be loaded (specified by 'Wb' or 'f')

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand, which is a register, 'Wb', without any address modifier
- The second source operand, which is a literal value
- The destination of the result (only if not the same as the first source operand), which is typically a register, 'Wd', with or without an address modifier

The control instructions may use some of the following operands:

- A program memory address
- The mode of the Table Read and Table Write instructions

All instructions are a single word, except for certain double-word instructions, which were made double-word instructions so that all the required information is available in these 48 bits. In the second word, the 8 MSbs are '`0`'s. If this second word is executed as an instruction (by itself), it will execute as a `NOP`.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true or the Program Counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles, with the additional instruction cycle(s) executed as a `NOP`. Notable exceptions are the `BRA` (unconditional/computed branch), indirect `CALL/GOTO`, all Table Reads and Table Writes, and `RETURN/RETFIE` instructions, which are single-word instructions but take two or three cycles.

Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles. The double-word instructions execute in two instruction cycles.

TABLE 33-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
	VIL	**Input Low Voltage(3)**					
DI10		I/O Pins with ST Buffer	VSS	—	0.2 VDD	V	
DI11		I/O Pins with TTL Buffer	VSS	—	0.15 VDD	V	
DI15		$\overline{\text{MCLR}}$	VSS	—	0.2 VDD	V	
DI16		OSCI (XT mode)	VSS	—	0.2 VDD	V	
DI17		OSCI (HS mode)	VSS	—	0.2 VDD	V	
DI18		I/O Pins with I²C Buffer	VSS	—	0.3 VDD	V	
DI19		I/O Pins with SMBus Buffer	VSS	—	0.8	V	SMBus is enabled
	VIH	**Input High Voltage(3)**					
DI20		I/O Pins with ST Buffer: with Analog Functions, Digital Only	 0.8 VDD 0.8 VDD	 — —	 VDD 5.5	 V V	
DI21		I/O Pins with TTL Buffer: with Analog Functions, Digital Only	 0.25 VDD + 0.8 0.25 VDD + 0.8	 — —	 VDD 5.5	 V V	
DI25		$\overline{\text{MCLR}}$	0.8 VDD	—	VDD	V	
DI26		OSCI (XT mode)	0.7 VDD	—	VDD	V	
DI27		OSCI (HS mode)	0.7 VDD	—	VDD	V	
DI28		I/O Pins with I²C Buffer: with Analog Functions, Digital Only	 0.7 VDD 0.7 VDD	 — —	 VDD 5.5	 V V	
DI29		I/O Pins with SMBus Buffer: with Analog Functions, Digital Only	 2.1 2.1	 — —	 VDD 5.5	 V V	 2.5V ≤ VPIN ≤ VDD
DI30	ICNPU	**CNx Pull-up Current**	150		450	μA	VDD = 3.3V, VPIN = VSS
DI30A	ICNPD	**CNx Pull-Down Current**	230		500	μA	VDD = 3.3V, VPIN = VDD
	IIL	**Input Leakage Current(2)**					
DI50		I/O Ports	—	—	±1	μA	VSS ≤ VPIN ≤ VDD, pin at high-impedance
DI51		Analog Input Pins	—	—	±1	μA	VSS ≤ VPIN ≤ VDD, pin at high-impedance
DI55		$\overline{\text{MCLR}}$	—	—	±1	μA	VSS ≤ VPIN ≤ VDD
DI56		OSCI/CLKI	—	—	±1	μA	VSS ≤ VPIN ≤ VDD, EC, XT and HS modes

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Negative current is defined as current sourced by the pin.

3: Refer to Table 1-1 for I/O pin buffer types.

