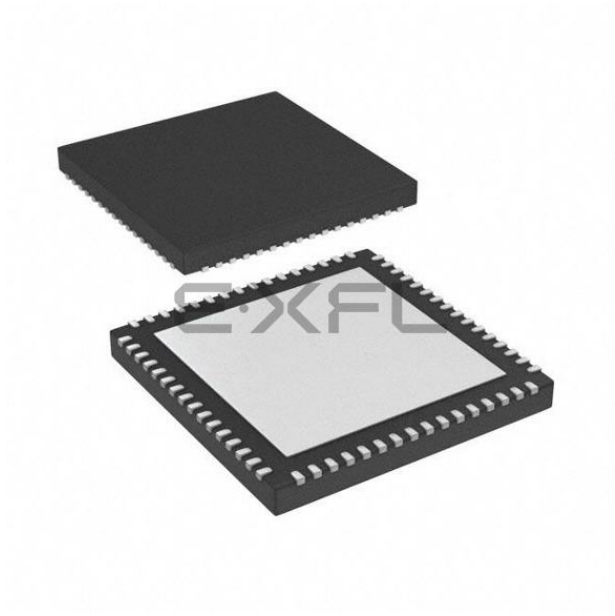
Microchip Technology - PIC24FJ128GA606-I/MR Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, HLVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128ga606-i-mr

TABLE 6: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJXXXGA610 BGA) (CONTINUED)

Pin	Full Pin Name	Pin	Full Pin Name
J1	AN3/C2INA/RB3	K7	AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/RB14
J2	AN2/CTCMP/C2INB/**RP13**/CTED13/RB2	K8	VDD
J3	PGED2/AN7/**RP7**/U6TX/RB7	K9	**RP5**/RD15
J4	AVDD	K10	**RP16**/RF3
J5	AN11/REFI/PMA12/RB11	K11	**RP30**/RF2
J6	TCK/RA1	L1	PGEC2/AN6/**RP6**/RB6
J7	AN12/U6RX/CTED2/PMA11/RB12	L2	CVREF-/VREF-/PMA7/RA9
J8	N/C	L3	AVSS
J9	N/C	L4	AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/RB9
J10	**RP15**/RF8	L5	CVREF/AN10/PMA13/RB10
J11	SDA1/RG3	L6	**RP31**/RF13
K1	PGEC1/ALTCVREF-/ALTVREF-/AN1/**RP1**/CTED12/RB1	L7	AN13/CTED1/PMA10/RB13
K2	PGED1/ALTCVREF+/ALTVREF+/AN0/**RP0**/RB0	L8	AN15/**RP29**/CTED6/PMA0/PMALL/RB15
K3	CVREF+/VREF+/PMA6/RA10	L9	**RPI43**/RD14
K4	AN8/**RP8**/PWRGT/RB8	L10	**RP10**/PMA9/RF4
K5	N/C	L11	**RP17**/PMA8/RF5
K6	**RPI32**/CTED7/PMA18/RF12		

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT MICROCONTROLLERS

2.1 Basic Connection Requirements

Getting started with the PIC24FJ1024GA610/GB610 family of 16-bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development.

The following pins must always be connected:

- All VDD and VSS pins
  (see **Section 2.2 "Power Supply Pins"**)
- The USB transceiver supply, VUSB3V3, regardless of whether or not the USB module is used
  (see **Section 2.2 "Power Supply Pins"**)
- All AVDD and AVSS pins, regardless of whether or not the analog device features are used
  (see **Section 2.2 "Power Supply Pins"**)
- $\overline{\text{MCLR}}$ pin
  (see **Section 2.3 "Master Clear (MCLR) Pin"**)
- VCAP pin (PIC24F J devices only)
  (see **Section 2.4 "Voltage Regulator Pin (VCAP)"**)

These pins must also be connected if they are being used in the end application:

- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes
  (see **Section 2.5 "ICSP Pins"**)
- OSCI and OSCO pins when an external oscillator source is used
  (see **Section 2.6 "External Oscillator Pins"**)

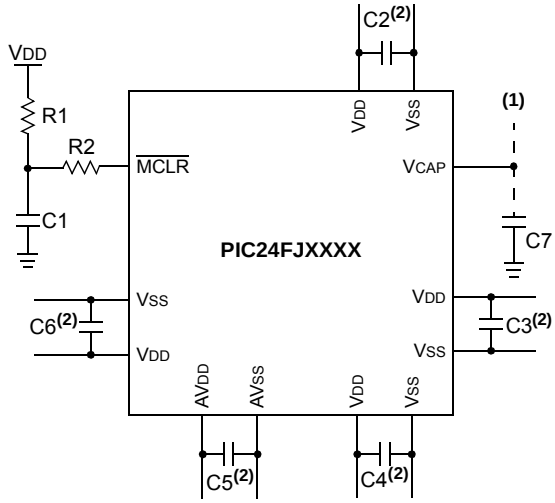
Additionally, the following pins may be required:

- VREF+/VREF- pins used when external voltage reference for analog modules is implemented

Note:	The AVDD and AVSS pins must always be connected, regardless of whether any of the analog modules are being used.

The minimum mandatory connections are shown in Figure 2-1.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTIONS



Key (all values are recommendations):

C1 through C6: 0.1 μF, 50V ceramic

C7: 10 μF, 16V or greater, ceramic

R1: 10 kΩ

R2: 100Ω to 470Ω

Note 1: See **Section 2.4 "Voltage Regulator Pin (VCAP)"** for an explanation of voltage regulator pin connections.

2: The example shown is for a PIC24F device with five VDD/VSS and AVDD/AVSS pairs. Other devices may have more or less pairs; adjust the number of decoupling capacitors appropriately.

2.2 Power Supply Pins

2.2.1 DECOUPLING CAPACITORS

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS, is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A 0.1 μF (100 nF), 16V-50V capacitor is recommended. The capacitor should be a low-ESR device with a self-resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF. Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1 μF in parallel with 0.001 μF).
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

2.2.2 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including microcontrollers to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μF to 47 μF.

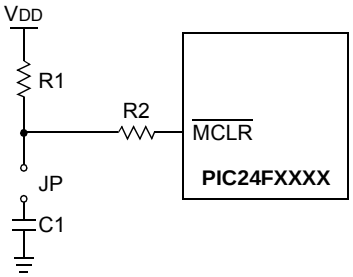
2.3 Master Clear ($\overline{MCLR}$) Pin

The $\overline{MCLR}$ pin provides two specific device functions: device Reset, and device programming and debugging. If programming and debugging are not required in the end application, a direct connection to VDD may be all that is required. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{MCLR}$ pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R1 and C1 will need to be adjusted based on the application and PCB requirements. For example, it is recommended that the capacitor, C1, be isolated from the $\overline{MCLR}$ pin during programming and debugging operations by using a jumper (Figure 2-2). The jumper is replaced for normal run-time operations.

Any components associated with the $\overline{MCLR}$ pin should be placed within 0.25 inch (6 mm) of the pin.

FIGURE 2-2: EXAMPLE OF $\overline{MCLR}$ PIN CONNECTIONS



Note 1: R1 ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the $\overline{MCLR}$ pin VIH and VIL specifications are met.

2: R2 ≤ 470Ω will limit any current flowing into $\overline{MCLR}$ from the external capacitor, C, in the event of a $\overline{MCLR}$ pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the $\overline{MCLR}$ pin VIH and VIL specifications are met.

TABLE 4-7: SFR MAP: 0300h BLOCK

File Name	Address	All Resets	File Name	Address	All Resets
SINGLE OUTPUT CAPTURE/COMPARE/PWM			**SINGLE OUTPUT CAPTURE/COMPARE/PWM (CONTINUED)**		
CCP4CON1L	0300	0000	CCP6STATH	0356	0000
CCP4CON1H	0302	0000	CCP6TMRL	0358	0000
CCP4CON2L	0304	0000	CCP6TMRH	035A	0000
CCP4CON2H	0306	0100	CCP6PRL	035C	FFFF
CCP4CON3L	0308	0000	CCP6PRH	035E	FFFF
CCP4CON3H	030A	0000	CCP6RAL	0360	0000
CCP4STATL	030C	00x0	CCP6RAH	0362	0000
CCP4STATH	030E	0000	CCP6RBL	0364	0000
CCP4TMRL	0310	0000	CCP6RBH	0366	0000
CCP4TMRH	0312	0000	CCP6BUFL	0368	0000
CCP4PRL	0314	FFFF	CCP6BUFH	036A	0000
CCP4PRH	0316	FFFF	CCP7CON1L	036C	0000
CCP4RAL	0318	0000	CCP7CON1H	036E	0000
CCP4RAH	031A	0000	CCP7CON2L	0370	0000
CCP4RBL	031C	0000	CCP7CON2H	0372	0100
CCP4RBH	031E	0000	CCP7CON3L	0374	0000
CCP4BUFL	0320	0000	CCP7CON3H	0376	0000
CCP4BUFH	0322	0000	CCP7STATL	0378	00x0
CCP5CON1L	0324	0000	CCP7STATH	037A	0000
CCP5CON1H	0326	0000	CCP7TMRL	037C	0000
CCP5CON2L	0328	0000	CCP7TMRH	037E	0000
CCP5CON2H	032A	0100	CCP7PRL	0380	FFFF
CCP5CON3L	032C	0000	CCP7PRH	0382	FFFF
CCP5CON3H	032E	0000	CCP7RAL	0384	0000
CCP5STATL	0330	00x0	CCP7RAH	0386	0000
CCP5STATH	0332	0000	CCP7RBL	0388	0000
CCP5TMRL	0334	0000	CCP7RBH	038A	0000
CCP5TMRH	0336	0000	CCP7BUFL	038C	0000
CCP5PRL	0338	FFFF	CCP7BUFH	038E	0000
CCP5PRH	033A	FFFF	**UART**		
CCP5RAL	033C	0000	U1MODE	0398	0000
CCP5RAH	033E	0000	U1STA	039A	0110
CCP5RBL	0340	0000	U1TXREG	039C	x0xx
CCP5RBH	0342	0000	U1RXREG	039E	0000
CCP5BUFL	0344	0000	U1BRG	03A0	0000
CCP5BUFH	0346	0000	U1ADMD	03A2	0000
CCP6CON1L	0348	0000	U2MODE	03AE	0000
CCP6CON1H	034A	0000	U2STA	03B0	0110
CCP6CON2L	034C	0000	U2TXREG	03B2	xxxx
CCP6CON2H	034E	0100	U2RXREG	03B4	0000
CCP6CON3L	0350	0000	U2BRG	03B6	0000
CCP6CON3H	0352	0000	U2ADMD	03B8	0000
CCP6STATL	0354	00x0	U3MODE	03C4	0000

Legend: — = unimplemented, read as '0'; x = undefined. Reset values are shown in hexadecimal.

9.6 PLL Oscillator Modes and USB Operation

The PLL block, shown in Figure 9-2, can generate a wide range of clocks used for both parts with USB functionality (PIC24FJ1024GB610 family) and non-USB functionality (PIC24FJ1024GA610 family). All of the available PLL modes are available for both families whether or nor USB is enabled or present.

The PLL input clock source (FRC or POSC) is controlled by the COSC<2:0> bits (OSCCON<14:12>) if the PLL output is used as a system clock. When COSC<2:0> = 001 (FRCPLL), the PLL is clocked from FRC, and when COSC<2:0> = 011 (PRIPLL), the Primary Oscillator (POSC) is connected to the PLL. The default COSC<2:0> value is selected by the FNOSC<2:0> Configuration bits (FOSCSEL<2:0>). Also, REFO can use the PLL when it is not selected for the system clock (COSC<2:0> bits (OSCCON<14:12>) are not '001' or '011'). In this case, the PLL clock source is selected by the PLLSS Configuration bit (FOSC<4>). If PLLSS is cleared ('0'), the PLL is fed by the FRC Oscillator. If the PLLSS Configuration bit is not programmed ('1'), the PLL is clocked from the Primary Oscillator.

When used in a USB application, the 48 MHz internal clock must be running at all times which requires the VCO of the PLL to run at 96 MHz. This, in turn, forces the system clock (that drives the CPU and peripherals) to route the 96 MHz through a fixed divide-by-3 block (generating 32 MHz) and then through a selection of four fixed divisors ('postscaler'). The postscaler output becomes the system clock.

The input to the PLL must be 4 MHz when used in a USB application, which restricts the frequency input sources to be used with a small set of fixed frequency dividers (see Figure 9-2). For example, if a 12 MHz crystal is used, the PLLMODE<3:0> Configuration bits must be set for divide-by-3 to generate the required 4 MHz. A popular baud rate crystal is 11.0592 MHz, but this value cannot be used for USB operation as there are no divisors available to generate 4 MHz exactly. See Table 9-3 for the possible combinations of input clock and PLLMODE<3:0> bits settings for USB operation.

Non-USB operation allows a wider range of PLL input frequencies. The multiplier ratios can be selected as 4x, 6x or 8x and there is no clock prescaler. The postscaler (CPDIV<1:0>) is available and can be used to reduce the system clock to meet the 32 MHz maximum specification. Note that the minimum input frequency to the PLL is 2 MHz, but the range is 2 MHz to 8 MHz. Therefore, it is possible to select a multiplier ratio that exceeds the 32 MHz maximum specification for the system clock. This allows the system clock to be any frequency between 8 MHz (2 MHz input clock with 4x multiplier ratio) and 32 MHz (4 MHz input clock with 8x multiplier ratio). For example, a common crystal frequency is 3.58 MHz ('color burst') and this can be used with the 6x multiplier to generate a system clock of 21.48 MHz. The VCO frequency becomes the system clock.

Note 1: The maximum operating frequency of the system clock is 32 MHz. It is up to the user to select the proper multiplier ratio with the selected clock source frequency.

The PLL block is shown in Figure 9-2. In this system, the PLL input is divided down by a PLL prescaler to generate a 4 MHz output. This is used to drive an on-chip, 96 MHz PLL frequency multiplier to drive the two clock branches. One branch uses a fixed, divide-by-2 frequency divider to generate the 48 MHz USB clock. The other branch uses a fixed, divide-by-3 frequency divider and configurable PLL prescaler/divider to generate a range of system clock frequencies. The CPDIV<1:0> bits select the system clock speed. The available clock options are listed in Table 9-2.

The USB PLL prescaler must be configured to generate the required 4 MHz VCO input using the PLLMODE<3:0> Configuration bits. This limits the choices for the PLL source frequency to a total of 8 possibilities, as shown in Table 9-3.

TABLE 9-2: SYSTEM CLOCK OPTIONS DURING USB OPERATION

Clock Division (CPDIV<1:0>)	Microcontroller Oscillator Clock Frequency (Fosc)
None (00)	32 MHz
÷2 (01)	16 MHz
÷4 (10)(1)	8 MHz
÷8 (11)(1)	4 MHz

Note 1: System clock frequencies below 16 MHz are too slow to allow USB operation. The USB module must be disabled to use this option. See **Section 9.6.1 "Considerations for USB Operation"**.

TABLE 9-3: VALID PRIMARY OSCILLATOR CONFIGURATIONS FOR USB OPERATIONS(1)

PLL Input Frequency	Clock Mode	PLL Mode (PLLMODE<3:0>)
48 MHz	EC	÷12 (0111)
32 MHz	HS, EC	÷8 (0110)
24 MHz	HS, EC	÷6 (0101)
20 MHz	HS, EC	÷5 (0100)
16 MHz	HS, EC	÷4 (0011)
12 MHz	HS, EC	÷3 (0010)
8 MHz	EC, XT, FRC(2)	÷2 (0001)
4 MHz	EC, XT	÷1 (0000)

Note 1: USB operation restricts the VCO input frequency to be 4 MHz.

2: This requires the use of the FRC self-tune feature to maintain the required clock accuracy.

REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
T5MD	T4MD	T3MD	T2MD	T1MD	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	—	ADC1MD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **T5MD:** Timer5 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 14 **T4MD:** Timer4 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 13 **T3MD:** Timer3 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 12 **T2MD:** Timer2 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 11 **T1MD:** Timer1 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 10-8 **Unimplemented:** Read as '0'

bit 7 **I2C1MD:** I2C1 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 6 **U2MD:** UART2 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 5 **U1MD:** UART1 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 4 **SPI2MD:** SPI2 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 3 **SPI1MD:** SPI1 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **ADC1MD:** A/D Converter Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

REGISTER 11-5: ANSE: PORTE ANALOG FUNCTION SELECTION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-1	U-0
—	—	—	—	—	—	ANSE9(1)	—
bit 15							bit 8

U-0	U-0	U-0	R/W-1	U-0	U-0	U-0	U-0
—	—	—	ANSE4	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9 **ANSE9:** PORTE Analog Function Selection bit(1)
1 = Pin is configured in Analog mode; I/O port read is disabled
0 = Pin is configured in Digital mode; I/O port read is enabled

bit 8-5 **Unimplemented:** Read as '0'

bit 4 **ANSE4:** PORTE Analog Function Selection bit
1 = Pin is configured in Analog mode; I/O port read is disabled
0 = Pin is configured in Digital mode; I/O port read is enabled

bit 3-0 **Unimplemented:** Read as '0'

Note 1: ANSE9 is not available on 64-pin devices.

REGISTER 11-6: ANSG: PORTG ANALOG FUNCTION SELECTION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-1
—	—	—	—	—	—	ANSG<9:8>	
bit 15							bit 8

R/W-1	R/W-1	U-0	U-0	U-0	U-0	U-0	U-0
ANSG<7:6>		—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9-6 **ANSG<9:6>:** PORTG Analog Function Selection bits
1 = Pin is configured in Analog mode; I/O port read is disabled
0 = Pin is configured in Digital mode; I/O port read is enabled

bit 5-0 **Unimplemented:** Read as '0'

11.3 Interrupt-on-Change (IOC)

The Interrupt-on-Change function of the I/O ports allows the PIC24FJ1024GA610/GB610 family of devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature is capable of detecting input Change-of-States, even in Sleep mode when the clocks are disabled.

Interrupt-on-Change functionality is enabled on a pin by setting the IOCPx and/or IOCNx register bit for that pin. For example, PORTC has register names, IOCPC and IOCNC, for these functions. Setting a value of '1' in the IOCPx register enables interrupts for low-to-high transitions, while setting a value of '1' in the IOCNx register enables interrupts for high-to-low transitions. Setting a value of '1' in both register bits will enable interrupts for either case (e.g., a pulse on the pin will generate two interrupts). In order for any IOC to be detected, the global IOC Interrupt Enable bit (IEC1<3>) must be set, the IOCON bit (PADCON<15>) set and the associated IFSx flag cleared.

When an interrupt request is generated for a pin, the corresponding status flag (IOCFx register bit) will be set, indicating that a Change-of-State occurred on that pin. The IOCFx register bit will remain set until cleared by writing a zero to it. When any IOCFx flag bit in a given port is set, the corresponding IOCPxF bit in the IOCSTAT register will be set. This flag indicates that a change was detected on one of the bits on the given port. The IOCPxF flag will be cleared when all IOCFx<15:0> bits are cleared.

Multiple individual status flags can be cleared by writing a zero to one or more bits using a Read-Modify-Write operation. If another edge is detected on a pin whose status bit is being cleared during the Read-Modify-Write sequence, the associated change flag will still be set at the end of the Read-Modify-Write sequence.

The user should use the instruction sequence (or equivalent) shown in Example 11-1 to clear the Interrupt-on-Change Status registers.

At the end of this sequence, the W0 register will contain a zero for each bit for which the port pin had a change detected. In this way, any indication of a pin changing will not be lost.

Due to the asynchronous and real-time nature of the Interrupt-on-Change, the value read on the port pins may not indicate the state of the port when the change was detected, as a second change can occur during the interval between clearing the flag and reading the port. It is up to the user code to handle this case if it is a possibility in their application. To keep this interval to a minimum, it is recommended that any code modifying the IOCFx registers be run either in the interrupt handler or with interrupts disabled.

Each Interrupt-on-Change (IOC) pin has both a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source connected to the pin, while the pull-downs act as a current sink connected to the pin. These eliminate the need for external resistors when push button or keypad devices are connected.

The pull-ups and pull-downs are separately enabled using the IOCPUx registers (for pull-ups) and the IOCPDx registers (for pull-downs). Each IOC pin has individual control bits for its pull-up and pull-down. Setting a control bit enables the weak pull-up or pull-down for the corresponding pin.

Note:	Pull-ups and pull-downs on pins should always be disabled whenever the pin is configured as a digital output.

EXAMPLE 11-1: IOC STATUS READ/CLEAR IN ASSEMBLY

```
MOV   0xFFFF, W0   ; Initial mask value 0xFFFF -> W0
XOR   IOCFx, W0    ; W0 has '1' for each bit set in IOCFx
AND   IOCFx        ; IOCFx & W0 ->IOCFx
```

EXAMPLE 11-2: PORT READ/WRITE IN ASSEMBLY

```
MOV   0xFF00, W0   ; Configure PORTB<15:8> as inputs
MOV   W0, TRISB    ; and PORTB<7:0> as outputs
NOP                ; Delay 1 cycle
BTSS  PORTB, #13   ; Next Instruction
```

EXAMPLE 11-3: PORT READ/WRITE IN 'C'

```
TRISB = 0xFF00;              // Configure PORTB<15:8> as inputs and PORTB<7:0> as outputs
Nop();                       // Delay 1 cycle
If (PORTBbits.RB13){ };      // Test if RB13 is a '1'
```

11.4.3.2 Output Mapping

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Each register contains two 6-bit fields, with each field being associated with one RPn pin (see Register 11-36 through Register 11-51). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 11-4).

Because of the mapping technique, the list of peripherals for output mapping also includes a null value of '000000'. This permits any given pin to remain disconnected from the output of any of the pin-selectable peripherals.

TABLE 11-4: SELECTABLE OUTPUT SOURCES (MAPS FUNCTION TO OUTPUT)

Output Function Number	Function	Output Name
0	None (Pin Disabled)	
1	C1OUT	Comparator 1 Output
2	C2OUT	Comparator 2 Output
3	U1TX	UART1 Transmit
4	$\overline{\text{U1RTS}}$	UART1 Request-to-Send
5	U2TX	UART2 Transmit
6	$\overline{\text{U2RTS}}$	UART2 Request-to-Send
7	SDO1	SPI1 Data Output
8	SCK1OUT	SPI1 Clock Output
9	SS1OUT	SPI1 Slave Select Output
10	SDO2	SPI2 Data Output
11	SCK2OUT	SPI2 Clock Output
12	SS2OUT	SPI2 Slave Select Output
13	OC1	Output Compare 1
14	OC2	Output Compare 2
15	OC3	Output Compare 3
16	OCM4	CCP4 Output Compare
17	OCM5	CCP5 Output Compare
18	OCM6	CCP6 Output Compare
19	U3TX	UART3 Transmit
20	$\overline{\text{U3RTS}}$	UART3 Request-to-Send
21	U4TX	UART4 Transmit
22	$\overline{\text{U4RTS}}$	UART4 Request-to-Send
23	SDO3	SPI3 Data Output
24	SCK3OUT	SPI3 Clock Output
25	SS3OUT	SPI3 Slave Select Output
26	C3OUT	Comparator 3 Output
27	OCM7	CCP7 Output Compare
28	REFO	Reference Clock Output
29	CLC1OUT	CLC1 Output
30	CLC2OUT	CLC2 Output
31	RTCC	RTCC Output

REGISTER 13-1: TxCON: TIMER2 AND TIMER4 CONTROL REGISTER(1)

R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
TON	—	TSIDL	—	—	—	TECS1(2)	TECS0(2)
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
—	TGATE	TCKPS1	TCKPS0	T32(3,4)	—	TCS(2)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timerx On bit
When TxCON<3> = 1:
1 = Starts 32-bit Timerx/y
0 = Stops 32-bit Timerx/y
When TxCON<3> = 0:
1 = Starts 16-bit Timerx
0 = Stops 16-bit Timerx

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timerx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9-8 **TECS<1:0>:** Timerx Extended Clock Source Select bits (selected when TCS = 1)(2)
When TCS = 1:
11 = Generic timer (TxCK) external input
10 = LPRC Oscillator
01 = TyCK external clock input
00 = SOSC
When TCS = 0:
These bits are ignored; the timer is clocked from the internal system clock (FOSC/2).

bit 7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timerx Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timerx Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

Note 1: Changing the value of TxCON while the timer is running (TON = 1) causes the timer prescale counter to reset and is not recommended.

2: If TCS = 1 and TECS<1:0> = x1, the selected external timer input (TxCK or TyCK) must be configured to an available RPn/RPIn pin. For more information, see **Section 11.4 "Peripheral Pin Select (PPS)"**.

3: In 32-bit mode, the T3CON or T5CON control bits do not affect 32-bit timer operation.

4: This bit is labeled T45 in the T4CON register.

NOTES:

REGISTER 20-2: BDnSTAT: BUFFER DESCRIPTOR n STATUS REGISTER PROTOTYPE, CPU MODE (BD0STAT THROUGH BD63STAT)

R/W-x	R/W-x	r-0	r-0	R/W-x	R/W-x	R/W-x, HSC	R/W-x, HSC
UOWN	DTS(1)	—	—	DTSEN	BSTALL	BC9	BC8
bit 15							bit 8

R/W-x, HSC	R/W-x, HSC	R/W-x, HSC	R/W-x, HSC	R/W-x, HSC	R/W-x, HSC	R/W-x, HSC	R/W-x, HSC
BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0
bit 7							bit 0

Legend:	r = Reserved bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'r' = Reserved bit	x = Bit is unknown

bit 15 **UOWN:** USB Own bit
- 0 = The microcontroller core owns the BD and its corresponding buffer; the USB module ignores all other fields in the BD

bit 14 **DTS:** Data Toggle Packet bit(1)
- 1 = Data 1 packet
- 0 = Data 0 packet

bit 13-12 **Reserved:** Maintain as '0'

bit 11 **DTSEN:** Data Toggle Synchronization Enable bit
- 1 = Data toggle synchronization is enabled; data packets with incorrect Sync value will be ignored
- 0 = No data toggle synchronization is performed

bit 10 **BSTALL:** Buffer STALL Enable bit
- 1 = Buffer STALL is enabled; STALL handshake issued if a token is received that would use the BD in the given location (UOWN bit remains set, BD value is unchanged); corresponding EPSTALL bit will get set on any STALL handshake
- 0 = Buffer STALL is disabled

bit 9-0 **BC<9:0>:** Byte Count bits

This represents the number of bytes to be transmitted or the maximum number of bytes to be received during a transfer. Upon completion, the byte count is updated by the USB module with the actual number of bytes transmitted or received.

Note 1: This bit is ignored unless DTSEN = 1.

REGISTER 20-6: U1STAT: USB STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	U-0	U-0
ENDPT3	ENDPT2	ENDPT1	ENDPT0	DIR	PPBI(1)	—	—
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-4 **ENDPT<3:0>:** Number of the Last Endpoint Activity bits
(Represents the number of the BDT updated by the last USB transfer.)
1111 = Endpoint 15
1110 = Endpoint 14
•
•
•
0001 = Endpoint 1
0000 = Endpoint 0

bit 3 **DIR:** Last BD Direction Indicator bit
1 = The last transaction was a transmit transfer (TX)
0 = The last transaction was a receive transfer (RX)

bit 2 **PPBI:** Ping-Pong BD Pointer Indicator bit(1)
1 = The last transaction was to the odd BD bank
0 = The last transaction was to the even BD bank

bit 1-0 **Unimplemented:** Read as '0'

Note 1: This bit is only valid for endpoints with available even and odd BD registers.

REGISTER 20-9: U1ADDR: USB ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LSPDEN(1)	DEVADDR6	DEVADDR5	DEVADDR4	DEVADDR3	DEVADDR2	DEVADDR1	DEVADDR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **LSPDEN:** Low-Speed Enable Indicator bit(1)
1 = USB module operates at low speed
0 = USB module operates at full speed

bit 6-0 **DEVADDR<6:0>:** USB Device Address bits

Note 1: Host mode only. In Device mode, this bit is unimplemented and read as '0'.

REGISTER 20-10: U1TOK: USB TOKEN REGISTER (HOST MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PID3	PID2	PID1	PID0	EP3	EP2	EP1	EP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-4 **PID<3:0>:** Token Type Identifier bits
1101 = SETUP (TX) token type transaction(1)
1001 = IN (RX) token type transaction(1)
0001 = OUT (TX) token type transaction(1)

bit 3-0 **EP<3:0>:** Token Command Endpoint Address bits
This value must specify a valid endpoint on the attached device.

Note 1: All other combinations are reserved and are not to be used.

REGISTER 20-12: U1CNFG1: USB CONFIGURATION REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
UTEYE	UOEMON(1)	—	USBSIDL	—	—	PPB1	PPB0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **UTEYE:** USB Eye Pattern Test Enable bit
- 1 = Eye pattern test is enabled
- 0 = Eye pattern test is disabled

bit 6 **UOEMON:** USB $\overline{OE}$ Monitor Enable bit(1)
- 1 = $\overline{OE}$ signal is active; it indicates intervals during which the D+/D- lines are driving
- 0 = $\overline{OE}$ signal is inactive

bit 5 **Unimplemented:** Read as '0'

bit 4 **USBSIDL:** USB OTG Stop in Idle Mode bit
- 1 = Discontinues module operation when the device enters Idle mode
- 0 = Continues module operation in Idle mode

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **PPB<1:0>:** Ping-Pong Buffers Configuration bits
- 11 = Even/Odd Ping-Pong Buffers are enabled for Endpoints 1 to 15
- 10 = Even/Odd Ping-Pong Buffers are enabled for all endpoints
- 01 = Even/Odd Ping-Pong Buffers are enabled for RX Endpoint 0
- 00 = Even/Odd Ping-Pong Buffers are disabled

Note 1: This bit is only active when the UTRDIS bit (U1CNFG2<0>) is set.

REGISTER 20-17: U1IR: USB INTERRUPT STATUS REGISTER (HOST MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS	R/K-0, HS
STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	DETACHIF
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	K = Write '1' to Clear bit	HS = Hardware Settable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **STALLIF:** STALL Handshake Interrupt bit
- 1 = A STALL handshake was sent by the peripheral device during the handshake phase of the transaction in Device mode
- 0 = A STALL handshake has not been sent

bit 6 **ATTACHIF:** Peripheral Attach Interrupt bit
- 1 = A peripheral attachment has been detected by the module; it is set if the bus state is not SE0 and there has been no bus activity for 2.5 μs
- 0 = No peripheral attachment has been detected

bit 5 **RESUMEIF:** Resume Interrupt bit
- 1 = A K-state is observed on the D+ or D- pin for 2.5 μs (differential '1' for low speed, differential '0' for full speed)
- 0 = No K-state is observed

bit 4 **IDLEIF:** Idle Detect Interrupt bit
- 1 = Idle condition is detected (constant Idle state of 3 ms or more)
- 0 = No Idle condition is detected

bit 3 **TRNIF:** Token Processing Complete Interrupt bit
- 1 = Processing of the current token is complete; read the U1STAT register for endpoint information
- 0 = Processing of the current token is not complete; clear the U1STAT register or load the next token from U1STAT

bit 2 **SOFIF:** Start-of-Frame Token Interrupt bit
- 1 = A Start-of-Frame token is received by the peripheral or the Start-of-Frame threshold is reached by the host
- 0 = No Start-of-Frame token is received or threshold reached

bit 1 **UERRIF:** USB Error Condition Interrupt bit
- 1 = An unmasked error condition has occurred; only error states enabled in the U1EIE register can set this bit
- 0 = No unmasked error condition has occurred

bit 0 **DETACHIF:** Detach Interrupt bit
- 1 = A peripheral detachment has been detected by the module; Reset state must be cleared before this bit can be re-asserted
- 0 = No peripheral detachment is detected. Individual bits can only be cleared by writing a '1' to the bit position as part of a word write operation on the entire register. Using Boolean instructions or bitwise operations to write to a single bit position will cause all set bits, at the moment of the write, to become cleared.

Note: Individual bits can only be cleared by writing a '1' to the bit position as part of a word write operation on the entire register. Using Boolean instructions or bitwise operations to write to a single bit position will cause all set bits, at the moment of the write, to become cleared.

REGISTER 25-3: AD1CON3: A/D CONTROL REGISTER 3

R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC(1)	EXTSAM	PUMPEN(2)	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ADRC:** A/D Conversion Clock Source bit(1)
1 = Dedicated ADC RC clock generator (4 MHz nominal)
0 = Clock derived from system clock

bit 14 **EXTSAM:** Extended Sampling Time bit
1 = A/D is still sampling after SAMP = 0
0 = A/D is finished sampling

bit 13 **PUMPEN:** Charge Pump Enable bit(2)
1 = Charge pump for switches is enabled
0 = Charge pump for switches is disabled

bit 12-8 **SAMC<4:0>:** Auto-Sample Time Select bits
11111 = 31 TAD
• • •
00001 = 1 TAD
00000 = 0 TAD

bit 7-0 **ADCS<7:0>:** A/D Conversion Clock Select bits
11111111 = 256 • TCY = TAD
• • •
00000001 = 2 • TCY = TAD
00000000 = TCY = TAD

Note 1: Selecting the internal ADC RC clock requires that ADCSx be '1' or greater. Setting ADCSx = 0 when ADRC = 1 will violate the TAD (min) specification.

2: Enable the charge pump if AVDD is < 2.7V. Longer sample times are required due to the increase of the internal resistance of the MUX if the charge pump is disabled.

REGISTER 26-1: CMxCON: COMPARATOR x CONTROL REGISTERS (COMPARATORS 1 THROUGH 3)

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0, HS	R-0, HSC
CEN	COE	CPOL	—	—	—	CEVT	COUT
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0
bit 7							bit 0

Legend:	HS = Hardware Settable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CEN:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 14 **COE:** Comparator Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **CEVT:** Comparator Event bit
1 = Comparator event that is defined by EVPOL<1:0> has occurred; subsequent Triggers and interrupts are disabled until the bit is cleared
0 = Comparator event has not occurred

bit 8 **COUT:** Comparator Output bit
When CPOL = 0:
1 = $V_{IN+} > V_{IN-}$
0 = $V_{IN+} < V_{IN-}$
When CPOL = 1:
1 = $V_{IN+} < V_{IN-}$
0 = $V_{IN+} > V_{IN-}$

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits
11 = Trigger/event/interrupt is generated on any change of the comparator output (while CEVT = 0)
10 = Trigger/event/interrupt is generated on transition of the comparator output:
If CPOL = 0 (non-inverted polarity):
High-to-low transition only.
If CPOL = 1 (inverted polarity):
Low-to-high transition only.
01 = Trigger/event/interrupt is generated on transition of comparator output:
If CPOL = 0 (non-inverted polarity):
Low-to-high transition only.
If CPOL = 1 (inverted polarity):
High-to-low transition only.
00 = Trigger/event/interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

TABLE 33-7: DC CHARACTERISTICS: Δ CURRENT (BOR, WDT, HLVD, RTCC)(3)

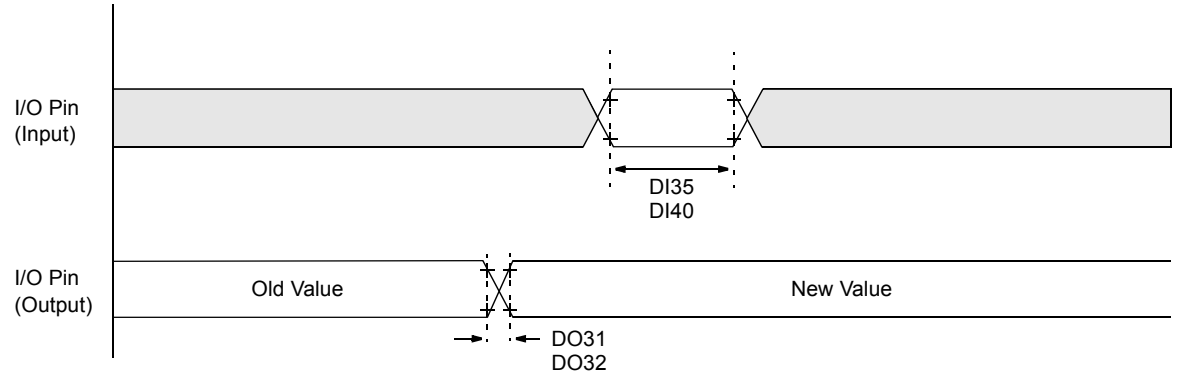
DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Operating Temperature**	**VDD**	**Conditions**
Incremental Current Brown-out Reset (ΔBOR)(2)						
DC25	3	5	μA	-40°C to +85°C	2.0V	ΔBOR(2)
	4	5	μA	-40°C to +85°C	3.3V	
Incremental Current Watchdog Timer (ΔWDT)(2)						
DC71	0.22	1	μA	-40°C to +85°C	2.0V	ΔWDT(2)
	0.3	1	μA	-40°C to +85°C	3.3V	
Incremental Current High/Low-Voltage Detect (ΔHLVD)(2)						
DC75	1.3	5	μA	-40°C to +85°C	2.0V	ΔHLVD(2)
	1.9	5	μA	-40°C to +85°C	3.3V	
Incremental Current Real-Time Clock and Calendar (ΔRTCC)(2)						
DC77	1.1	2	μA	-40°C to +85°C	2.0V	ΔRTCC (with SOSC enabled in Low-Power mode)(2)
	1.2	2.2	μA	-40°C to +85°C	3.3V	
DC77A	0.35	1	μA	-40°C to +85°C	2.0V	ΔRTCC (with LPRC enabled)(2)
	0.45	1	μA	-40°C to +85°C	3.3V	

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Incremental current while the module is enabled and running.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current. The current includes the selected clock source enabled for WDT and RTCC.

FIGURE 33-4: CLKO AND I/O TIMING CHARACTERISTICS



Note: Refer to Figure 33-2 for load conditions.

TABLE 33-23: CLKO AND I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			**Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
DO31	TIOR	Port Output Rise Time	—	10	25	ns	
DO32	TIOF	Port Output Fall Time	—	10	25	ns	
DI35	TINP	INTx Pin High or Low Time (input)	1	—	—	TCY	
DI40	TRBP	CNx High or Low Time (input)	1	—	—	TCY	

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated.