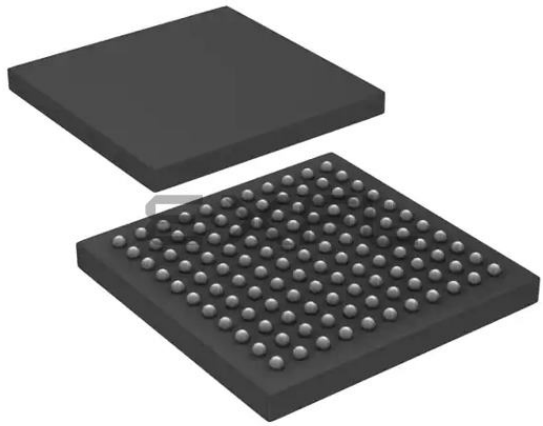
Microchip Technology - PIC24FJ128GB610-I/BG Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128gb610-i-bg

TABLE 1-3: PIC24FJ1024GA610/GB610 FAMILY PINOUT DESCRIPTIONS

Pin Function	Pin Number/Grid Locator						I/O	Input Buffer	Description
	GA606 64-Pin QFN/TQFP/ QFP	GB606 64-Pin QFN/ TQFP/QFP	GA610 100-Pin TQFP/ QFP	GB610 100-Pin TQFP/ QFP	GA612 121-Pin BGA	GB612 121-Pin BGA			
AN0	16	16	25	25	K2	K2	I	ANA	A/D Analog Inputs
AN1	15	15	24	24	K1	K1	I	ANA	
AN2	14	14	23	23	J2	J2	I	ANA	
AN3	13	13	22	22	J1	J1	I	ANA	
AN4	12	12	21	21	H2	H2	I	ANA	
AN5	11	11	20	20	H1	H1	I	ANA	
AN6	17	17	26	26	L1	L1	I	ANA	
AN7	18	18	27	27	J3	J3	I	ANA	
AN8	21	21	32	32	K4	K4	I	ANA	
AN9	22	22	33	33	L4	L4	I	ANA	
AN10	23	23	34	34	L5	L5	I	ANA	
AN11	24	24	35	35	J5	J5	I	ANA	
AN12	27	27	41	41	J7	J7	I	ANA	
AN13	28	28	42	42	L7	L7	I	ANA	
AN14	29	29	43	43	K7	K7	I	ANA	
AN15	30	30	44	44	L8	L8	I	ANA	
AN16	—	—	9	9	E1	E1	I	ANA	
AN17	—	—	10	10	E3	E3	I	ANA	
AN18	—	—	11	11	F4	F4	I	ANA	
AN19	—	—	12	12	F2	F2	I	ANA	
AN20	—	—	14	14	F3	F3	I	ANA	
AN21	—	—	19	19	G2	G2	I	ANA	
AN22	—	—	92	92	B5	B5	I	ANA	
AN23	—	—	91	91	C5	C5	I	ANA	
AV_{DD}	19	19	30	30	J4	J4	P	—	Positive Supply for Analog modules
AV_{SS}	20	20	31	31	L3	L3	P	—	Ground Reference for Analog modules
C1INA	11	11	20	20	H1	H1	I	ANA	Comparator 1 Input A
C1INB	12	12	21	21	H2	H2	I	ANA	Comparator 1 Input B
C1INC	5,8	5,8	11,14	11,14	F4,F3	F4,F3	I	ANA	Comparator 1 Input C
C1IND	4	4	10	10	E3	E3	I	ANA	Comparator 1 Input D
C2INA	13	13	22	22	J1	J1	I	ANA	Comparator 2 Input A
C2INB	14	14	23	23	J2	J2	I	ANA	Comparator 2 Input B
C2INC	8	8	14	14	F3	F3	I	ANA	Comparator 2 Input C
C2IND	6	6	12	12	F2	F2	I	ANA	Comparator 2 Input D
C3INA	55	55	84	84	C7	C7	I	ANA	Comparator 3 Input A

Legend: TTL = TTL input buffer; ANA = Analog level input/output; DIG = Digital input/output; ST = Schmitt Trigger input buffer; I^2C = I^2C/SMBus input buffer; XCVR = Dedicated Transceiver

REGISTER 3-2: CORCON: CPU CORE CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/C-0	R/W-1	U-0	U-0
—	—	—	—	IPL3(1)	PSV(2)	—	—
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit(1)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

bit 2 **PSV:** Program Space Visibility (PSV) in Data Space Enable
1 = Program space is visible in Data Space
0 = Program space is not visible in Data Space

bit 1-0 **Unimplemented:** Read as '0'

Note 1: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level; see Register 3-1 for bit description.

2: If PSV = 0, any reads from data memory at 0x8000 and above will cause an address trap error instead of reading from the PSV section of program memory. This bit is not individually addressable.

TABLE 4-9: SFR MAP: 0500h BLOCK

File Name	Address	All Resets	File Name	Address	All Resets
DMA (CONTINUED)			**USB OTG (CONTINUED)**		
DMAINT5	0500	0000	U1ADDR	056E	00xx
DMASRC5	0502	0000	U1BDTP1	0570	0000
DMADST5	0504	0000	U1FRML	0572	0000
DMACNT5	0506	0001	U1FRMH	0574	0000
DMACH6	0508	0000	U1TOK	0576	0000
DMAINT6	050A	0000	U1SOF	0578	0000
DMASRC6	050C	0000	U1BDTP2	057A	0000
DMADST6	050E	0000	U1BDTP3	057C	0000
DMACNT6	0510	0001	U1CNFG1	057E	0000
DMACH7	0512	0000	U1CNFG2	0580	0000
DMAINT7	0514	0000	U1EP0	0582	0000
DMASRC7	0516	0000	U1EP1	0584	0000
DMADST7	0518	0000	U1EP2	0586	0000
DMACNT7	051A	0001	U1EP3	0588	0000
USB OTG			U1EP4	058A	0000
U1OTGIR	0558	0000	U1EP5	058C	0000
U1OTGIE	055A	0000	U1EP6	058E	0000
U1OTGSTAT	055C	0000	U1EP7	0590	0000
U1OTGCON	055E	0000	U1EP8	0592	0000
U1PWRC	0560	00x0	U1EP9	0594	0000
U1IR	0562	0000	U1EP10	0596	0000
U1IE	0564	0000	U1EP11	0598	0000
U1EIR	0566	0000	U1EP12	059A	0000
U1EIE	0568	0000	U1EP13	059C	0000
U1STAT	056A	0000	U1EP14	059E	0000
U1CON	056C	00x0	U1EP15	05A0	0000

Legend: — = unimplemented, read as '0'; x = undefined. Reset values are shown in hexadecimal.

REGISTER 5-2: DMACHn: DMA CHANNEL n CONTROL REGISTER

U-0	U-0	U-0	r-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	NULLW	RELOAD(1)	CHREQ(3)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SAMODE1	SAMODE0	DAMODE1	DAMODE0	TRMODE1	TRMODE0	SIZE	CHEN
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **Reserved:** Maintain as '0'

bit 11 **Unimplemented:** Read as '0'

bit 10 **NULLW:** Null Write Mode bit
- 1 = A dummy write is initiated to DMASRCn for every write to DMADSTn
- 0 = No dummy write is initiated

bit 9 **RELOAD:** Address and Count Reload bit(1)
- 1 = DMASRCn, DMADSTn and DMACNTn registers are reloaded to their previous values upon the start of the next operation
- 0 = DMASRCn, DMADSTn and DMACNTn are not reloaded on the start of the next operation(2)

bit 8 **CHREQ:** DMA Channel Software Request bit(3)
- 1 = A DMA request is initiated by software; automatically cleared upon completion of a DMA transfer
- 0 = No DMA request is pending

bit 7-6 **SAMODE<1:0>:** Source Address Mode Selection bits
- 11 = DMASRCn is used in Peripheral Indirect Addressing and remains unchanged
- 10 = DMASRCn is decremented based on the SIZE bit after a transfer completion
- 01 = DMASRCn is incremented based on the SIZE bit after a transfer completion
- 00 = DMASRCn remains unchanged after a transfer completion

bit 5-4 **DAMODE<1:0>:** Destination Address Mode Selection bits
- 11 = DMADSTn is used in Peripheral Indirect Addressing and remains unchanged
- 10 = DMADSTn is decremented based on the SIZE bit after a transfer completion
- 01 = DMADSTn is incremented based on the SIZE bit after a transfer completion
- 00 = DMADSTn remains unchanged after a transfer completion

bit 3-2 **TRMODE<1:0>:** Transfer Mode Selection bits
- 11 = Repeated Continuous mode
- 10 = Continuous mode
- 01 = Repeated One-Shot mode
- 00 = One-Shot mode

bit 1 **SIZE:** Data Size Selection bit
- 1 = Byte (8-bit)
- 0 = Word (16-bit)

bit 0 **CHEN:** DMA Channel Enable bit
- 1 = The corresponding channel is enabled
- 0 = The corresponding channel is disabled

Note 1: Only the original DMACNTn is required to be stored to recover the original DMASRCn and DMADSTn.

2: DMASRCn, DMADSTn and DMACNTn are always reloaded in Repeated mode transfers (DMACHn<2> = 1), regardless of the state of the RELOAD bit.

3: The number of transfers executed while CHREQ is set depends on the configuration of TRMODE<1:0>.

6.0 FLASH PROGRAM MEMORY

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"PIC24F Flash Program Memory"** (DS30009715), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

The PIC24FJ1024GA610/GB610 family of devices contains internal Flash program memory for storing and executing application code. The program memory is readable, writable and erasable. The Flash memory can be programmed in four ways:

- In-Circuit Serial Programming™ (ICSP™)
- Run-Time Self-Programming (RTSP)
- JTAG
- Enhanced In-Circuit Serial Programming (Enhanced ICSP)

ICSP allows a PIC24FJ1024GA610/GB610 family device to be serially programmed while in the end application circuit. This is simply done with two lines for the programming clock and programming data (named PGECx and PGEDx, respectively), and three other lines for power (V_{DD}), ground (V_{SS}) and Master Clear ($\overline{MCLR}$). This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using TBLRD (Table Read) and TBLWT (Table Write) instructions. With RTSP, the user may write program memory data in blocks of 128 instructions (384 bytes) at a time and erase program memory in blocks of 1024 instructions (3072 bytes) at a time.

The device implements a 7-bit Error Correcting Code (ECC). The NVM block contains a logic to write and read ECC bits to and from the Flash memory. The Flash is programmed at the same time as the corresponding ECC parity bits. The ECC provides improved resistance to Flash errors. ECC single bit errors can be transparently corrected. ECC Double-Bit Errors (ECCDBE) result in a trap.

6.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the Table Read and Table Write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using the TBLPAG<7:0> bits and the Effective Address (EA) from a W register, specified in the table instruction, as shown in Figure 6-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 6-1: ADDRESSING FOR TABLE REGISTERS

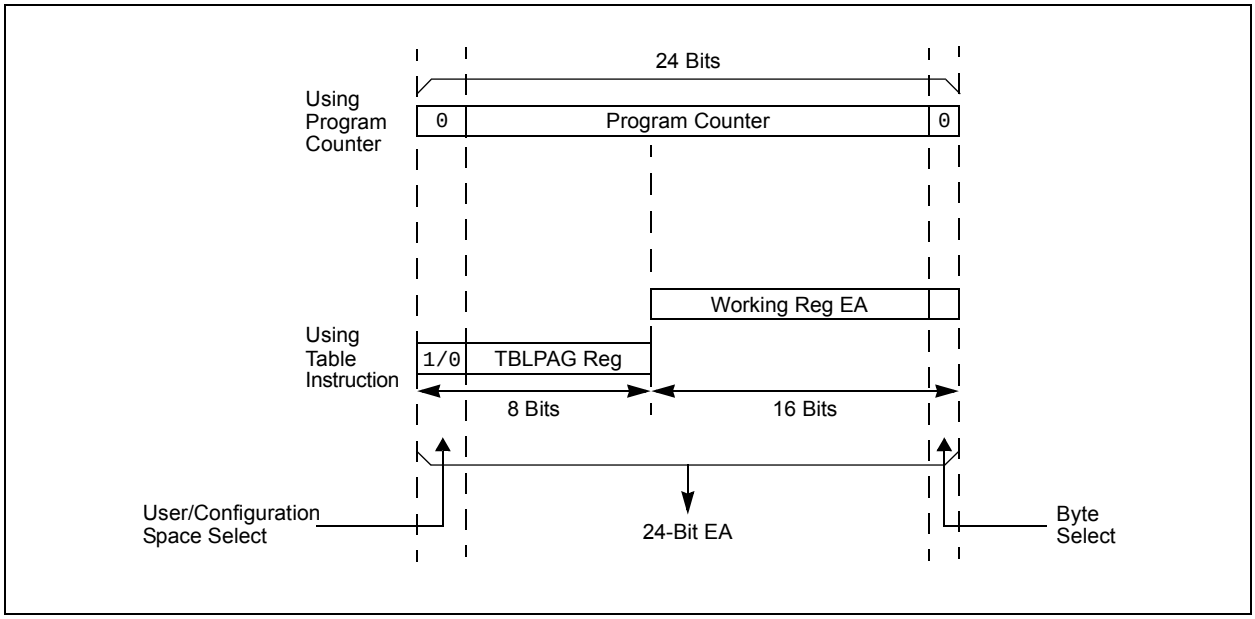


TABLE 7-3: RESET DELAY TIMES FOR VARIOUS DEVICE RESETS

Reset Type	Clock Source	$\overline{\text{SYSRST}}$ Delay	System Clock Delay	Notes
POR	EC	TPOR + TSTARTUP + TRST	—	**1, 2, 3**
	ECPLL	TPOR + TSTARTUP + TRST	TLOCK	**1, 2, 3, 5**
	XT, HS, SOSC	TPOR + TSTARTUP + TRST	TOST	**1, 2, 3, 4**
	XTPLL, HSPLL	TPOR + TSTARTUP + TRST	TOST + TLOCK	**1, 2, 3, 4, 5**
	FRC, OSCFDIV	TPOR + TSTARTUP + TRST	TFRC	**1, 2, 3, 6, 7**
	FRCPLL	TPOR + TSTARTUP + TRST	TFRC + TLOCK	**1, 2, 3, 5, 6**
	LPRC	TPOR + TSTARTUP + TRST	TLPRC	**1, 2, 3, 6**
	DCO	TPOR + TSTARTUP + TRST	TDCO	**1, 2, 3, 8**
BOR	EC	TSTARTUP + TRST	—	**2, 3**
	ECPLL	TSTARTUP + TRST	TLOCK	**2, 3, 5**
	XT, HS, SOSC	TSTARTUP + TRST	TOST	**2, 3, 4**
	XTPLL, HSPLL	TSTARTUP + TRST	TOST + TLOCK	**2, 3, 4, 5**
	FRC, OSCFDIV	TSTARTUP + TRST	TFRC	**2, 3, 6, 7**
	FRCPLL	TSTARTUP + TRST	TFRC + TLOCK	**2, 3, 5, 6**
	LPRC	TSTARTUP + TRST	TLPRC	**2, 3, 6**
	DCO	TPOR + TSTARTUP + TRST	TDCO	**1, 2, 3, 8**
$\overline{\text{MCLR}}$	Any Clock	TRST	—	**3**
WDT	Any Clock	TRST	—	**3**
Software	Any clock	TRST	—	**3**
Illegal Opcode	Any Clock	TRST	—	**3**
Uninitialized W	Any Clock	TRST	—	**3**
Trap Conflict	Any Clock	TRST	—	**3**

Note 1: TPOR = Power-on Reset Delay (10 μs nominal).

2: TSTARTUP = TVREG.

3: TRST = Internal State Reset Time (2 μs nominal).

4: TOST = Oscillator Start-up Timer (OST). A 10-bit counter counts 1024 oscillator periods before releasing the oscillator clock to the system.

5: TLOCK = PLL Lock Time.

6: TFRC and TLPRC = RC Oscillator Start-up Times.

7: If Two-Speed Start-up is enabled, regardless of the Primary Oscillator selected, the device starts with FRC so the system clock delay is just TFRC, and in such cases, FRC start-up time is valid; it switches to the Primary Oscillator after its respective clock delay.

8: TDCO = DCO Start-up and Stabilization Times.

A recommended code sequence for a clock switch includes the following:

1. Disable interrupts during the OSCCON register unlock and write sequence.
2. Execute the unlock sequence for the OSCCON high byte by writing 78h and 9Ah to OSCCON<15:8> in two back-to-back instructions.
3. Write the new oscillator source to the NOSCx bits in the instruction immediately following the unlock sequence.
4. Execute the unlock sequence for the OSCCON low byte by writing 46h and 57h to OSCCON<7:0> in two back-to-back instructions.
5. Set the OSWEN bit in the instruction immediately following the unlock sequence.
6. Continue to execute code that is not clock-sensitive (optional).
7. Invoke an appropriate amount of software delay (cycle counting) to allow the selected oscillator and/or PLL to start and stabilize.
8. Check to see if OSWEN is '0'. If it is, the switch was successful. If OSWEN is still set, then check the LOCK bit to determine the cause of the failure.

The core sequence for unlocking the OSCCON register and initiating a clock switch is shown in Example 9-1.

EXAMPLE 9-1: BASIC CODE SEQUENCE FOR CLOCK SWITCHING

```
;Place the new oscillator selection in W0
;OSCCONH (high byte) Unlock Sequence
MOV         #OSCCONH, w1
MOV         #0x78, w2
MOV         #0x9A, w3
MOV.b       w2, [w1]
MOV.b       w3, [w1]
;Set new oscillator selection
MOV.b       WREG, OSCCONH
;OSCCONL (low byte) unlock sequence
MOV         #OSCCONL, w1
MOV         #0x46, w2
MOV         #0x57, w3
MOV.b       w2, [w1]
MOV.b       w3, [w1]
;Start oscillator switch operation
BSET        OSCCON, #0
```

9.5 FRC Active Clock Tuning

PIC24FJ1024GA610/GB610 family devices include an automatic mechanism to calibrate the FRC during run time. This system uses active clock tuning from a source of known accuracy to maintain the FRC within a very narrow margin of its nominal 8 MHz frequency. This allows for a frequency accuracy that is well within the requirements of the *"USB 2.0 Specification"* regarding full-speed USB devices.

Note:	The self-tune feature maintains sufficient accuracy for operation in USB Device mode. For applications that function as a USB host, a high-accuracy clock source (±0.05%) is still required.

The self-tune system is controlled by the bits in the upper half of the OSCTUN register. Setting the STEN bit (OSCTUN<15>) enables the self-tuning feature, allowing the hardware to calibrate to a source selected by the STSRC bit (OSCTUN<12>). When STSRC = 1, the system uses the Start-of-Frame (SOF) packets from an external USB host for its source. When STSRC = 0, the system uses the crystal-controlled SOSC for its calibration source. Regardless of the source, the system uses the TUN<5:0> bits (OSCTUN<5:0>) to change the FRC Oscillator's frequency. Frequency monitoring and adjustment is dynamic, occurring continuously during run time. While the system is active, the TUNx bits cannot be written to by software.

Note:	To use the USB as a reference clock tuning source (STSRC = 1), the microcontroller must be configured for USB device operation and connected to a non-suspended USB host or hub port. If the SOSC is to be used as the reference clock tuning source (STSRC = 0), the SOSC must also be enabled for clock tuning to occur.

The self-tune system can generate a hardware interrupt, FSTIF. The interrupt can result from a drift of the FRC from the reference, by greater than 0.2% in either direction, or whenever the frequency deviation is beyond the ability of the TUN<5:0> bits to correct (i.e., greater than 1.5%). The STLOCK and STOR status bits (OSCTUN<11,9>) are used to indicate these conditions.

The STLPOL and STORPOL bits (OSCTUN<10,8>) configure the FSTIF interrupt to occur in the presence or the absence of the conditions. It is the user's responsibility to monitor both the STLOCK and STOR bits to determine the exact cause of the interrupt.

Note:	The STLPOL and STORPOL bits should be ignored when the self-tune system is disabled (STEN = 0).

REGISTER 11-3: ANSC: PORTC ANALOG FUNCTION SELECTION REGISTER

U-0	R/W-1	R/W-1	U-0	U-0	U-0	U-0	U-0
—	ANSC<14:13>		—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-1	U-0	U-0	U-0	U-0
—	—	—	ANSC4(1)	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-13 **ANSC<14:13>:** PORTC Analog Function Selection bits
1 = Pin is configured in Analog mode; I/O port read is disabled
0 = Pin is configured in Digital mode; I/O port read is enabled

bit 12-5 **Unimplemented:** Read as '0'

bit 4 **ANSC4:** PORTC Analog Function Selection bit(1)
1 = Pin is configured in Analog mode; I/O port read is disabled
0 = Pin is configured in Digital mode; I/O port read is enabled

bit 3-0 **Unimplemented:** Read as '0'

Note 1: ANSC4 is not available on 64-pin devices.

REGISTER 11-4: ANSD: PORTD ANALOG FUNCTION SELECTION REGISTER

U-0	U-0	r-1	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-1	R/W-1	U-0	U-0	U-0	U-0	U-0	U-0
ANSD<7:6>		—	—	—	—	—	—
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **Reserved:** Read as '1'

bit 12-8 **Unimplemented:** Read as '0'

bit 7-6 **ANSD<7:6>:** PORTD Analog Function Selection bits
1 = Pin is configured in Analog mode; I/O port read is disabled
0 = Pin is configured in Digital mode; I/O port read is enabled

bit 5-0 **Unimplemented:** Read as '0'

NOTES:

17.0 SERIAL PERIPHERAL INTERFACE (SPI)

Note: This data sheet summarizes the features of the PIC24FJ1024GA610/GB610 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Serial Peripheral Interface (SPI) with Audio Codec Support"** (DS70005136), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

The Serial Peripheral Interface (SPI) module is a synchronous serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D Converters, etc. The SPI module is compatible with the Motorola® SPI and SIOP interfaces. All devices in the PIC24FJ1024GA610/GB610 family include three SPI modules.

The module supports operation in two buffer modes. In Standard mode, data is shifted through a single serial buffer. In Enhanced Buffer mode, data is shifted through a FIFO buffer. The FIFO level depends on the configured mode.

Variable length data can be transmitted and received from 2 to 32 bits.

Note: Do not perform Read-Modify-Write operations (such as bit-oriented instructions) on the SPIxBUF register in either Standard or Enhanced Buffer mode.

The module also supports a basic framed SPI protocol while operating in either Master or Slave mode. A total of four framed SPI configurations are supported.

The module also supports Audio modes. Four different Audio modes are available.

- I^2S mode
- Left Justified
- Right Justified
- PCM/DSP

In each of these modes, the serial clock is free-running and audio data is always transferred.

If an audio protocol data transfer takes place between two devices, then usually one device is the master and the other is the slave. However, audio data can be transferred between two slaves. Because the audio protocols require free-running clocks, the master can be a third party controller. In either case, the master generates two free-running clocks: SCKx and LRC (Left, Right Channel Clock/$\overline{SS}$x/FSYNC).

The SPI serial interface consists of four pins:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- SCKx: Shift Clock Input or Output
- $\overline{SS}$x: Active-Low Slave Select or Frame Synchronization I/O Pulse

The SPI module can be configured to operate using 2, 3 or 4 pins. In the 3-pin mode, $\overline{SS}$x is not used. In the 2-pin mode, both SDOx and $\overline{SS}$x are not used.

The SPI module has the ability to generate three interrupts reflecting the events that occur during the data communication. The following types of interrupts can be generated:

1. Receive interrupts are signalled by SPIxRXIF. This event occurs when:
   - RX watermark interrupt
   - SPIROV = 1
   - SPIRBF = 1
   - SPIRBE = 1

   provided the respective mask bits are enabled in SPIxIMSKL/H.
2. Transmit interrupts are signalled by SPIxTXIF. This event occurs when:
   - TX watermark interrupt
   - SPITUR = 1
   - SPITBF = 1
   - SPITBE = 1

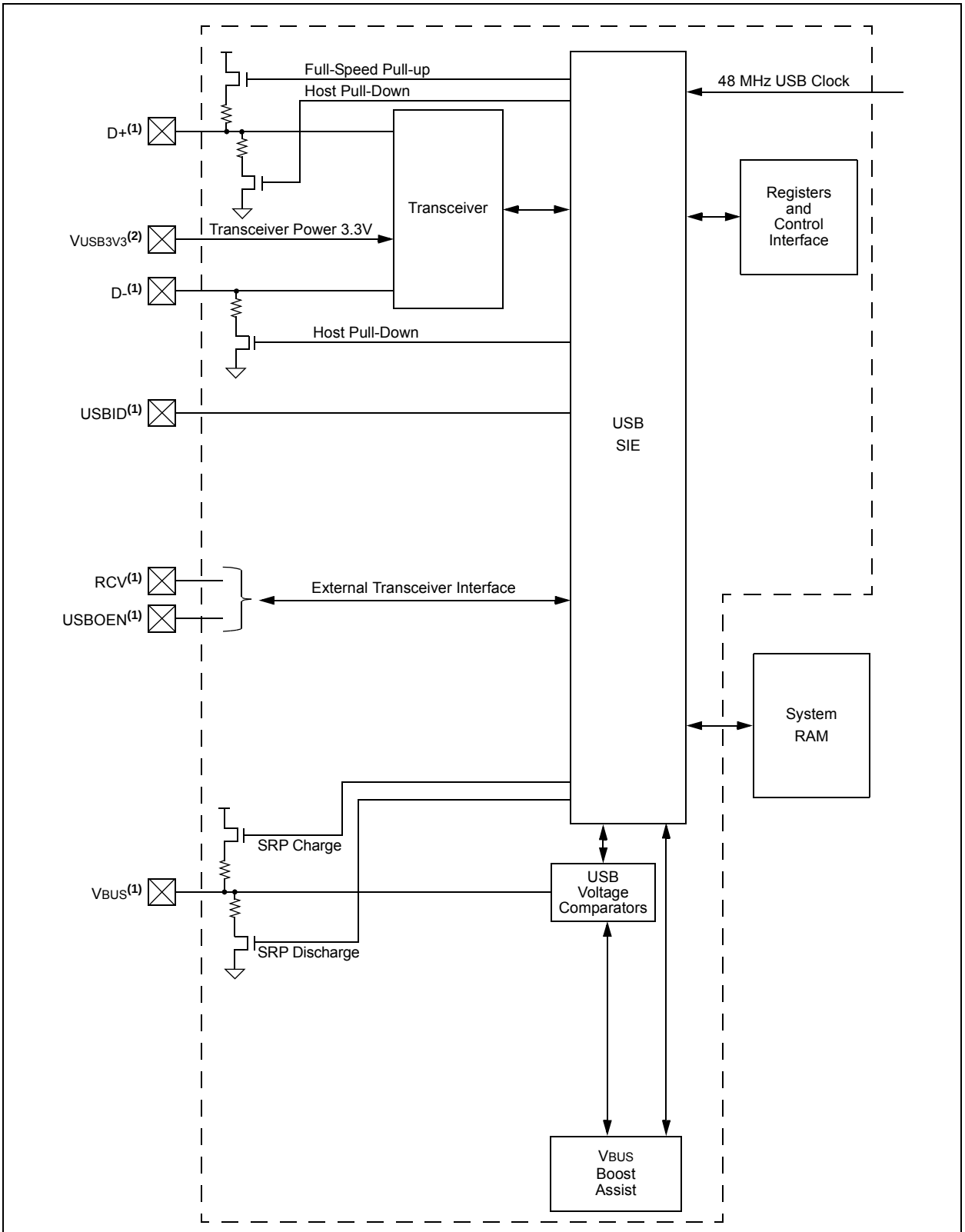
   provided the respective mask bits are enabled in SPIxIMSKL/H.
3. General interrupts are signalled by SPIxIF. This event occurs when
   - FRMERR = 1
   - SPIBUSY = 1
   - SRMT = 1

   provided the respective mask bits are enabled in SPIxIMSKL/H.

A block diagram of the module in Enhanced Buffer mode is shown in Figure 17-1.

Note: In this section, the SPI modules are referred to together as SPIx, or separately as SPI1, SPI2 or SPI3. Special Function Registers will follow a similar notation. For example, SPIxCON1 and SPIxCON2 refer to the control registers for any of the three SPI modules.

FIGURE 20-1: USB OTG MODULE BLOCK DIAGRAM



Note 1: Pins are multiplexed with digital I/O and other device features.

2: Connecting V_{BUS3V3} to V_{DD} is highly recommended, as floating this input can cause increased I_{PD} currents. The pin should be tied to V_{DD} when the USB functions are not used.

REGISTER 21-5: PMCSxCF: EPMP CHIP SELECT x CONFIGURATION REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
CSDIS	CSP	CSPTEN	BEP	—	WRSP	RDSP	SM
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
ACKP	PTSZ1	PTSZ0	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CSDIS:** Chip Select x Disable bit
1 = Disables the Chip Select x functionality
0 = Enables the Chip Select x functionality

bit 14 **CSP:** Chip Select x Polarity bit
1 = Active-high (PMCSx)
0 = Active-low ($\overline{\text{PMCSx}}$)

bit 13 **CSPTEN:** PMCSx Port Enable bit
1 = PMCSx port is enabled
0 = PMCSx port is disabled

bit 12 **BEP:** Chip Select x Nibble/Byte Enable Polarity bit
1 = Nibble/byte enable is active-high (PMBE0, PMBE1)
0 = Nibble/byte enable is active-low ($\overline{\text{PMBE0}}$, $\overline{\text{PMBE1}}$)

bit 11 **Unimplemented:** Read as '0'

bit 10 **WRSP:** Chip Select x Write Strobe Polarity bit
For Slave modes and Master mode when SM = 0:
1 = Write strobe is active-high (PMWR)
0 = Write strobe is active-low ($\overline{\text{PMWR}}$)
For Master mode when SM = 1:
1 = Enable strobe is active-high (PMENB)
0 = Enable strobe is active-low ($\overline{\text{PMENB}}$)

bit 9 **RDSP:** Chip Select x Read Strobe Polarity bit
For Slave modes and Master mode when SM = 0:
1 = Read strobe is active-high (PMRD)
0 = Read strobe is active-low ($\overline{\text{PMRD}}$)
For Master mode when SM = 1:
1 = Read/write strobe is active-high (PMRD/$\overline{\text{PMWR}}$)
0 = Read/Write strobe is active-low ($\overline{\text{PMRD}}$/$\overline{\text{PMWR}}$)

bit 8 **SM:** Chip Select x Strobe Mode bit
1 = Reads/writes and enables strobes (PMRD/$\overline{\text{PMWR}}$ and PMENB)
0 = Reads and writes strobes (PMRD and PMWR)

bit 7 **ACKP:** Chip Select x Acknowledge Polarity bit
1 = ACK is active-high (PMACK1)
0 = ACK is active-low ($\overline{\text{PMACK1}}$)

bit 6-5 **PTSZ<1:0>:** Chip Select x Port Size bits
11 = Reserved
10 = 16-bit port size (PMD<15:0>)
01 = 4-bit port size (PMD<3:0>)
00 = 8-bit port size (PMD<7:0>)

bit 4-0 **Unimplemented:** Read as '0'

REGISTER 22-9: DATEL: RTCC DATE REGISTER (LOW)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-12 **DAYTEN<1:0>:** Binary Coded Decimal Value of Days ‘10’ Digit bits
Contains a value from 0 to 3.

bit 11-8 **DAYONE<3:0>:** Binary Coded Decimal Value of Days ‘1’ Digit bits
Contains a value from 0 to 9.

bit 7-3 **Unimplemented:** Read as ‘0’

bit 2-0 **WDAY<2:0>:** Binary Coded Decimal Value of Weekdays ‘1’ Digit bits
Contains a value from 0 to 6.

REGISTER 22-10: DATEH: RTCC DATE REGISTER (HIGH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-x	R/W-x	R/W-x	R/W-x
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 15							bit 8

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **YRTEN<3:0>:** Binary Coded Decimal Value of Years ‘10’ Digit bits

bit 11-8 **YRONE<3:0>:** Binary Coded Decimal Value of Years ‘1’ Digit bits

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **MTHTEN:** Binary Coded Decimal Value of Months ‘10’ Digit bit
Contains a value from 0 to 1.

bit 3-0 **MTHONE<3:0>:** Binary Coded Decimal Value of Months ‘1’ Digit bits
Contains a value from 0 to 9.

REGISTER 22-13: ALMDATEL: RTCC ALARM DATE REGISTER (LOW)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-12 **DAYTEN<1:0>:** Binary Coded Decimal Value of Days ‘10’ Digit bits
Contains a value from 0 to 3.

bit 11-8 **DAYONE<3:0>:** Binary Coded Decimal Value of Days ‘1’ Digit bits
Contains a value from 0 to 9.

bit 7-3 **Unimplemented:** Read as ‘0’

bit 2-0 **WDAY<2:0>:** Binary Coded Decimal Value of Weekdays ‘1’ Digit bits
Contains a value from 0 to 6.

REGISTER 22-14: ALMDATEH: RTCC ALARM DATE REGISTER (HIGH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	MTHTEN	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **YRTEN<3:0>:** Binary Coded Decimal Value of Years ‘10’ Digit bits

bit 11-8 **YRONE<3:0>:** Binary Coded Decimal Value of Years ‘1’ Digit bits

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **MTHTEN:** Binary Coded Decimal Value of Months ‘10’ Digit bit
Contains a value from 0 to 1.

bit 3-0 **MTHONE<3:0>:** Binary Coded Decimal Value of Months ‘1’ Digit bits
Contains a value from 0 to 9.

REGISTER 22-17: TSADATEL: RTCC TIMESTAMP A DATE REGISTER (LOW)(1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **DAYTEN<1:0>:** Binary Coded Decimal Value of Days '10' Digit bits
Contains a value from 0 to 3.

bit 11-8 **DAYONE<3:0>:** Binary Coded Decimal Value of Days '1' Digit bits
Contains a value from 0 to 9.

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **WDAY<2:0>:** Binary Coded Decimal Value of Weekdays '1' Digit bits
Contains a value from 0 to 6.

Note 1: If TSAEN = 0, bits<15:0> can be used for persistence storage throughout a non-Power-on Reset ($\overline{\text{MCLR}}$, WDT, etc.).

25.0 12-BIT A/D CONVERTER WITH THRESHOLD DETECT

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the 12-Bit A/D Converter, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"12-Bit A/D Converter with Threshold Detect"** (DS39739), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

The A/D Converter has the following key features:

- Successive Approximation Register (SAR) Conversion
- Selectable 10-Bit or 12-Bit (default) Conversion Resolution
- Conversion Speeds of up to 200 ksps (12-bit)
- Up to 24 Analog Input Channels (internal and external)
- Multiple Internal Reference Input Channels
- External Voltage Reference Input Pins
- Unipolar Differential Sample-and-Hold (S/H) Amplifier
- Automated Threshold Scan and Compare Operation to Pre-Evaluate Conversion Results
- Selectable Conversion Trigger Source
- Fixed Length (one word per channel), Configurable Conversion Result Buffer
- Four Options for Results Alignment
- Configurable Interrupt Generation
- Enhanced DMA Operations with Indirect Address Generation
- Operation During CPU Sleep and Idle modes

The 12-bit A/D Converter module is an enhanced version of the 10-bit module offered in earlier PIC24 devices. It is a Successive Approximation Register (SAR) Converter, enhanced with 12-bit resolution, a wide range of automatic sampling options, tighter integration with other analog modules and a configurable results buffer.

It also includes a unique Threshold Detect feature that allows the module itself to make simple decisions based on the conversion results, and enhanced operation with the DMA Controller through Peripheral Indirect Addressing (PIA).

A simplified block diagram for the module is shown in Figure 25-1.

25.1 Basic Operation

To perform a standard A/D conversion:

1. Configure the module:
   a) Configure port pins as analog inputs by setting the appropriate bits in the ANSx registers (see **Section 11.2 "Configuring Analog Port Pins (ANSx)"** for more information).
   b) Select the voltage reference source to match the expected range on analog inputs (AD1CON2<15:13>).
   c) Select the positive and negative multiplexer inputs for each channel (AD1CHS<15:0>).
   d) Select the analog conversion clock to match the desired data rate with the processor clock (AD1CON3<7:0>).
   e) Select the appropriate sample/conversion sequence (AD1CON1<7:4> and AD1CON3<12:8>).
   f) For Channel A scanning operations, select the positive channels to be included (AD1CSSH and AD1CSSL registers).
   g) Select how conversion results are presented in the buffer (AD1CON1<9:8> and AD1CON5 register).
   h) Select the interrupt rate (AD1CON2<5:2>).
   i) Turn on A/D module (AD1CON1<15>).
2. Configure the A/D interrupt (if required):
   a) Clear the AD1IF bit (IFS0<13>).
   b) Enable the AD1IE interrupt (IEC0<13>).
   c) Select the A/D interrupt priority (IPC3<6:4>).
3. If the module is configured for manual sampling, set the SAMP bit (AD1CON1<1>) to begin sampling.

REGISTER 25-2: AD1CON2: A/D CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	r-0	R/W-0	R/W-0	U-0	U-0
PVCFG1	PVCFG0	NVCFG0	—	BUFREGEN	CSCNA	—	—
bit 15							bit 8

R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUFS	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **PVCFG<1:0>:** A/D Converter Positive Voltage Reference Configuration bits
1x = Unimplemented, do not use
01 = External VREF+
00 = AVDD

bit 13 **NVCFG0:** A/D Converter Negative Voltage Reference Configuration bit
1 = External VREF-
0 = AVSS

bit 12 **Reserved:** Maintain as '0'

bit 11 **BUFREGEN:** A/D Buffer Register Enable bit
1 = Conversion result is loaded into the buffer location determined by the converted channel
0 = A/D result buffer is treated as a FIFO

bit 10 **CSCNA:** Scan Input Selections for CH0+ During Sample A bit
1 = Scans inputs
0 = Does not scan inputs

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit
When DMAEN = 1 and DMABM = 1:
1 = A/D is currently filling the destination buffer from [buffer start + (buffer size/2)] to [buffer start + (buffer size – 1)]. User should access data located from [buffer start] to [buffer start + (buffer size/2) – 1].
0 = A/D is currently filling the destination buffer from [buffer start] to [buffer start + (buffer size/2) – 1]. User should access data located from [buffer start + (buffer size/2)] to [buffer start + (buffer size – 1)].
When DMAEN = 0:
1 = A/D is currently filling ADC1BUF13-ADC1BUF25, user should access data in ADC1BUF0-ADC1BUF12
0 = A/D is currently filling ADC1BUF0-ADC1BUF12, user should access data in ADC1BUF13-ADC1BUF25

TABLE 33-4: DC CHARACTERISTICS: OPERATING CURRENT (I_{DD})

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Operating Temperature**	**VDD**	**Conditions**
Operating Current (I_{DD})(2)						
DC19	230	365	µA	-40°C to +85°C	2.0V	0.5 MIPS, FOSC = 1 MHz
	250	365	µA	-40°C to +85°C	3.3V	
DC20	430	640	µA	-40°C to +85°C	2.0V	1 MIPS, FOSC = 2 MHz
	440	640	µA	-40°C to +85°C	3.3V	
DC23	1.5	2.4	mA	-40°C to +85°C	2.0V	4 MIPS, FOSC = 8 MHz
	1.65	2.4	mA	-40°C to +85°C	3.3V	
DC24	6.1	7.7	mA	-40°C to +85°C	2.0V	16 MIPS, FOSC = 32 MHz
	6.3	7.7	mA	-40°C to +85°C	3.3V	
DC31	43	130	µA	-40°C to +85°C	2.0V	LPRC (15.5 KIPS), FOSC = 31 kHz
	46	130	µA	-40°C to +85°C	3.3V	
DC32	1.63	2.5	mA	-40°C to +85°C	2.0V	FRC (4 MIPS), FOSC = 8 MHz
	1.65	2.5	mA	-40°C to +85°C	3.3V	
DC33	1.9	3.0	mA	-40°C to +85°C	2.0V	DCO (4 MIPS), FOSC = 8 MHz
	2.0	3.0	mA	-40°C to +85°C	3.3V	

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Typical parameters are for design guidance only and are not tested.

2: The test conditions for all IDD measurements are as follows: OSC1 driven with external square wave from rail-to-rail. All I/O pins are configured as outputs driving low. $\overline{MCLR}$ = VDD; WDT and FSCM are disabled. CPU, program memory and data memory are operational. All peripheral modules are clocked but inactive (PMDx bits are all '1'). JTAG module is disabled.

TABLE 33-5: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Operating Temperature**	**VDD**	**Conditions**
Idle Current (I_{IDLE})(2)						
DC40	95	215	µA	-40°C to +85°C	2.0V	1 MIPS, FOSC = 2 MHz
	105	225	µA	-40°C to +85°C	3.3V	
DC43	290	720	µA	-40°C to +85°C	2.0V	4 MIPS, FOSC = 8 MHz
	315	750	µA	-40°C to +85°C	3.3V	
DC47	1.05	2.7	mA	-40°C to +85°C	2.0V	16 MIPS, FOSC = 32 MHz
	1.16	2.8	mA	-40°C to +85°C	3.3V	
DC50	350	820	µA	-40°C to +85°C	2.0V	FRC (4 MIPS), FOSC = 8 MHz
	360	850	µA	-40°C to +85°C	3.3V	
DC51	26	110	µA	-40°C to +85°C	2.0V	LPRC (15.5 KIPS), FOSC = 31 kHz
	30	110	µA	-40°C to +85°C	3.3V	

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base IIDLE current is measured with the core off, the clock on and all modules turned off. Peripheral Module Disable SFR registers are '1'. All I/O pins are configured as outputs driving low. JTAG module is disabled.

TABLE 33-11: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
DVR	TVREG	Voltage Regulator Start-up Time	—	10	—	μs	VREGS = 0 with any POR or BOR
DVR10	VBG	Internal Band Gap Reference	1.14	1.2	1.26	V	
DVR11	TBG	Band Gap Reference Start-up Time	—	1	—	ms	
DVR20	VRGOUT	Regulator Output Voltage	1.6	1.8	2	V	VDD > 2.1V
DVR21	CEFC	External Filter Capacitor Value	10	—	—	μF	Series resistance < 3Ω recommended; < 5Ω required
DVR30	VLVR	Low-Voltage Regulator Output Voltage	—	1.2	—	V	RETEN = 1, $\overline{\text{LPCFG}}$ = 0

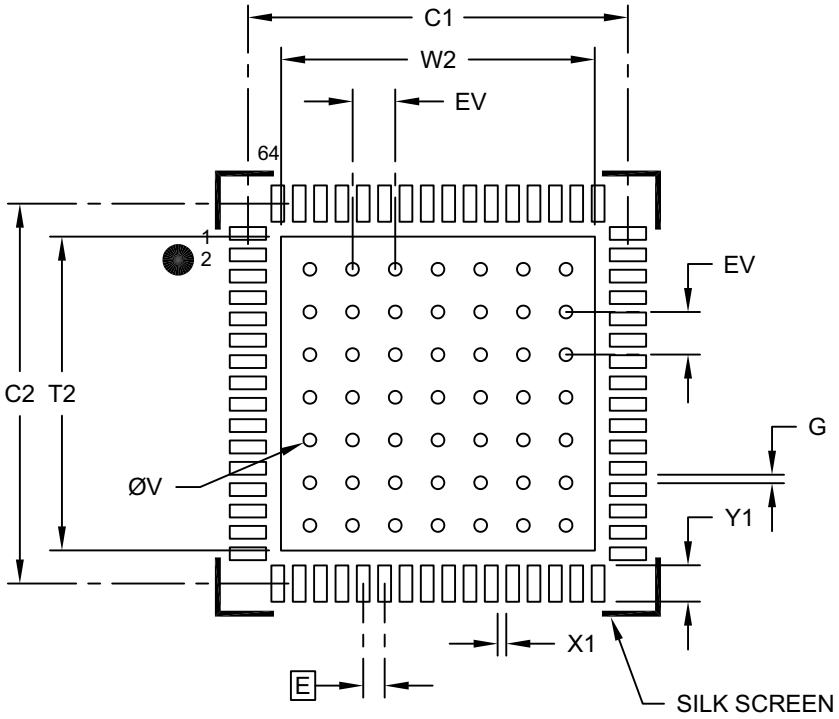
TABLE 33-12: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)								
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
DC18	VHLVD	HLVD Voltage on VDD Transition	HLVDL<3:0> = 0100(1)	3.40	—	3.74	V	VDIR = 1
			HLVDL<3:0> = 0101	3.25	—	3.58	V	
			HLVDL<3:0> = 0110	2.95	—	3.25	V	
			HLVDL<3:0> = 0111	2.75	—	3.04	V	
			HLVDL<3:0> = 1000	2.65	—	2.93	V	
			HLVDL<3:0> = 1001	2.45	—	2.75	V	
			HLVDL<3:0> = 1010	2.35	—	2.64	V	
			HLVDL<3:0> = 1011	2.25	—	2.50	V	
			HLVDL<3:0> = 1100	2.15	—	2.39	V	
			HLVDL<3:0> = 1101	2.08	—	2.28	V	
			HLVDL<3:0> = 1110	2.00	—	2.17	V	
DC101	VTHL	HLVD Voltage on HLVDIN Pin Transition	HLVDL<3:0> = 1111	—	1.20	—	V	
DC105	TONLVD	HLVD Module Enable Time		—	5	—	μS	From POR or HLVDEN = 1

Note 1: Trip points for values of HLVD<3:0>, from '0000' to '0011', are not implemented.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length and 7.70x7.70mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			7.50
Optional Center Pad Length	T2			7.50
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X20)	X1			0.30
Contact Pad Length (X20)	Y1			0.90
Contact Pad to Center Pad (X20)	G	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-2213B