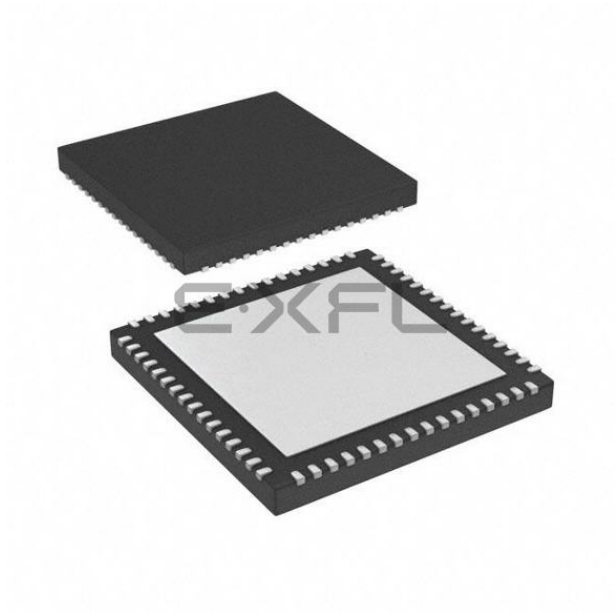
Microchip Technology - PIC24FJ256GA606T-I/MR Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, HLVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256ga606t-i-mr

TABLE 3: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJXXXGB606)

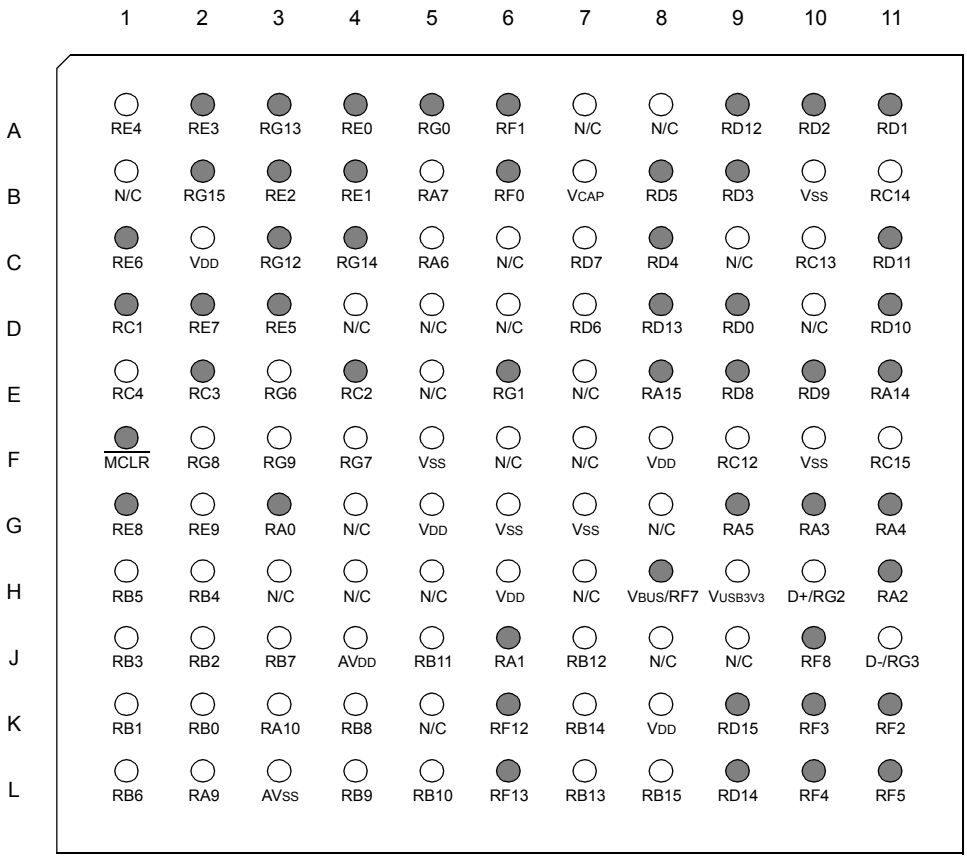
Pin	Function	Pin	Function
1	IC4/CTED4/PMD5/RE5	33	**RP16**/USBID/RF3
2	SCL3/IC5/PMD6/RE6	34	VBUS/RF7
3	SDA3/IC6/PMD7/RE7	35	VUSB3V3
4	C1IND/**RP21**/ICM1/OCM1A/PMA5/RG6	36	D-/RG3
5	C1INC/**RP26**/OCM1B/PMA4/RG7	37	D+/RG2
6	C2IND/**RP19**/ICM2/OCM2A/PMA3/RG8	38	VDD
7	$\overline{\text{MCLR}}$	39	OSCI/CLKI/RC12
8	C1INC/C2INC/C3INC/**RP27**/OCM2B/PMA2/PMALU/RG9	40	OSCO/CLKO/RC15
9	VSS	41	VSS
10	VDD	42	CLC4OUT/**RP2**/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/RD8
11	PGEC3/AN5/C1INA/**RP18**/ICM3/OCM3A/RB5	43	**RP4**/SDA1/PMACK2/RD9
12	PGED3/AN4/C1INB/**RP28**/$\overline{\text{USBOEN}}$/OCM3B/RB4	44	**RP3**/SCL1/PMA15/PMCS2/RD10
13	AN3/C2INA/RB3	45	**RP12**/PMA14/PMCS1/RD11
14	AN2/CTCMP/C2INB/**RP13**/CTED13/RB2	46	CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/INT0/RD0
15	PGEC1/ALTCVREF-/ALTVREF-/AN1/**RP1**/CTED12/RB1	47	SOSCI/C3IND/RC13
16	PGED1/ALTCVREF+/ALTVREF+/AN0/**RP0**/PMA6/RB0	48	SOSCO/C3INC/**RPI37**/PWRLCLK/RC14
17	PGEC2/AN6/**RP6**/RB6	49	**RP24**/U5TX/ICM4/RD1
18	PGED2/AN7/**RP7**/U6TX/RB7	50	**RP23**/PMACK1/RD2
19	AVDD	51	**RP22**/ICM7/PMBE0/RD3
20	AVSS	52	**RP25**/PMWR/PMENB/RD4
21	AN8/**RP8**/PWRGT/RB8	53	**RP20**/PMRD/$\overline{\text{PMWR}}$/RD5
22	AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/PMA7/RB9	54	C3INB/U5RX/OC4/RD6
23	TMS/CVREF/AN10/PMA13/RB10	55	C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/RD7
24	TDO/AN11/REFI/PMA12/RB11	56	VCAP
25	VSS	57	N/C
26	VDD	58	$\overline{\text{U5CTS}}$/OC6/RF0
27	TCK/AN12/U6RX/CTED2/PMA11/RB12	59	RF1
28	TDI/AN13/CTED1/PMA10/RB13	60	PMD0/RE0
29	AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/RB14	61	PMD1/RE1
30	AN15/**RP29**/CTED6/PMA0/PMALL/RB15	62	PMD2/RE2
31	**RP10**/SDA2/PMA9/RF4	63	CTED9/PMD3/RE3
32	**RP17**/SCL2/PMA8/RF5	64	HLVDIN/CTED8/PMD4/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.

Pin Diagrams(1) (Continued)

PIC24FJXXXGB610 121-Pin BGA



Legend: See Table 7 for a complete description of pin functions. Pinouts are subject to change.
Note 1: Gray shading indicates 5.5V tolerant input pins.

Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33/PIC24 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note 1: To access the documents listed below, browse to the documentation section of the PIC24FJ1024GA610/GB610 product page of the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.

In addition to parameters, features and other documentation, the resulting page provides links to the related family reference manual sections.

- **"CPU with Extended Data Space (EDS)"** (DS39732)
- **"Data Memory with Extended Data Space (EDS)"** (DS39733)
- **"Direct Memory Access Controller (DMA)"** (DS39742)
- **"PIC24F Flash Program Memory"** (DS30009715)
- **"Reset"** (DS39712)
- **"Interrupts"** (DS70000600)
- **"Power-Saving Features"** (DS39698)
- **"I/O Ports with Peripheral Pin Select (PPS)"** (DS39711)
- **"Timers"** (DS39704)
- **"Input Capture with Dedicated Timer"** (DS70000352)
- **"Output Compare with Dedicated Timer"** (DS70005159)
- **"Capture/Compare/PWM/Timer (MCCP and SCCP)"** (DS33035A)
- **"Serial Peripheral Interface (SPI) with Audio Codec Support"** (DS70005136)
- **"Inter-Integrated Circuit (I^2C)"** (DS70000195)
- **"UART"** (DS39708)
- **"USB On-The-Go (OTG)"** (DS39721)
- **"Enhanced Parallel Master Port (EPMP)"** (DS39730)
- **"RTCC with Timestamp"** (DS70005193)
- **"RTCC with External Power Control"** (DS39745)
- **"32-Bit Programmable Cyclic Redundancy Check (CRC)"** (DS30009729)
- **"12-Bit A/D Converter with Threshold Detect"** (DS39739)
- **"Scalable Comparator Module"** (DS39734)
- **"Dual Comparator Module"** (DS39710)
- **"Charge Time Measurement Unit (CTMU) and CTMU Operation with Threshold Detect"** (DS30009743)
- **"High-Level Integration with Programmable High/Low-Voltage Detect (HLVD)"** (DS39725)
- **"Watchdog Timer (WDT)"** (DS39697)
- **"CodeGuard™ Intermediate Security"** (DS70005182)
- **"High-Level Device Integration"** (DS39719)
- **"Programming and Diagnostics"** (DS39716)
- **"Dual Partition Flash Program Memory"** (DS70005156)

11.0 I/O PORTS

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"I/O Ports with Peripheral Pin Select (PPS)"** (DS39711), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

All of the device pins (except VDD, VSS, $\overline{\text{MCLR}}$ and OSCI/CLKI) are shared between the peripherals and the Parallel I/O (PIO) ports. All I/O input ports feature Schmitt Trigger (ST) inputs for improved noise immunity.

11.1 Parallel I/O (PIO) Ports

A Parallel I/O port that shares a pin with a peripheral is, in general, subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through", in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 shows how ports are shared with other peripherals and the associated I/O pin to which they are connected.

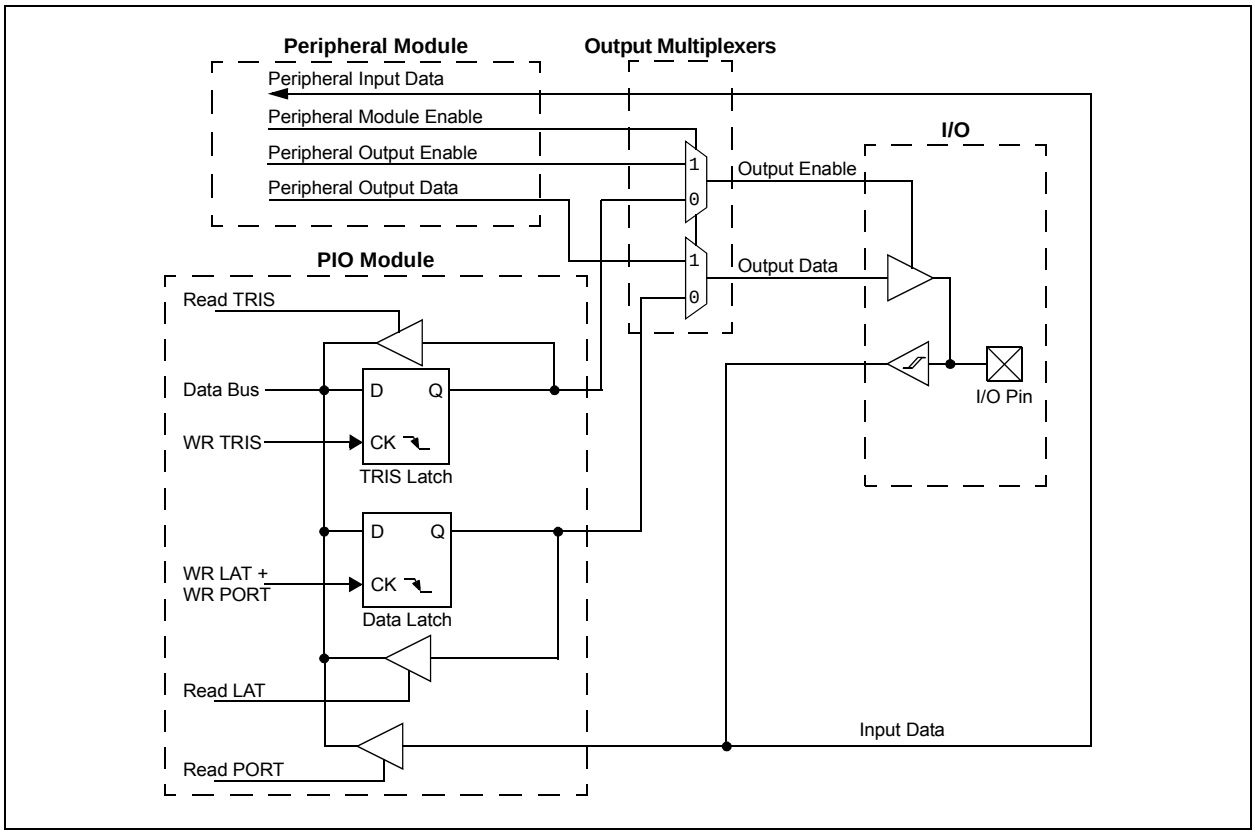
When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin may be read, but the output driver for the parallel port bit will be disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin may be driven by a port.

All port pins have three registers directly associated with their operation as digital I/Os and one register associated with their operation as analog inputs. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the Output Latch register (LATx), read the latch; writes to the latch, write the latch. Reads from the PORTx register, read the port pins; writes to the port pins, write the latch.

Any bit and its associated data and control registers that are not valid for a particular device will be disabled. That means the corresponding LATx and TRISx registers, and the port pin, will read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is regarded as a dedicated port because there is no other competing source of inputs.

FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE



11.4.3.3 Mapping Limitations

The control schema of the Peripheral Pin Select is extremely flexible. Other than systematic blocks that prevent signal contention, caused by two physical pins being configured as the same functional input or two functional outputs configured as the same pin, there are no hardware enforced lockouts. The flexibility extends to the point of allowing a single input to drive multiple peripherals or a single functional output to drive multiple output pins.

11.4.3.4 Mapping Exceptions for PIC24FJ1024GA610/GB610 Family Devices

Although the PPS registers theoretically allow for inputs to be remapped to up to 64 pins, or for outputs to be remapped from 32 pins, not all of these are implemented in all devices. For 100-pin or 121-pin variants of the PIC24FJ1024GA610/GB610 family devices, 32 remappable input/output pins are available and 12 remappable input pins are available. For 64-pin variants, 29 input/outputs and 1 input are available. The differences in available remappable pins are summarized in Table 11-5.

When developing applications that use remappable pins, users should also keep these things in mind:

- For the RPINRx registers, bit combinations corresponding to an unimplemented pin for a particular device are treated as invalid; the corresponding module will not have an input mapped to it.
- For RPORx registers, the bit fields corresponding to an unimplemented pin will also be unimplemented; writing to these fields will have no effect.

11.4.4 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC24F devices include three features to prevent alterations to the peripheral map:

- Control register lock sequence
- Continuous state monitoring
- Configuration bit remapping lock

11.4.4.1 Control Register Lock

Under normal operation, writes to the RPINRx and RPORx registers are not allowed. Attempted writes will appear to execute normally, but the contents of the registers will remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK bit (OSCCON<6>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear IOLOCK, a specific command sequence must be executed:

1. Write 46h to OSCCON<7:0>.
2. Write 57h to OSCCON<7:0>.
3. Clear (or set) IOLOCK as a single operation.

Unlike the similar sequence with the oscillator's LOCK bit, IOLOCK remains in one state until changed. This allows all of the Peripheral Pin Selects to be configured with a single unlock sequence, followed by an update to all control registers, then locked with a second lock sequence.

11.4.4.2 Continuous State Monitoring

In addition to being protected from direct writes, the contents of the RPINRx and RPORx registers are constantly monitored in hardware by shadow registers. If an unexpected change in any of the registers occurs (such as cell disturbances caused by ESD or other external events), a Configuration Mismatch Reset will be triggered.

11.4.4.3 Configuration Bit Pin Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPINRx and RPORx registers. The IOL1WAY (FOSC<5>) Configuration bit blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure will not execute and the Peripheral Pin Select Control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session. Programming IOL1WAY allows users unlimited access (with the proper use of the unlock sequence) to the Peripheral Pin Select registers.

TABLE 11-5: REMAPPABLE PIN EXCEPTIONS FOR PIC24FJ1024GA610/GB610 FAMILY DEVICES

Device	RPn Pins (I/O)		RPIn Pins	
	Total	Unimplemented	Total	Unimplemented
PIC24FJXXXGB606	28	RP5, RP15, RP30, RP31	1	All except RPI37
PIC24FJXXXGX61X	32	—	12	—
PIC24FJXXXGA606	29	RP5, RP15, RP31	1	All except RPI37

NOTES:

20.2 USB Buffer Descriptors and the BDT

Endpoint buffer control is handled through a structure called the Buffer Descriptor Table (BDT). This provides a flexible method for users to construct and control endpoint buffers of various lengths and configurations.

The BDT can be located in any available 512-byte, aligned block of data RAM. The BDT Pointer (U1BDTP1) contains the upper address byte of the BDT and sets the location of the BDT in RAM. The user must set this pointer to indicate the table's location.

The BDT is composed of Buffer Descriptors (BDs) which are used to define and control the actual buffers in the USB RAM space. Each BD consists of two 16-bit, "soft" (non-fixed-address) registers, BDnSTAT and BDnADR, where n represents one of the 64 possible BDs (range of 0 to 63). BDnSTAT is the status register for BDn, while BDnADR specifies the starting address for the buffer associated with BDn.

Note: Since BDnADR is a 16-bit register, only the first 64 Kbytes of RAM can be accessed by the USB module.

Depending on the endpoint buffering configuration used, there are up to 64 sets of Buffer Descriptors, for a total of 256 bytes. At a minimum, the BDT must be at least 8 bytes long. This is because the *"USB 2.0 Specification"* mandates that every device must have Endpoint 0 with both input and output for initial setup.

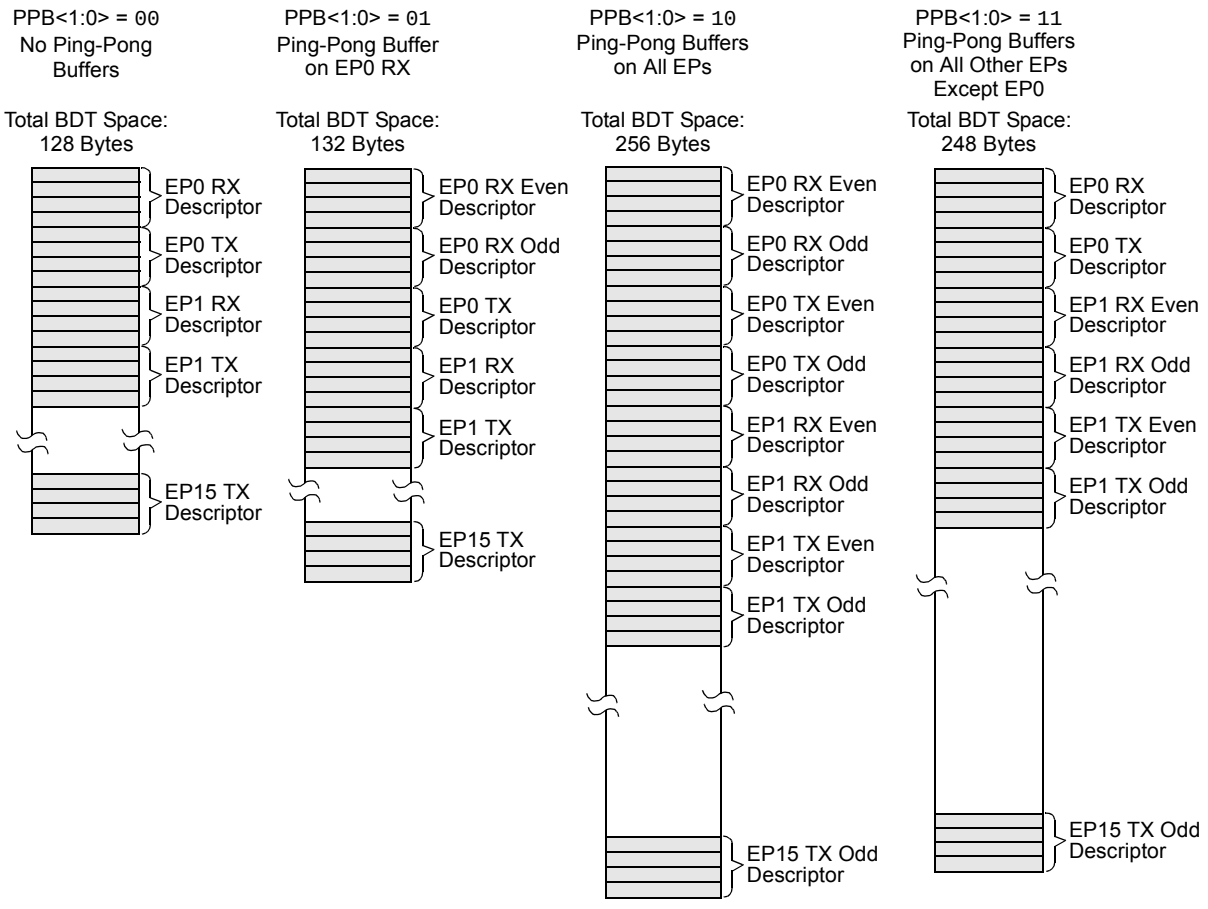
Endpoint mapping in the BDT is dependent on three variables:

- Endpoint number (0 to 15)
- Endpoint direction (RX or TX)
- Ping-pong settings (U1CNFG1<1:0>)

Figure 20-7 illustrates how these variables are used to map endpoints in the BDT.

In Host mode, only Endpoint 0 Buffer Descriptors are used. All transfers utilize the Endpoint 0 Buffer Descriptor and Endpoint Control register (U1EP0). For received packets, the attached device's source endpoint is indicated by the value of ENDPT<3:0> in the USB Status register (U1STAT<7:4>). For transmitted packets, the attached device's destination endpoint is indicated by the value written to the USB Token register (U1TOK).

FIGURE 20-7: BDT MAPPING FOR ENDPOINT BUFFERING MODES



Note: Memory area is not shown to scale.

REGISTER 20-2: BDnSTAT: BUFFER DESCRIPTOR n STATUS REGISTER PROTOTYPE, CPU MODE (BD0STAT THROUGH BD63STAT)

R/W-x	R/W-x	r-0	r-0	R/W-x	R/W-x	R/W-x, HSC	R/W-x, HSC
UOWN	DTS(1)	—	—	DTSEN	BSTALL	BC9	BC8
bit 15							bit 8

R/W-x, HSC	R/W-x, HSC	R/W-x, HSC	R/W-x, HSC	R/W-x, HSC	R/W-x, HSC	R/W-x, HSC	R/W-x, HSC
BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0
bit 7							bit 0

Legend:	r = Reserved bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'r' = Reserved bit	x = Bit is unknown

bit 15 **UOWN:** USB Own bit
- 0 = The microcontroller core owns the BD and its corresponding buffer; the USB module ignores all other fields in the BD

bit 14 **DTS:** Data Toggle Packet bit(1)
- 1 = Data 1 packet
- 0 = Data 0 packet

bit 13-12 **Reserved:** Maintain as '0'

bit 11 **DTSEN:** Data Toggle Synchronization Enable bit
- 1 = Data toggle synchronization is enabled; data packets with incorrect Sync value will be ignored
- 0 = No data toggle synchronization is performed

bit 10 **BSTALL:** Buffer STALL Enable bit
- 1 = Buffer STALL is enabled; STALL handshake issued if a token is received that would use the BD in the given location (UOWN bit remains set, BD value is unchanged); corresponding EPSTALL bit will get set on any STALL handshake
- 0 = Buffer STALL is disabled

bit 9-0 **BC<9:0>:** Byte Count bits

This represents the number of bytes to be transmitted or the maximum number of bytes to be received during a transfer. Upon completion, the byte count is updated by the USB module with the actual number of bytes transmitted or received.

Note 1: This bit is ignored unless DTSEN = 1.

20.6.2 HOST NEGOTIATION PROTOCOL (HNP)

In USB OTG applications, a Dual Role Device (DRD) is a device that is capable of being either a host or a peripheral. Any OTG DRD must support Host Negotiation Protocol (HNP).

HNP allows an OTG B-device to temporarily become the USB host. The A-device must first enable the B-device to follow HNP. Refer to the *"On-The-Go Supplement"* to the *"USB 2.0 Specification"* for more information regarding HNP. HNP may only be initiated at full speed.

After being enabled for HNP by the A-device, the B-device requests being the host any time that the USB link is in the suspend state, by simply indicating a disconnect. This can be done in software by clearing DPPULUP and DMPULUP. When the A-device detects the disconnect condition (via the URSTIF (U1IR<0>) interrupt), the A-device may allow the B-device to take over as host. The A-device does this by signaling connect as a full-speed function. Software may accomplish this by setting DPPULUP.

If the A-device responds instead with resume signaling, the A-device remains as host. When the B-device detects the connect condition (via ATTACHIF, U1IR<6>), the B-device becomes host. The B-device drives Reset signaling prior to using the bus.

When the B-device has finished in its role as host, it stops all bus activity and turns on its D+ pull-up resistor by setting DPPULUP. When the A-device detects a suspend condition (Idle for 3 ms), the A-device turns off its D+ pull-up. The A-device may also power down the VBUS supply to end the session. When the A-device detects the connect condition (via ATTACHIF), the A-device resumes host operation and drives Reset signaling.

20.7 USB OTG Module Registers

There are a total of 37 memory-mapped registers associated with the USB OTG module. They can be divided into four general categories:

- USB OTG Module Control (12)
- USB Interrupt (7)
- USB Endpoint Management (16)
- USB VBUS Power Control (2)

This total does not include the (up to) 128 BD registers in the BDT. Their prototypes, described in Register 20-1 and Register 20-2, are shown separately in **Section 20.2 "USB Buffer Descriptors and the BDT"**.

All USB OTG registers are implemented in the Least Significant Byte (LSB) of the register. Bits in the upper byte are unimplemented and have no function. Note that some registers are instantiated only in Host mode, while other registers have different bit instantiations and functions in Device and Host modes.

The registers described in the following sections are those that have bits with specific control and configuration features. The following registers are used for data or address values only:

- U1BDTP1, U1BDTP2 and U1BDTP3: Specifies the 256-word page in data RAM used for the BDT; 8-bit value with bit 0 fixed as '0' for boundary alignment.
- U1FRML and U1FRMH: Contains the 11-bit byte counter for the current data frame.

REGISTER 22-3: RTCCON2L: RTCC CONTROL REGISTER 2 (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
FDIV4	FDIV3	FDIV2	FDIV1	FDIV0	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
PWCPS1	PWCPS0	PS1	PS0	—	—	CLKSEL1	CLKSEL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **FDIV<4:0>:** Fractional Clock Divide bits
00000 = No fractional clock division.
00001 = Increase period by 1 RTCC input clock cycle every 16 seconds
00010 = Increase period by 2 RTCC input clock cycles every 16 seconds
•
•
•
11101 = Increase period by 30 RTCC input clock cycles every 16 seconds
11111 = Increase period by 31 RTCC input clock cycles every 16 seconds

bit 10-8 **Unimplemented:** Read as '0'

bit 7-6 **PWCPS<1:0>:** Power Control Prescale Select bits
00 = 1:1
01 = 1:16
10 = 1:64
11 = 1:256

bit 5-4 **PS<1:0>:** Prescale Select bits
00 = 1:1
01 = 1:16
10 = 1:64
11 = 1:256

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CLKSEL<1:0>:** Clock Select bits
00 = SOSC
01 = LPRC
10 = PWRLCLK pin
11 = System clock

REGISTER 22-18: TSADATEH: RTCC TIMESTAMP A DATE REGISTER (HIGH)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	MTHTEN	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **YRTEN<3:0>:** Binary Coded Decimal Value of Years ‘10’ Digit bits

bit 11-8 **YRONE<3:0>:** Binary Coded Decimal Value of Years ‘1’ Digit bits

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **MTHTEN:** Binary Coded Decimal Value of Months ‘10’ Digit bit
Contains a value from 0 to 1.

bit 3-0 **MTHONE<2:0>:** Binary Coded Decimal Value of Months ‘1’ Digit bits
Contains a value from 0 to 9.

Note 1: If TSAEN = 0, bits<15:0> can be used for persistence storage throughout a non-Power-on Reset ($\overline{\text{MCLR}}$, WDT, etc.).

22.4 Calibration

22.4.1 CLOCK SOURCE CALIBRATION

A crystal oscillator that is connected to the RTCC may be calibrated to provide an accurate 1 second clock in two ways. First, coarse frequency adjustment is performed by adjusting the value written to the DIV<15:0> bits. Secondly, a 5-bit value can be written to the FDIV<4:0> control bits to perform a fine clock division.

The DIVx and FDIVx values can be concatenated and considered as a 21-bit prescaler value. If the oscillator source is slightly faster than ideal, the FDIV<4:0> value can be increased to make a small decrease in the RTC frequency. The value of DIV<15:0> should be increased to make larger decreases in the RTC frequency. If the oscillator source is slower than ideal, FDIV<4:0> may be decreased for small calibration changes and DIV<15:0> may need to be decreased to make larger calibration changes.

Before calibration, the user must determine the error of the crystal. This should be done using another timer resource on the device or an external timing reference. It is up to the user to include in the error value, the initial error of the crystal, drift due to temperature and drift due to crystal aging.

22.5 Alarm

- Configurable from half second to one year
- Enabled using the ALRMEN bit (RTCCON1H<15>)
- One-time alarm and repeat alarm options are available

22.5.1 CONFIGURING THE ALARM

The alarm feature is enabled using the ALRMEN bit. This bit is cleared when an alarm is issued. Writes to ALRMVAL should only take place when ALRMEN = 0.

As shown in Figure 22-2, the interval selection of the alarm is configured through the AMASK<3:0> bits (RTCCON1H<11:8>). These bits determine which and how many digits of the alarm must match the clock value for the alarm to occur.

The alarm can also be configured to repeat based on a preconfigured interval. The amount of times this occurs, once the alarm is enabled, is stored in the ALMRPT<7:0> bits (RTCCON1H<7:0>). When the value of the ALMRPTx bits equals 00h and the CHIME bit (RTCCON1H<14>) is cleared, the repeat function is disabled and only a single alarm will occur. The alarm can be repeated, up to 255 times by loading ALMRPT<7:0> with FFh.

After each alarm is issued, the value of the ALMRPTx bits is decremented by one. Once the value has reached 00h, the alarm will be issued one last time, after which, the ALRMEN bit will be cleared automatically and the alarm will turn off.

Indefinite repetition of the alarm can occur if the CHIME bit = 1. Instead of the alarm being disabled when the value of the ALMRPTx bits reaches 00h, it rolls over to FFh and continues counting indefinitely while CHIME is set.

22.5.2 ALARM INTERRUPT

At every alarm event, an interrupt is generated. This output is completely synchronous to the RTCC clock and can be used as a Trigger clock to the other peripherals.

Note:	Changing any of the register bits, other than the RTCOE bit (RTCCON1L<7>), the ALMRPT<7:0> bits (RTCCON1H<7:0> and the CHIME bit, while the alarm is enabled (ALRMEN = 1), can result in a false alarm event leading to a false alarm interrupt. To avoid a false alarm event, the timer and alarm values should only be changed while the alarm is disabled (ALRMEN = 0).

23.1 User Interface

23.1.1 POLYNOMIAL INTERFACE

The CRC module can be programmed for CRC polynomials of up to the 32nd order, using up to 32 bits.

Polynomial length, which reflects the highest exponent in the equation, is selected by the PLEN<4:0> bits (CRCCON2<4:0>).

The CRCXORL and CRCXORH registers control which exponent terms are included in the equation. Setting a particular bit includes that exponent term in the equation. Functionally, this includes an XOR operation on the corresponding bit in the CRC engine. Clearing the bit disables the XOR.

For example, consider two CRC polynomials, one a 16-bit and the other a 32-bit equation.

EQUATION 23-1: 16-BIT, 32-BIT CRC POLYNOMIALS

$$X16 + X12 + X5 + 1$$

and

$$X32+X26 + X23 + X22 + X16 + X12 + X11 + X10 + X8 + X7 + X5 + X4 + X2 + X + 1$$

To program these polynomials into the CRC generator, set the register bits, as shown in Table 23-1.

Note that the appropriate positions are set to '1' to indicate that they are used in the equation (for example, X26 and X23). The '0' bit required by the equation is always XORed; thus, X0 is a don't care. For a polynomial of length 32, it is assumed that the 32nd bit will be used. Therefore, the X<31:1> bits do not have the 32nd bit.

23.1.2 DATA INTERFACE

The module incorporates a FIFO that works with a variable data width. Input data width can be configured to any value between 1 and 32 bits using the DWIDTH<4:0> bits (CRCCON2<12:8>). When the data width is greater than 15, the FIFO is 4 words deep. When the DWIDTHx bits are between 15 and 8, the FIFO is 8 words deep. When the DWIDTHx bits are less than 8, the FIFO is 16 words deep.

The data for which the CRC is to be calculated must first be written into the FIFO. Even if the data width is less than 8, the smallest data element that can be written into the FIFO is 1 byte. For example, if the DWIDTHx bits are 5, then the size of the data is DWIDTH<4:0> + 1 or 6. The data is written as a whole byte; the two unused upper bits are ignored by the module.

Once data is written into the MSb of the CRCDAT registers (that is, the MSb as defined by the data width), the value of the VWORD<4:0> bits (CRCCON1<12:8>) increments by one. For example, if the DWIDTHx bits are 24, the VWORDx bits will increment when bit 7 of CRCDATH is written. Therefore, CRCDATL must always be written to before CRCDATH.

The CRC engine starts shifting data when the CRCGO bit (CRCCON1<4>) is set and the value of the VWORDx bits is greater than zero.

Each word is copied out of the FIFO into a buffer register, which decrements the VWORDx bits. The data is then shifted out of the buffer. The CRC engine continues shifting at a rate of two bits per instruction cycle, until the VWORDx bits reach zero. This means that for a given data width, it takes half that number of instructions for each word to complete the calculation. For example, it takes 16 cycles to calculate the CRC for a single word of 32-bit data.

When the VWORDx bits reach the maximum value for the configured value of the DWIDTHx bits (4, 8 or 16), the CRCFUL bit (CRCCON1<7>) becomes set. When the VWORDx bits reach zero, the CRCMPT bit (CRCCON1<6>) becomes set. The FIFO is emptied and the VWORD<4:0> bits are set to '00000' whenever CRCEN is '0'.

At least one instruction cycle must pass after a write to CRCWDAT before a read of the VWORDx bits is done.

TABLE 23-1: CRC SETUP EXAMPLES FOR 16 AND 32-BIT POLYNOMIALS

CRC Control Bits	Bit Values	
	16-Bit Polynomial	32-Bit Polynomial
PLEN<4:0>	01111	11111
X<31:16>	0000 0000 0000 0001	0000 0100 1100 0001
X<15:1>	0001 0000 0010 000	0001 1101 1011 011

REGISTER 25-3: AD1CON3: A/D CONTROL REGISTER 3

R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC(1)	EXTSAM	PUMPEN(2)	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ADRC:** A/D Conversion Clock Source bit(1)
1 = Dedicated ADC RC clock generator (4 MHz nominal)
0 = Clock derived from system clock

bit 14 **EXTSAM:** Extended Sampling Time bit
1 = A/D is still sampling after SAMP = 0
0 = A/D is finished sampling

bit 13 **PUMPEN:** Charge Pump Enable bit(2)
1 = Charge pump for switches is enabled
0 = Charge pump for switches is disabled

bit 12-8 **SAMC<4:0>:** Auto-Sample Time Select bits
11111 = 31 TAD
• • •
00001 = 1 TAD
00000 = 0 TAD

bit 7-0 **ADCS<7:0>:** A/D Conversion Clock Select bits
11111111 = 256 • TCY = TAD
• • •
00000001 = 2 • TCY = TAD
00000000 = TCY = TAD

Note 1: Selecting the internal ADC RC clock requires that ADCSx be '1' or greater. Setting ADCSx = 0 when ADRC = 1 will violate the TAD (min) specification.

2: Enable the charge pump if AVDD is < 2.7V. Longer sample times are required due to the increase of the internal resistance of the MUX if the charge pump is disabled.

26.0 TRIPLE COMPARATOR MODULE

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Scalable Comparator Module"** (DS39734), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

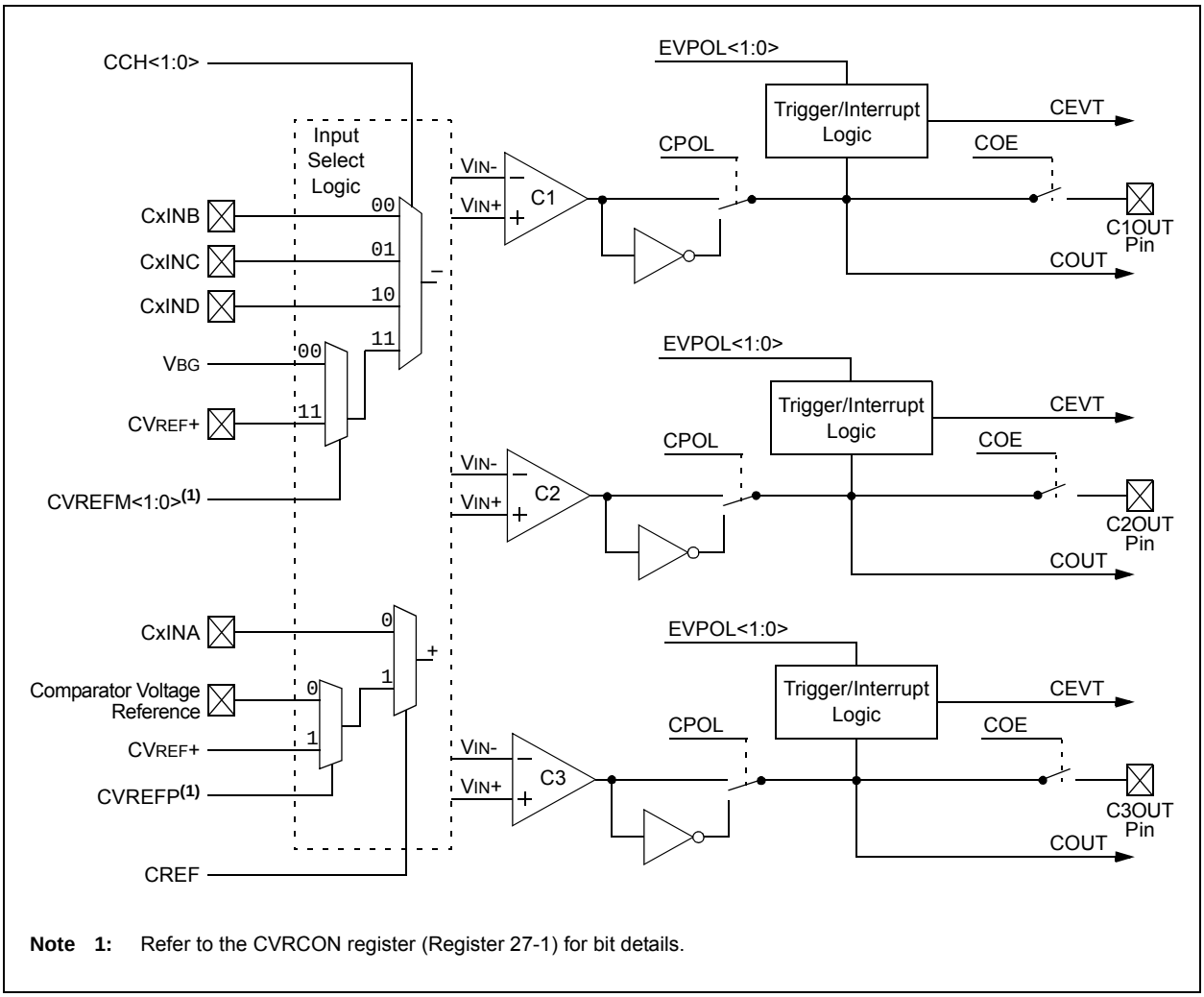
The triple comparator module provides three dual input comparators. The inputs to the comparator can be configured to use any one of five external analog inputs (CxINA, CxINB, CxINC, CxIND and CVREF+) and a voltage reference input from one of the internal band gap references or the comparator voltage reference generator (VBG and CVREF).

The comparator outputs may be directly connected to the CxOUT pins. When the respective COE bit equals '1', the I/O pad logic makes the unsynchronized output of the comparator available on the pin.

A simplified block diagram of the module in shown in Figure 26-1. Diagrams of the possible individual comparator configurations are shown in Figure 26-2 through Figure 26-4.

Each comparator has its own control register, CMxCON (Register 26-1), for enabling and configuring its operation. The output and event status of all three comparators is provided in the CMSTAT register (Register 26-2).

FIGURE 26-1: TRIPLE COMPARATOR MODULE BLOCK DIAGRAM



Note 1: Refer to the CVRCON register (Register 27-1) for bit details.

TABLE 30-1: CONFIGURATION WORD ADDRESSES

Configuration Registers	Single Partition Mode			
	PIC24FJ1024GX6XX	PIC24FJ512GX6XX	PIC24FJ256GX6XX	PIC24FJ128GX6XX
FSEC	0ABF00h	055F00h	02AF00h	015F00h
FBSLIM	0ABF10h	055F10h	02AF10h	015F10h
FSIGN	0ABF14h	055F14h	02AF14h	015F14h
FOSCSEL	0ABF18h	055F18h	02AF18h	015F18h
FOSC	0ABF1Ch	055F1Ch	02AF1Ch	015F1Ch
FWDT	0ABF20h	055F20h	02AF20h	015F20h
FPOR	0ABF24h	055F24h	02AF24h	015F24h
FICD	0ABF28h	055F28h	02AF28h	015F28h
FDEVOPT1	0ABF2Ch	055F2Ch	02AF2Ch	015F2Ch
FBOOT	801800h			
	Dual Partition Modes(1)			
FSEC(2)	055F00h/455F00h	02AF00h/42AF00h	015700h/415700h	00AF00h/40AF00h
FBSLIM(2)	055F10h/455F10h	02AF10h/42AF10h	015710h/415710h	00AF10h/40AF10h
FSIGN(2)	055F14h/455F14h	02AF14h/42AF14h	015714h/ 415714h	00AF14h/40AF14h
FOSCSEL	055F18h/455F18h	02AF18h/42AF18h	015718h/415718h	00AF18h/40AF18h
FOSC	055F1Ch/455F1Ch	02AF1Ch/42AF1Ch	01571Ch/41571Ch	00AF1Ch/40AF1Ch
FWDT	055F20h/455F20h	02AF20h/42AF20h	015720h/415720h	00AF20h/40AF20h
FPOR	055F24h/ 455F24h	02AF24h/42AF24h	015724h/415724h	00AF24h/40AF24h
FICD	055F28h/455F28h	02AF28h/42AF28h	015728h/415728h	00AF28h/40AF28h
FDEVOPT1	055F2Ch/455F2Ch	02AF2Ch/42AF2Ch	01572Ch/41572Ch	00AF2Ch/40AF2Ch
FBTSEQ(3)	055FFCh/455FFCh	02AFFCh/42AFFCh	0157FCh/4157FCh	00AFFCh/40AFFCh
FBOOT	801800h			

Note 1: Addresses shown for Dual Partition modes are for the Active/Inactive Partitions, respectively.

2: Changes to these Inactive Partition Configuration Words affect how the Active Partition accesses the Inactive Partition.

3: FBTSEQ is a 24-bit Configuration Word, using all three bytes of the program memory width.

NOTES:

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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