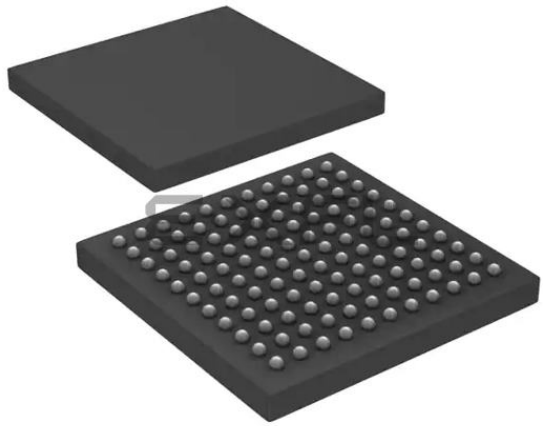
Microchip Technology - PIC24FJ256GA610T-I/BG Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, HLVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256ga610t-i-bg

2.6 External Oscillator Pins

Many microcontrollers have options for at least two oscillators: a high-frequency Primary Oscillator and a low-frequency Secondary Oscillator (refer to **Section 9.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins with no more than 0.5 inch (12 mm) between the circuit components and the pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

Layout suggestions are shown in Figure 2-5. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

In planning the application's routing and I/O assignments, ensure that adjacent port pins, and other signals in close proximity to the oscillator, are benign (i.e., free of high frequencies, short rise and fall times and other similar noise).

For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate web site (www.microchip.com):

- *AN943, "Practical PICmicro® Oscillator Analysis and Design"*
- *AN949, "Making Your Oscillator Work"*
- *AN1798, "Crystal Selection for Low-Power Secondary Oscillator"*

FIGURE 2-5: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT

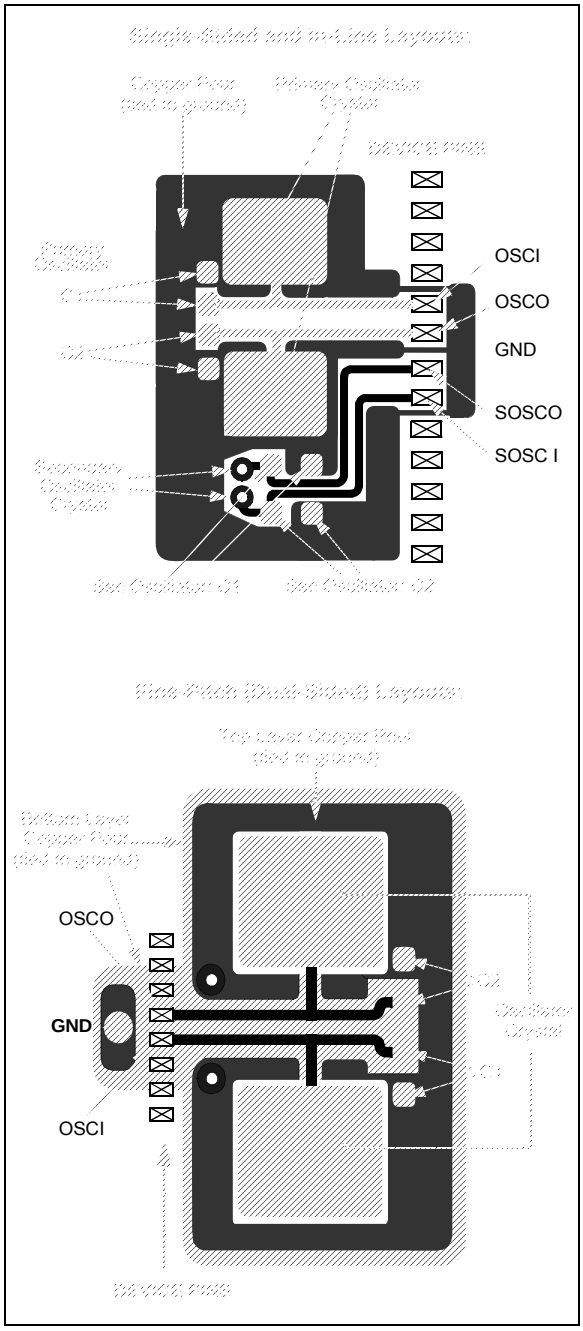


TABLE 4-2: CONFIGURATION WORD ADDRESSES

Configuration Register	Single Partition Mode			
	PIC24FJ1024GX6XX	PIC24FJ512GX6XX	PIC24FJ256GX6XX	PIC24FJ128GX6XX
FSEC	0ABF00h	055F00h	02AF00h	015F00h
FBSLIM	0ABF10h	055F10h	02AF10h	015F10h
FSIGN	0ABF14h	055F14h	02AF14h	015F14h
FOSCSEL	0ABF18h	055F18h	02AF18h	015F18h
FOSC	0ABF1Ch	055F1Ch	02AF1Ch	015F1Ch
FWDT	0ABF20h	055F20h	02AF20h	015F20h
FPOR	0ABF24h	055F24h	02AF24h	015F24h
FICD	0ABF28h	055F28h	02AF28h	015F28h
FDEVOPT1	0ABF2Ch	055F2Ch	02AF2Ch	015F2Ch
FBOOT	801800h			
	Dual Partition Modes(1)			
FSEC(2)	055F00h/455F00h	02AF00h/42AF00h	015700h/415700h	00AF00h/40AF00h
FBSLIM(2)	055F10h/455F10h	02AF10h/42AF10h	015710h/415710h	00AF10h/40AF10h
FSIGN(2)	055F14h/455F14h	02AF14h/42AF14h	015714h/415714h	00AF14h/40AF14h
FOSCSEL	055F18h/455F18h	02AF18h/42AF18h	015718h/415718h	00AF18h/40AF18h
FOSC	055F1Ch/455F1Ch	02AF1Ch/42AF1Ch	01571Ch/41571Ch	00AF1Ch/40AF1Ch
FWDT	055F20h/455F20h	02AF20h/42AF20h	015720h/415720h	00AF20h/40AF20h
FPOR	055F24h/455F24h	02AF24h/42AF24h	015724h/415724h	00AF24h/40AF24h
FICD	055F28h/455F28h	02AF28h/42AF28h	015728h/415728h	00AF28h/40AF28h
FDEVOPT1	055F2Ch/455F2Ch	02AF2Ch/42AF2Ch	01572Ch/41572Ch	00AF2Ch/40AF2Ch
FBTSEQ(3)	055FFCh/455FFCh	02AFFCh/42AFFCh	0157FCh/4157FCh	00AFFCh/40AFFCh
FBOOT	801800h			

Note 1: Addresses shown for Dual Partition modes are for the Active/Inactive Partitions, respectively.

2: Changes to these Inactive Partition Configuration Words affect how the Active Partition accesses the Inactive Partition.

3: FBTSEQ is a 24-bit Configuration Word, using all three bytes of the program memory width.

4.2.5.1 Data Read from EDS

In order to read the data from the EDS space, first, an Address Pointer is set up by loading the required EDS page number into the DSRPAG register and assigning the offset address to one of the W registers. Once the above assignment is done, the EDS window is enabled by setting bit 15 of the Working register which is assigned with the offset address; then, the contents of the pointed EDS location can be read.

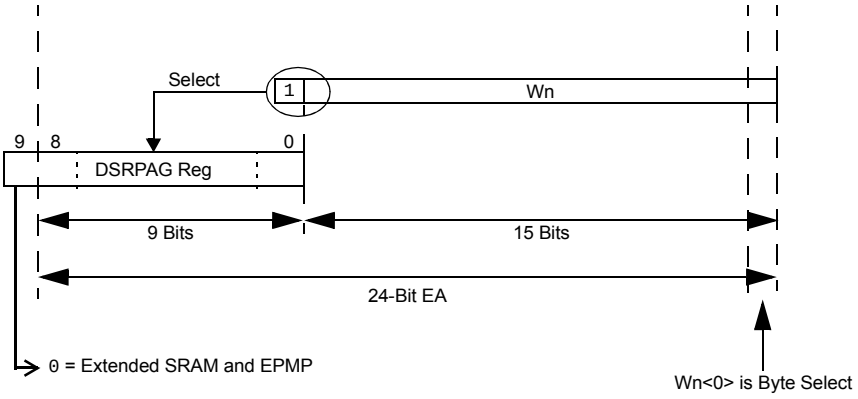
Figure 4-5 illustrates how the EDS space address is generated for read operations.

When the Most Significant bit (MSb) of EA is '1' and DSRPAG<9> = 0, the lower 9 bits of DSRPAG are concatenated to the lower 15 bits of EA to form a 24-bit EDS space address for read operations.

Example 4-1 shows how to read a byte, word and double word from EDS.

Note:	All read operations from EDS space have an overhead of one instruction cycle. Therefore, a minimum of two instruction cycles are required to complete an EDS read. For EDS reads under the REPEAT instruction; the first two accesses take three cycles and the subsequent accesses take one cycle.

FIGURE 4-5: EDS ADDRESS GENERATION FOR READ OPERATIONS



EXAMPLE 4-1: EDS READ CODE IN ASSEMBLY

```
; Set the EDS page from where the data to be read
    mov         #0x0002, w0
    mov         w0, DSRPAG      ;page 2 is selected for read
    mov         #0x0800, w1     ;select the location (0x800) to be read
    bset        w1, #15         ;set the MSB of the base address, enable EDS mode

;Read a byte from the selected location
    mov.b       [w1++], w2      ;read Low byte
    mov.b       [w1++], w3      ;read High byte

;Read a word from the selected location
    mov         [w1], w2        ;

;Read Double - word from the selected location
    mov.d       [w1], w2        ;two word read, stored in w2 and w3
```

REGISTER 5-2: DMACHn: DMA CHANNEL n CONTROL REGISTER

U-0	U-0	U-0	r-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	NULLW	RELOAD(1)	CHREQ(3)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SAMODE1	SAMODE0	DAMODE1	DAMODE0	TRMODE1	TRMODE0	SIZE	CHEN
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **Reserved:** Maintain as '0'

bit 11 **Unimplemented:** Read as '0'

bit 10 **NULLW:** Null Write Mode bit
- 1 = A dummy write is initiated to DMASRCn for every write to DMADSTn
- 0 = No dummy write is initiated

bit 9 **RELOAD:** Address and Count Reload bit(1)
- 1 = DMASRCn, DMADSTn and DMACNTn registers are reloaded to their previous values upon the start of the next operation
- 0 = DMASRCn, DMADSTn and DMACNTn are not reloaded on the start of the next operation(2)

bit 8 **CHREQ:** DMA Channel Software Request bit(3)
- 1 = A DMA request is initiated by software; automatically cleared upon completion of a DMA transfer
- 0 = No DMA request is pending

bit 7-6 **SAMODE<1:0>:** Source Address Mode Selection bits
- 11 = DMASRCn is used in Peripheral Indirect Addressing and remains unchanged
- 10 = DMASRCn is decremented based on the SIZE bit after a transfer completion
- 01 = DMASRCn is incremented based on the SIZE bit after a transfer completion
- 00 = DMASRCn remains unchanged after a transfer completion

bit 5-4 **DAMODE<1:0>:** Destination Address Mode Selection bits
- 11 = DMADSTn is used in Peripheral Indirect Addressing and remains unchanged
- 10 = DMADSTn is decremented based on the SIZE bit after a transfer completion
- 01 = DMADSTn is incremented based on the SIZE bit after a transfer completion
- 00 = DMADSTn remains unchanged after a transfer completion

bit 3-2 **TRMODE<1:0>:** Transfer Mode Selection bits
- 11 = Repeated Continuous mode
- 10 = Continuous mode
- 01 = Repeated One-Shot mode
- 00 = One-Shot mode

bit 1 **SIZE:** Data Size Selection bit
- 1 = Byte (8-bit)
- 0 = Word (16-bit)

bit 0 **CHEN:** DMA Channel Enable bit
- 1 = The corresponding channel is enabled
- 0 = The corresponding channel is disabled

Note 1: Only the original DMACNTn is required to be stored to recover the original DMASRCn and DMADSTn.

2: DMASRCn, DMADSTn and DMACNTn are always reloaded in Repeated mode transfers (DMACHn<2> = 1), regardless of the state of the RELOAD bit.

3: The number of transfers executed while CHREQ is set depends on the configuration of TRMODE<1:0>.

8.0 INTERRUPT CONTROLLER

Note 1: This data sheet summarizes the features of the PIC24FJ1024GA610/GB610 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Interrupts"** (DS70000600) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The PIC24FJ1024GA610/GB610 family interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the PIC24FJ1024GA610/GB610 family CPU.

The interrupt controller has the following features:

- Up to Eight Processor Exceptions and Software Traps
- Seven User-Selectable Priority Levels
- Interrupt Vector Table (IVT) with a Unique Vector for Each Interrupt or Exception Source
- Fixed Priority within a Specified User Priority Level
- Fixed Interrupt Entry and Return Latencies

8.1 Interrupt Vector Table

The PIC24FJ1024GA610/GB610 family Interrupt Vector Table (IVT), shown in Figure 8-1, resides in program memory starting at location, 000004h. The IVT contains 6 non-maskable trap vectors and up to 118 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

8.1.1 ALTERNATE INTERRUPT VECTOR TABLE

The Alternate Interrupt Vector Table (AIVT) is located after the IVT, as shown in Figure 8-1. The AIVTEN (INTCON2<8>) control bit provides access to the AIVT. If the AIVTEN bit is set, all interrupt and exception processes will use the alternate vectors instead of the default vectors. The alternate vectors are organized in the same manner as the default vectors.

The AIVT is available only if the Boot Segment has been defined and the AIVT has been enabled. To enable the AIVT, both the Configuration bit, AIVTDIS (FSEC<15>), and the AIVTEN bit (INTCON2<8> in the SFR), have to be set. When the AIVT is enabled, all interrupts and exception processes use the alternate vectors instead of the default vectors. The AIVT begins at the start of the last page of the Boot Segment (BS) defined by the BSLIM<12:0> bits. The AIVT address is: (BSLIM<12:0> – 1) x 0x800.

8.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The PIC24FJ1024GA610/GB610 family devices clear their registers in response to a Reset, which forces the PC to zero. The device then begins program execution at location, 0x000000. A GOTO instruction at the Reset address can redirect program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

11.4.6 PERIPHERAL PIN SELECT REGISTERS

The PIC24FJ1024GA610/GB610 family of devices implements a total of 40 registers for remappable peripheral configuration:

- Input Remappable Peripheral Registers (24)
- Output Remappable Peripheral Registers (16)

Note: Input and Output register values can only be changed if IOLOCK (OSCCON<6>) = 0. See **Section 11.4.4.1 "Control Register Lock"** for a specific command sequence.

REGISTER 11-12: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	INT1R5	INT1R4	INT1R3	INT1R2	INT1R1	INT1R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	OCTRIG1R5	OCTRIG1R4	OCTRIG1R3	OCTRIG1R2	OCTRIG1R1	OCTRIG1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **INT1R<5:0>:** Assign External Interrupt 1 (INT1) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **OCTRIG1R<5:0>:** Assign Output Compare Trigger 1 to Corresponding RPn or RPIn Pin bits

REGISTER 11-13: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	INT3R5	INT3R4	INT3R3	INT3R2	INT3R1	INT3R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	INT2R5	INT2R4	INT2R3	INT2R2	INT2R1	INT2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **INT3R<5:0>:** Assign External Interrupt 3 (INT3) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **INT2R<5:0>:** Assign External Interrupt 2 (INT2) to Corresponding RPn or RPIn Pin bits

REGISTER 11-34: RPINR28: PERIPHERAL PIN SELECT INPUT REGISTER 28

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SCK3R5	SCK3R4	SCK3R3	SCK3R2	SCK3R1	SCK3R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SDI3R5	SDI3R4	SDI3R3	SDI3R2	SDI3R1	SDI3R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **SCK3R<5:0>:** Assign SPI3 Clock Input (SCK3IN) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **SDI3R<5:0>:** Assign SPI3 Data Input (SDI3) to Corresponding RPn or RPIn Pin bits

REGISTER 11-35: RPINR29: PERIPHERAL PIN SELECT INPUT REGISTER 29

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SS3R5	SS3R4	SS3R3	SS3R2	SS3R1	SS3R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **SS3R<5:0>:** Assign SPI3 Slave Select Input (SS3IN) to Corresponding RPn or RPIn Pin bits

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER(1)

R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
TON	—	TSIDL	—	—	—	TECS1	TECS0
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
—	TGATE	TCKPS1	TCKPS0	—	TSYNC	TCS	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timer1 On bit
1 = Starts 16-bit Timer1
0 = Stops 16-bit Timer1

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timer1 Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9-8 **TECS<1:0>:** Timer1 Extended Clock Source Select bits (selected when TCS = 1)
11 = Generic timer (TxCK) external input
10 = LPRC Oscillator
01 = T1CK external clock input
00 = SOSC

bit 7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timer1 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3 **Unimplemented:** Read as '0'

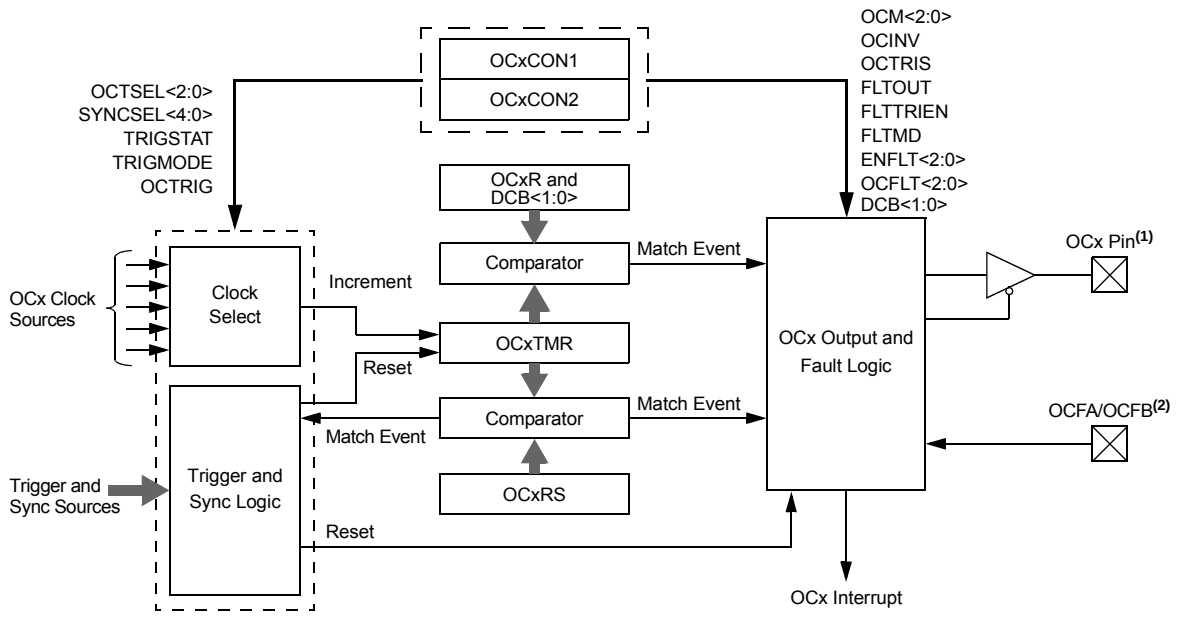
bit 2 **TSYNC:** Timer1 External Clock Input Synchronization Select bit
When TCS = 1:
1 = Synchronizes the external clock input
0 = Does not synchronize the external clock input
When TCS = 0:
This bit is ignored.

bit 1 **TCS:** Timer1 Clock Source Select bit
1 = Extended clock is selected by the timer
0 = Internal clock (FOSC/2)

bit 0 **Unimplemented:** Read as '0'

Note 1: Changing the value of T1CON while the timer is running (TON = 1) causes the timer prescale counter to reset and is not recommended.

FIGURE 15-1: OUTPUT COMPARE x BLOCK DIAGRAM (16-BIT MODE)



Note 1: The OCx outputs must be assigned to an available RPn pin before use. See **Section 11.4 "Peripheral Pin Select (PPS)"** for more information.

2: The OCFA/OCFB Fault inputs must be assigned to an available RPn/RPIn pin before use. See **Section 11.4 "Peripheral Pin Select (PPS)"** for more information.

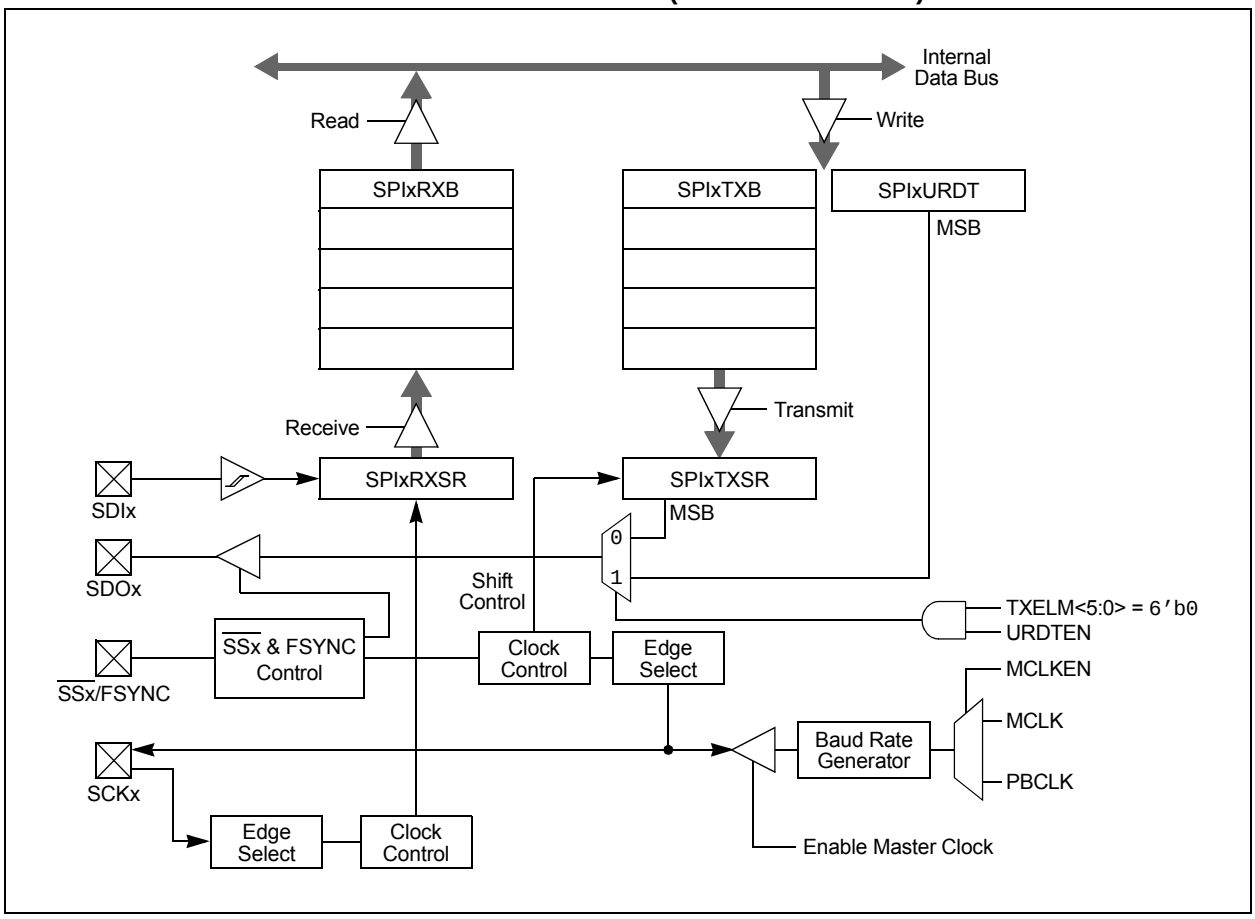
15.2 Compare Operations

In Compare mode (Figure 15-1), the output compare module can be configured for Single-Shot or Continuous mode pulse generation. It can also repeatedly toggle an output pin on each timer event.

To set up the module for compare operations:

1. Configure the OCx output for one of the available Peripheral Pin Select pins if available on the OCx module you are using. Otherwise, configure the dedicated OCx output pins.
2. Calculate the required values for the OCxR and (for Double Compare modes) OCxRS Duty Cycle registers:
   a) Determine the instruction clock cycle time. Take into account the frequency of the external clock to the timer source (if one is used) and the timer prescaler settings.
   b) Calculate the time to the rising edge of the output pulse relative to the timer start value (0000h).
   c) Calculate the time to the falling edge of the pulse based on the desired pulse width and the time to the rising edge of the pulse.
3. Write the rising edge value to OCxR and the falling edge value to OCxRS.
4. Set the Timer Period register, PRy, to a value equal to or greater than the value in OCxRS.
5. Set the OCM<2:0> bits for the appropriate compare operation (= `0xx`).
6. For Trigger mode operations, set OCTRIG to enable Trigger mode. Set or clear TRIGMODE to configure Trigger operation and TRIGSTAT to select a hardware or software Trigger. For Synchronous mode, clear OCTRIG.
7. Set the SYNCSEL<4:0> bits to configure the Trigger or Sync source. If free-running timer operation is required, set the SYNCSELx bits to '`00000`' (no Sync/Trigger source).
8. Select the time base source with the OCTSEL<2:0> bits. If necessary, set the TON bit for the selected timer, which enables the compare time base to count. Synchronous mode operation starts as soon as the time base is enabled; Trigger mode operation starts after a Trigger source event occurs.

FIGURE 17-1: SPIx MODULE BLOCK DIAGRAM (ENHANCED MODE)



17.3 Audio Mode Operation

To initialize the SPIx module for Audio mode, follow the steps to initialize it for Master/Slave mode, but also set the AUDEN bit (SPIxCON1H<15>). In Master+Audio mode:

- This mode enables the device to generate SCKx and LRC pulses as long as the SPIEN bit (SPIxCON1L<15>) = 1.
- The SPIx module generates LRC and SCKx continuously in all cases, regardless of the transmit data, while in Master mode.
- The SPIx module drives the leading edge of LRC and SCKx within 1 SCKx period, and the serial data shifts in and out continuously, even when the TX FIFO is empty.

In Slave+Audio mode:

- This mode enables the device to receive SCKx and LRC pulses as long as the SPIEN bit (SPIxCON1L<15>) = 1.
- The SPIx module drives zeros out of SDOx, but does not shift data out or in (SDIx) until the module receives the LRC (i.e., the edge that precedes the left channel).
- Once the module receives the leading edge of LRC, it starts receiving data if DISSDI (SPIxCON1L<4>) = 0 and the serial data shifts out continuously, even when the TX FIFO is empty.

20.2 USB Buffer Descriptors and the BDT

Endpoint buffer control is handled through a structure called the Buffer Descriptor Table (BDT). This provides a flexible method for users to construct and control endpoint buffers of various lengths and configurations.

The BDT can be located in any available 512-byte, aligned block of data RAM. The BDT Pointer (U1BDTP1) contains the upper address byte of the BDT and sets the location of the BDT in RAM. The user must set this pointer to indicate the table's location.

The BDT is composed of Buffer Descriptors (BDs) which are used to define and control the actual buffers in the USB RAM space. Each BD consists of two 16-bit, "soft" (non-fixed-address) registers, BDnSTAT and BDnADR, where n represents one of the 64 possible BDs (range of 0 to 63). BDnSTAT is the status register for BDn, while BDnADR specifies the starting address for the buffer associated with BDn.

Note: Since BDnADR is a 16-bit register, only the first 64 Kbytes of RAM can be accessed by the USB module.

Depending on the endpoint buffering configuration used, there are up to 64 sets of Buffer Descriptors, for a total of 256 bytes. At a minimum, the BDT must be at least 8 bytes long. This is because the *"USB 2.0 Specification"* mandates that every device must have Endpoint 0 with both input and output for initial setup.

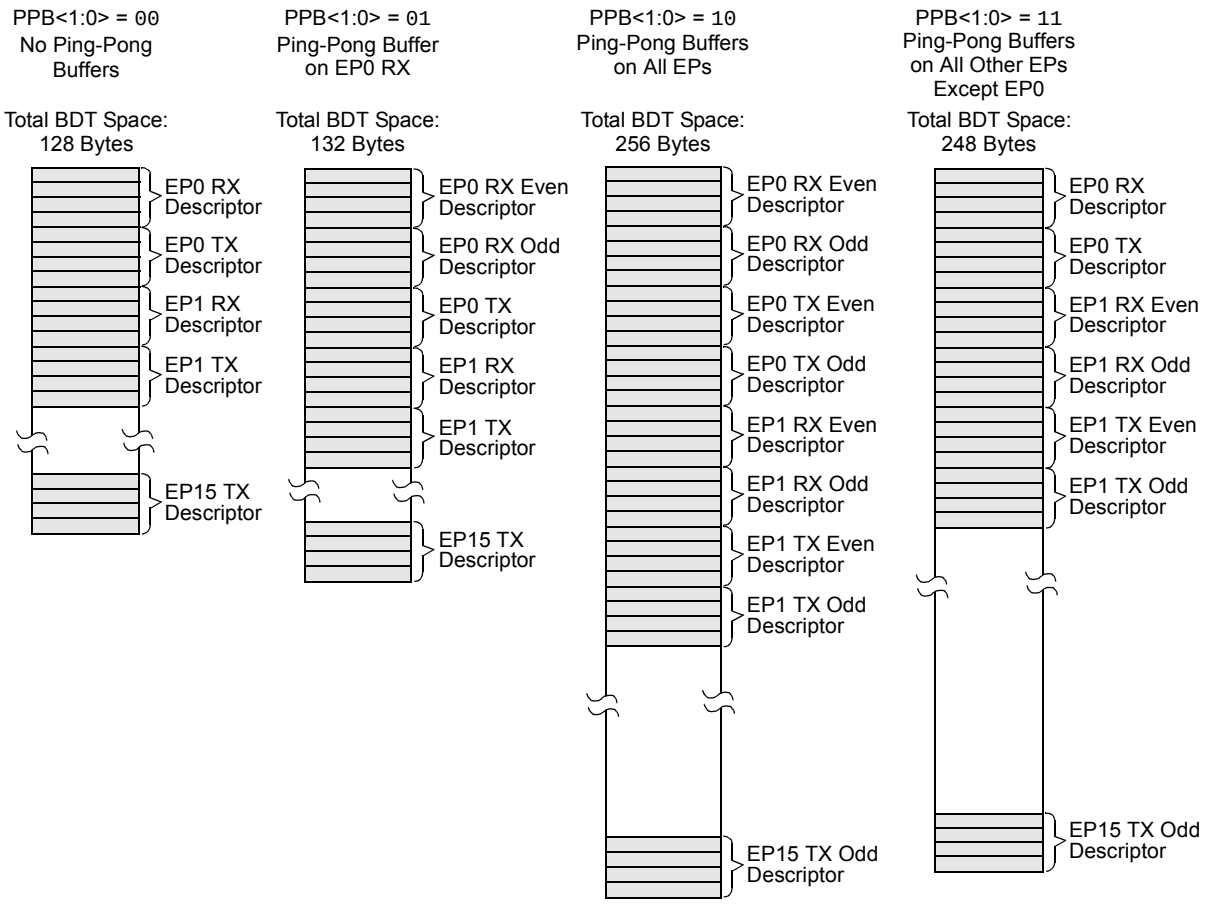
Endpoint mapping in the BDT is dependent on three variables:

- Endpoint number (0 to 15)
- Endpoint direction (RX or TX)
- Ping-pong settings (U1CNFG1<1:0>)

Figure 20-7 illustrates how these variables are used to map endpoints in the BDT.

In Host mode, only Endpoint 0 Buffer Descriptors are used. All transfers utilize the Endpoint 0 Buffer Descriptor and Endpoint Control register (U1EP0). For received packets, the attached device's source endpoint is indicated by the value of ENDPT<3:0> in the USB Status register (U1STAT<7:4>). For transmitted packets, the attached device's destination endpoint is indicated by the value written to the USB Token register (U1TOK).

FIGURE 20-7: BDT MAPPING FOR ENDPOINT BUFFERING MODES



Note: Memory area is not shown to scale.

REGISTER 21-1: PMCON1: EPMP CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
PMPEN	—	PSIDL	ADRMUX1	ADRMUX0	—	MODE1	MODE0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
CSF1	CSF0	ALP	ALMODE	—	BUSKEEP	IRQM1	IRQM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PMPEN:** Parallel Master Port Enable bit
1 = EPMP is enabled
0 = EPMP is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **PSIDL:** Parallel Master Port Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
11 = Lower address bits are multiplexed with data bits using 3 address phases
10 = Lower address bits are multiplexed with data bits using 2 address phases
01 = Lower address bits are multiplexed with data bits using 1 address phase
00 = Address and data appear on separate pins

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **MODE<1:0>:** Parallel Port Mode Select bits
11 = Master mode
10 = Enhanced PSP; pins used are PMRD, PMWR, PMCS, PMD<7:0> and PMA<1:0>
01 = Buffered PSP; pins used are PMRD, PMWR, PMCS and PMD<7:0>
00 = Legacy Parallel Slave Port; pins used are PMRD, PMWR, PMCS and PMD<7:0>

bit 7-6 **CSF<1:0>:** Chip Select Function bits
11 = Reserved
10 = PMA15 is used for Chip Select 2, PMA14 is used for Chip Select 1
01 = PMA15 is used for Chip Select 2, PMCS1 is used for Chip Select 1
00 = PMCS2 is used for Chip Select 2, PMCS1 is used for Chip Select 1

bit 5 **ALP:** Address Latch Polarity bit
1 = Active-high (PMALL, PMALH and PMALU)
0 = Active-low ($\overline{\text{PMALL}}$, $\overline{\text{PMALH}}$ and $\overline{\text{PMALU}}$)

bit 4 **ALMODE:** Address Latch Strobe Mode bit
1 = Enables "smart" address strobes (each address phase is only present if the current access would cause a different address in the latch than the previous address)
0 = Disables "smart" address strobes

bit 3 **Unimplemented:** Read as '0'

bit 2 **BUSKEEP:** Bus Keeper bit
1 = Data bus keeps its last value when not actively being driven
0 = Data bus is in a high-impedance state when not actively being driven

bit 1-0 **IRQM<1:0>:** Interrupt Request Mode bits
11 = Interrupt is generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode), or on a read or write operation when PMA<1:0> = 11 (Addressable PSP mode only)
10 = Reserved
01 = Interrupt is generated at the end of a read/write cycle
00 = No interrupt is generated

REGISTER 21-8: PMSTAT: EPMP STATUS REGISTER (SLAVE MODE ONLY)

R-0, HSC	R/W-0, HS	U-0	U-0	R-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IBF	IBOV	—	—	IB3F(1)	IB2F(1)	IB1F(1)	IB0F(1)
bit 15							bit 8

R-1, HSC	R/W-0, HS	U-0	U-0	R-1, HSC	R-1, HSC	R-1, HSC	R-1, HSC
OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E
bit 7							bit 0

Legend:	HS = Hardware Settable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **IBF:** Input Buffer Full Status bit
1 = All writable Input Buffer registers are full
0 = Some or all of the writable Input Buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit
1 = A write attempt to a full Input register occurred (must be cleared in software)
0 = No overflow occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IB3F:IB0F:** Input Buffer x Status Full bits(1)
1 = Input buffer contains unread data (reading the buffer will clear this bit)
0 = Input buffer does not contain unread data

bit 7 **OBE:** Output Buffer Empty Status bit
1 = All readable Output Buffer registers are empty
0 = Some or all of the readable Output Buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit
1 = A read occurred from an empty Output Buffer register (must be cleared in software)
0 = No underflow occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OB3E:OB0E:** Output Buffer x Status Empty bit
1 = Output Buffer x is empty (writing data to the buffer will clear this bit)
0 = Output Buffer x contains untransmitted data

Note 1: Even though an individual bit represents the byte in the buffer, the bits corresponding to the word (Byte 0 and 1, or Byte 2 and 3) get cleared, even on byte reading.

REGISTER 25-7: ANCFG: A/D BAND GAP REFERENCE CONFIGURATION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	VBGUSB(1)	VBGADC(1)	VBGCMP(1)	VBGEN(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **VBGUSB:** Band Gap Reference Enable for USB bit(1)
1 = Band gap reference is enabled
0 = Band gap reference is disabled

bit 2 **VBGADC:** Band Gap Reference Enable for A/D bit(1)
1 = Band gap reference is enabled
0 = Band gap reference is disabled

bit 1 **VBGCMP:** Band Gap Reference Enable for CTMU and Comparator bit(1)
1 = Band gap reference is enabled
0 = Band gap reference is disabled

bit 0 **VBGEN:** Band Gap Reference Enable for VREG, BOR, HLVD, FRC, DCO, NVM and A/D Boost bit(1)
1 = Band gap reference is enabled
0 = Band gap reference is disabled

Note 1: When a module requests a band gap reference voltage, that reference will be enabled automatically after a brief start-up time. The user can manually enable the band gap references using the ANCFG register before enabling the module requesting the band gap reference to avoid this startup time (~1 ms).

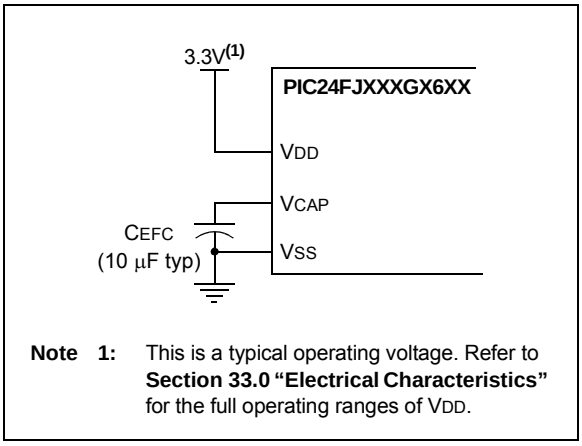
30.3 On-Chip Voltage Regulator

All PIC24FJ1024GA610/GB610 family devices power their core digital logic at a nominal 1.8V. This may create an issue for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the PIC24FJ1024GA610/GB610 family incorporate an on-chip regulator that allows the device to run its core logic from VDD.

This regulator is always enabled. It provides a constant voltage (1.8V nominal) to the digital core logic, from a VDD of about 2.1V, all the way up to the device's VDDMAX. It does not have the capability to boost VDD levels. In order to prevent "brown-out" conditions when the voltage drops too low for the regulator, the Brown-out Reset occurs. Then, the regulator output follows VDD with a typical voltage drop of 300 mV.

A low-ESR capacitor (such as ceramic) must be connected to the VCAP pin (Figure 30-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor (CEFC) is provided in **Section 33.1 "DC Characteristics"**.

FIGURE 30-1: CONNECTIONS FOR THE ON-CHIP REGULATOR



Note 1: This is a typical operating voltage. Refer to **Section 33.0 "Electrical Characteristics"** for the full operating ranges of VDD.

30.3.1 ON-CHIP REGULATOR AND POR

The voltage regulator takes approximately 10 μs for it to generate output. During this time, designated as TVREG, code execution is disabled. TVREG is applied every time the device resumes operation after any power-down, including Sleep mode. TVREG is determined by the status of the VREGS bit (RCON<8>) and the WDTWIN<1:0> Configuration bits (FWDT<9:8>). Refer to **Section 33.0 "Electrical Characteristics"** for more information on TVREG.

Note:	For more information, see **Section 33.0 "Electrical Characteristics"**. The information in this data sheet supersedes the information in the FRM.

30.3.2 VOLTAGE REGULATOR STANDBY MODE

The on-chip regulator always consumes a small incremental amount of current over IDD/IPD, including when the device is in Sleep mode, even though the core digital logic does not require power. To provide additional savings in applications where power resources are critical, the regulator can be made to enter Standby mode on its own whenever the device goes into Sleep mode. This feature is controlled by the VREGS bit (RCON<8>). Clearing the VREGS bit enables the Standby mode. When waking up from Standby mode, the regulator needs to wait for TVREG to expire before wake-up.

30.3.3 LOW-VOLTAGE/RETENTION REGULATOR

When in Sleep mode, PIC24FJ1024GA610/GB610 family devices may use a separate low-power, low-voltage/retention regulator to power critical circuits. This regulator, which operates at 1.2V nominal, maintains power to data RAM and the RTCC while all other core digital logic is powered down. The low-voltage/retention regulator is described in more detail in **Section 10.2.4 "Low-Voltage Retention Regulator"**.

31.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

31.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

31.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

31.9 PICkit 3 In-Circuit Debugger/ Programmer

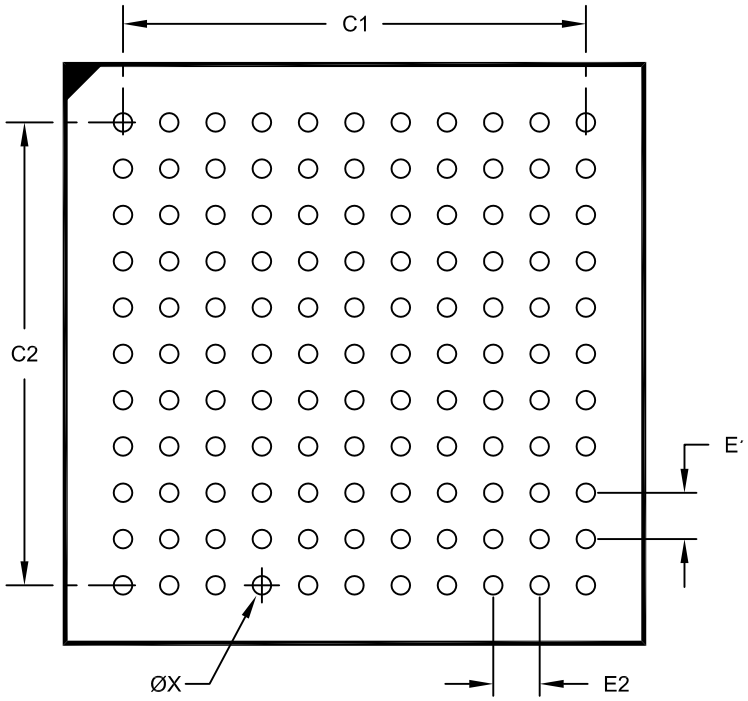
The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

31.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA--Formerly XBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E1		0.80 BSC	
Contact Pitch	E2		0.80 BSC	
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Diameter (X121)	X			0.32

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2148 Rev D

APPENDIX A: REVISION HISTORY

Revision A (March 2015)

Original data sheet for the PIC24FJ1024GA610/GB610 family of devices.

Revision B (November 2015)

This revision incorporates the following updates:

- Sections:
  - Changed 12-bit conversion rate to 200 ksps in the Analog Features section on Page 1.
  - Added Smart Card support (ISO 7816) information to the Peripheral Features section on Page 2.
  - Added **Section 9.3.1 "DCO Overview"**.
  - Added **Section 25.4 "Achieving Maximum A/D Converter (ADC) Performance"**.
  - Added **Section 30.2 "Unique Device Identifier (UDID)"**.
  - Updated **Section 6.6 "Programming Operations"**, **Section 9.6 "PLL Oscillator Modes and USB Operation"**, **Section 9.6.1 "Considerations for USB Operation"**, **Section 9.7 "Reference Clock Output"**, **Section 9.8 "Secondary Oscillator"**, **Section 10.2 "Instruction-Based Power-Saving Modes"**, **Section 10.2.2 "Idle Mode"**, **Section 12.0 "Timer1"**, **Section 16.1 "Time Base Generator"** and **Section 33.0 "Electrical Characteristics"**
- Registers
  - Updated Register 5-1, Register 6-1, Register 7-1, Register 9-4, Register 9-5, Register 18-1, Register 22-3, Register 25-2, Register 25-3, Register 25-6, Register 25-7, Register 30-1, Register 30-5, Register 30-7, Register 30-8 and Register 30-9
- Figures:
  - Updated Figure 2-1, Figure 9-2 and Figure 25-3
  - Added Figure 33-5, Figure 33-6, Figure 33-7 and Figure 33-8
- Tables:
  - Updated Table 2-1, Table 4-1, Table 4-2, Table 4-3, Table 4-10, Table 9-2, Table 9-3, Table 30-1, Table 33-3, Table 33-4, Table 33-5, Table 33-6, Table 33-7, Table 33-8, Table 33-9, Table 33-11, Table 33-12, Table 33-13, Table 33-15, Table 33-19, Table 33-24, Table 33-25 and Table 33-26.
- Examples:
  - Updated Example 15-1.
- Other minor typographic changes and updates throughout the document.

Revision C (November 2015)

This revision incorporates the following updates:

- Tables:
  - Updated Table 33-5 and Table 33-20.
- Figures:
  - Updated Figure 33-8.

Revision D (December 2016)

This revision incorporates the following updates:

- Sections:
  - Added **Section 8.1.1 "Alternate Interrupt Vector Table"**, **Section 8.4.1 "INTCON1-INTCON4"** and **Section 10.2.5 "Exiting from Low-Voltage Retention Sleep"**.
  - Updated the **"Referenced Sources"** section. Updated **Section 4.1.2 "Dual Partition Flash Program Memory Organization"** **Section 4.1.5 "Code-Protect Configuration Bits"**, **Section 8.1.1 "Alternate Interrupt Vector Table"**, **Section 8.4 "Interrupt Control and Status Registers"**, **Section 9.0 "Oscillator Configuration"**, **Section 10.2.4 "Low-Voltage Retention Regulator"**, **Section 11.3 "Interrupt-on-Change (IOC)"**, **Section 11.4.2 "Available Peripherals"**, **Section 17.0 "Serial Peripheral Interface (SPI)"**, **Section 22.0 "Real-Time Clock and Calendar with Timestamp"** and **Section 22.2.2 "Write Lock"**.
- Tables:
  - Added Table 8-1.
  - Updated Table 4, Table 5, Table 6, Table 7, Table 1-3, Table 8-1, Table 9-1, Table 9-2, Table 9-3, Table 11-4, Table 33-4, Table 33-5, Table 33-6 and Table 33-7.
- Figures:
  - Updated Figure 8-1, Figure 9-1, Figure 9-2 and Figure 22-1.
- Examples:
  - Updated Example 11-3, Example 15-1 and Example 22-1.
- Equations:
  - Updated Equation 15-2.
- Registers:
  - Updated Register 7-1, Register 9-8, Register 17-1, Register 27-1 and Register 30-10.

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THE MICROCHIP WEB SITE

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- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
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To register, access the Microchip web site at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://microchip.com/support