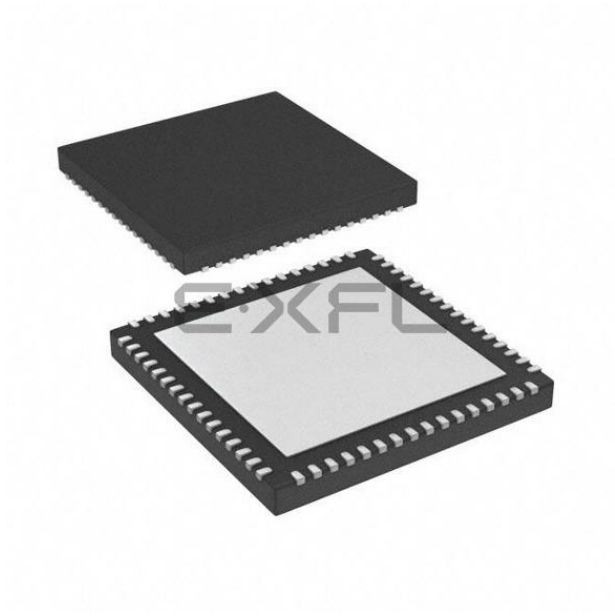

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Details	
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Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256gb606-i-mr

TABLE 2: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJXXXGA606)

Pin	Function	Pin	Function
1	IC4/CTED4/PMD5/RE5	33	**RP16**/RF3
2	SCL3/IC5/PMD6/RE6	34	**RP30**/RF2
3	SDA3/IC6/PMD7/RE7	35	INT0/RF6
4	C1IND/**RP21**/ICM1/OCM1A/PMA5/RG6	36	SDA1/RG3
5	C1INC/**RP26**/OCM1B/PMA4/RG7	37	SCL1/RG2
6	C2IND/**RP19**/ICM2/OCM2A/PMA3/RG8	38	VDD
7	$\overline{\text{MCLR}}$	39	OSCI/CLKI/RC12
8	C1INC/C2INC/C3INC/**RP27**/OCM2B/PMA2/PMALU/RG9	40	OSCO/CLKO/RC15
9	VSS	41	VSS
10	VDD	42	CLC4OUT/**RP2**/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/RD8
11	PGEC3/AN5/C1INA/**RP18**/ICM3/OCM3A/RB5	43	**RP4**/PMACK2/RD9
12	PGED3/AN4/C1INB/**RP28**/OCM3B/RB4	44	**RP3**/PMA15/PMCS2/RD10
13	AN3/C2INA/RB3	45	**RP12**/PMA14/PMCS1/RD11
14	AN2/CTCMP/C2INB/**RP13**/CTED13/RB2	46	CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/RD0
15	PGEC1/ALTCVREF-/ALTVREF-/AN1/**RP1**/CTED12/RB1	47	SOSCI/C3IND/RC13
16	PGED1/ALTCVREF+/ALTVREF+/AN0/**RP0**/PMA6/RB0	48	SOSCO/C3INC/**RPI37**/PWRLCLK/RC14
17	PGEC2/AN6/**RP6**/RB6	49	**RP24**/U5TX/ICM4/RD1
18	PGED2/AN7/**RP7**/U6TX/RB7	50	**RP23**/PMACK1/RD2
19	AVDD	51	**RP22**/ICM7/PMBE0/RD3
20	AVSS	52	**RP25**/PMWR/PMENB/RD4
21	AN8/**RP8**/PWRGT/RB8	53	**RP20**/PMRD/$\overline{\text{PMWR}}$/RD5
22	AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/PMA7/RB9	54	C3INB/U5RX/OC4/RD6
23	TMS/CVREF/AN10/PMA13/RB10	55	C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/RD7
24	TDO/AN11/REFI/PMA12/RB11	56	VCAP
25	VSS	57	N/C
26	VDD	58	$\overline{\text{U5CTS}}$/OC6/RF0
27	TCK/AN12/U6RX/CTED2/PMA11/RB12	59	RF1
28	TDI/AN13/CTED1/PMA10/RB13	60	PMD0/RE0
29	AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/RB14	61	PMD1/RE1
30	AN15/**RP29**/CTED6/PMA0/PMALL/RB15	62	PMD2/RE2
31	**RP10**/SDA2/PMA9/RF4	63	CTED9/PMD3/RE3
32	**RP17**/SCL2/PMA8/RF5	64	HLVDIN/CTED8/PMD4/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.

TABLE 5: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJXXXGB610 TQFP)

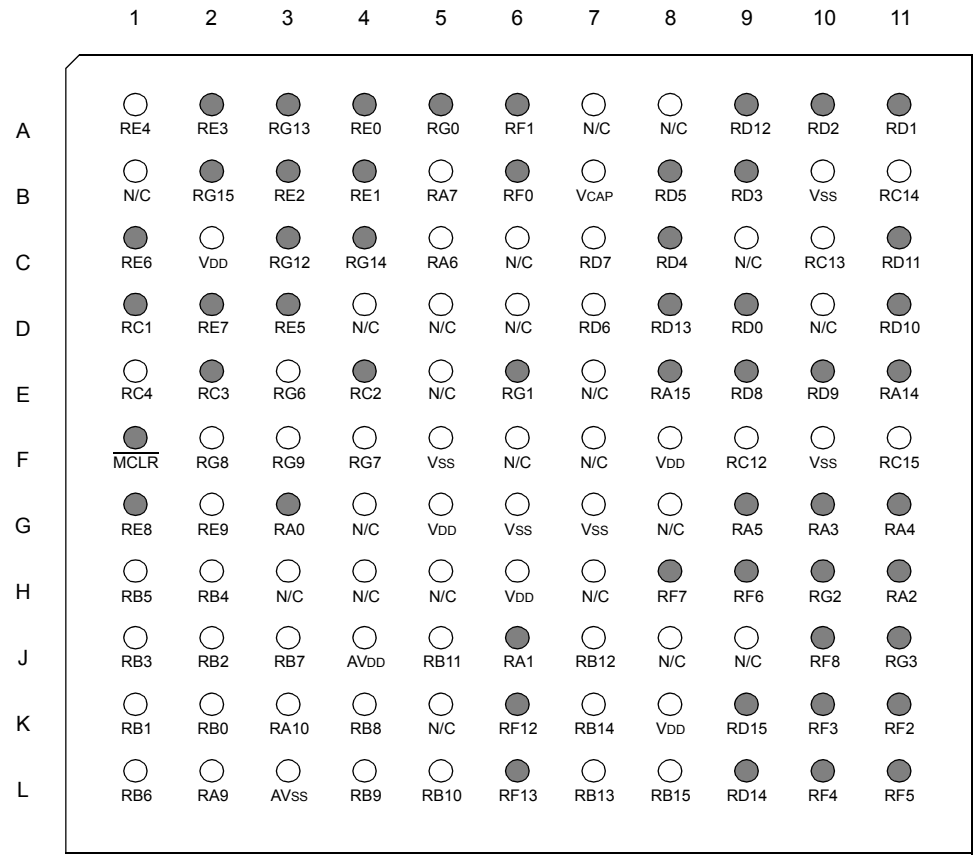
Pin	Function	Pin	Function
1	OCM1C/CTED3/RG15	51	**RP16**/USBID/RF3
2	VDD	52	**RP30**/RF2
3	IC4/CTED4/PMD5/RE5	53	**RP15**/RF8
4	SCL3/IC5/PMD6/RE6	54	VBUS/RF7
5	SDA3/IC6/PMD7/RE7	55	VUSB3V3
6	**RPI38**/OCM1D/RC1	56	D-/RG3
7	**RPI39**/OCM2C/RC2	57	D+/RG2
8	**RPI40**/OCM2D/RC3	58	PMPCS1/SCL2/RA2
9	AN16/**RPI41**/OCM3C/PMCS2/RC4	59	SDA2/PMA20/RA3
10	AN17/C1IND/**RP21**/ICM1/OCM1A/PMA5/RG6	60	TDI/PMA21/RA4
11	AN18/C1INC/**RP26**/OCM1B/PMA4/RG7	61	TDO/RA5
12	AN19/C2IND/**RP19**/ICM2/OCM2A/PMA3/RG8	62	VDD
13	$\overline{\text{MCLR}}$	63	OSCI/CLKI/RC12
14	AN20/C1INC/C2INC/C3INC/**RP27**/OCM2B/PMA2/PMALU/RG9	64	OSCO/CLKO/RC15
15	VSS	65	VSS
16	VDD	66	**RPI36**/SCL1/PMA22/RA14
17	TMS/OCM3D/RA0	67	**RPI35**/SDA1/PMBE1/RA15
18	**RPI33**/PMCS1/RE8	68	CLC4OUT/**RP2**/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/RD8
19	AN21/**RPI34**/PMA19/RE9	69	**RP4**/PMACK2/RD9
20	PGEC3/AN5/C1INA/**RP18**/ICM3/OCM3A/RB5	70	**RP3**/PMA15/PMCS2/RD10
21	PGED3/AN4/C1INB/**RP28**/$\overline{\text{USBOEN}}$/OCM3B/RB4	71	**RP12**/PMA14/PMCS1/RD11
22	AN3/C2INA/RB3	72	CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/INT0/RD0
23	AN2/CTCMP/C2INB/**RP13**/CTED13/RB2	73	SOSCI/C3IND/RC13
24	PGEC1/ALTCVREF-/ALTVREF-/AN1/**RP1**/CTED12/RB1	74	SOSCO/C3INC/**RPI37**/PWRLCLK/RC14
25	PGED1/ALTCVREF+/ALTVREF+/AN0/**RP0**/RB0	75	VSS
26	PGEC2/AN6/**RP6**/RB6	76	**RP24**/U5TX/ICM4/RD1
27	PGED2/AN7/**RP7**/U6TX/RB7	77	**RP23**/PMACK1/RD2
28	CVREF-/VREF-/PMA7/RA9	78	**RP22**/ICM7/PMBE0/RD3
29	CVREF+/VREF+/PMA6/RA10	79	**RPI42**/OCM3E/PMD12/RD12
30	AVDD	80	OCM3F/PMD13/RD13
31	AVSS	81	**RP25**/PMWR/PMENB/RD4
32	AN8/**RP8**/PWRGT/RB8	82	**RP20**/PMRD/$\overline{\text{PMWR}}$/RD5
33	AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/RB9	83	C3INB/U5RX/OC4/PMD14/RD6
34	CVREF/AN10/PMA13/RB10	84	C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/PMD15/RD7
35	AN11/REFI/PMA12/RB11	85	VCAP
36	VSS	86	N/C
37	VDD	87	$\overline{\text{U5CTS}}$/OC6/PMD11/RF0
38	TCK/RA1	88	PMD10/RF1
39	**RP31**/RF13	89	PMD9/RG1
40	**RPI32**/CTED7/PMA18/RF12	90	PMD8/RG0
41	AN12/U6RX/CTED2/PMA11/RB12	91	AN23/OCM1E/RA6
42	AN13/CTED1/PMA10/RB13	92	AN22/OCM1F/PMA17/RA7
43	AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/RB14	93	PMD0/RE0
44	AN15/**RP29**/CTED6/PMA0/PMALL/RB15	94	PMD1/RE1
45	VSS	95	CTED11/PMA16/RG14
46	VDD	96	OCM2E/RG12
47	**RPI43**/RD14	97	OCM2F/CTED10/RG13
48	**RP5**/RD15	98	PMD2/RE2
49	**RP10**/PMA9/RF4	99	CTED9/PMD3/RE3
50	**RP17**/PMA8/RF5	100	HLVDIN/CTED8/PMD4/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.

Pin Diagrams(1) (Continued)

PIC24FJXXXGA610 121-Pin BGA



Legend: See Table 6 for a complete description of pin functions. Pinouts are subject to change.

Note 1: Gray shading indicates 5.5V tolerant input pins.

TABLE 7: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJXXXGB610 BGA) (CONTINUED)

Pin	Full Pin Name	Pin	Full Pin Name
J1	AN3/C2INA/RB3	K7	AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/RB14
J2	AN2/CTCMP/C2INB/**RP13**/CTED13/RB2	K8	VDD
J3	PGED2/AN7/**RP7**/U6TX/RB7	K9	**RP5**/RD15
J4	AVDD	K10	**RP16**/USBID/RF3
J5	AN11/REFI/PMA12/RB11	K11	**RP30**/RF2
J6	TCK/RA1	L1	PGEC2/AN6/**RP6**/RB6
J7	AN12/U6RX/CTED2/PMA11/RB12	L2	CVREF-/VREF-/PMA7/RA9
J8	N/C	L3	AVSS
J9	N/C	L4	AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/RB9
J10	**RP15**/RF8	L5	CVREF/AN10/PMA13/RB10
J11	D-/RG3	L6	**RP31**/RF13
K1	PGEC1/ALTCVREF-/ALTVREF-/AN1/**RP1**/CTED12/RB1	L7	AN13/CTED1/PMA10/RB13
K2	PGED1/ALTCVREF+/ALTVREF+/AN0/**RP0**/RB0	L8	AN15/**RP29**/CTED6/PMA0/PMALL/RB15
K3	CVREF+/VREF+/PMA6/RA10	L9	**RPI43**/RD14
K4	AN8/**RP8**/PWRGT/RB8	L10	**RP10**/PMA9/RF4
K5	N/C	L11	**RP17**/PMA8/RF5
K6	**RPI32**/CTED7/PMA18/RF12		

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.l

TABLE 4-6: SFR MAP: 0200h BLOCK (CONTINUED)

File Name	Address	All Resets	File Name	Address	All Resets
MULTIPLE OUTPUT CAPTURE/COMPARE/PWM (CONTINUED)			**MULTIPLE OUTPUT CAPTURE/COMPARE/PWM (CONTINUED)**		
CCP2RAL	02A8	0000	CCP3PRL	02C8	FFFF
CCP2RAH	02AA	0000	CCP3PRH	02CA	FFFF
CCP2RBL	02AC	0000	CCP3RAL	02CC	0000
CCP2RBH	02AE	0000	CCP3RAH	02CE	0000
CCP2BUFL	02B0	0000	CCP3RBL	02D0	0000
CCP2BUFH	02B2	0000	CCP3RBH	02D2	0000
CCP3CON1L	02B4	0000	CCP3BUFL	02D4	0000
CCP3CON1H	02B6	0000	CCP3BUFH	02D6	0000
CCP3CON2L	02B8	0000	**COMPARATORS**		
CCP3CON2H	02BA	0100	CMSTAT	02E6	0000
CCP3CON3L	02BC	0000	CVRCON	02E8	00xx
CCP3CON3H	02BE	0000	CM1CON	02EA	0000
CCP3STATL	02C0	00x0	CM2CON	02EC	0000
CCP3STATH	02C2	0000	CM3CON	02EE	0000
CCP3TMRL	O2C4	0000	**ANALOG CONFIGURATION**		
CCP3TMRH	02C6	0000	ANCFG	02F4	0000

Legend: — = unimplemented, read as '0'; x = undefined. Reset values are shown in hexadecimal.

TABLE 4-9: SFR MAP: 0500h BLOCK

File Name	Address	All Resets	File Name	Address	All Resets
DMA (CONTINUED)			**USB OTG (CONTINUED)**		
DMAINT5	0500	0000	U1ADDR	056E	00xx
DMASRC5	0502	0000	U1BDTP1	0570	0000
DMADST5	0504	0000	U1FRML	0572	0000
DMACNT5	0506	0001	U1FRMH	0574	0000
DMACH6	0508	0000	U1TOK	0576	0000
DMAINT6	050A	0000	U1SOF	0578	0000
DMASRC6	050C	0000	U1BDTP2	057A	0000
DMADST6	050E	0000	U1BDTP3	057C	0000
DMACNT6	0510	0001	U1CNFG1	057E	0000
DMACH7	0512	0000	U1CNFG2	0580	0000
DMAINT7	0514	0000	U1EP0	0582	0000
DMASRC7	0516	0000	U1EP1	0584	0000
DMADST7	0518	0000	U1EP2	0586	0000
DMACNT7	051A	0001	U1EP3	0588	0000
USB OTG			U1EP4	058A	0000
U1OTGIR	0558	0000	U1EP5	058C	0000
U1OTGIE	055A	0000	U1EP6	058E	0000
U1OTGSTAT	055C	0000	U1EP7	0590	0000
U1OTGCON	055E	0000	U1EP8	0592	0000
U1PWRC	0560	00x0	U1EP9	0594	0000
U1IR	0562	0000	U1EP10	0596	0000
U1IE	0564	0000	U1EP11	0598	0000
U1EIR	0566	0000	U1EP12	059A	0000
U1EIE	0568	0000	U1EP13	059C	0000
U1STAT	056A	0000	U1EP14	059E	0000
U1CON	056C	00x0	U1EP15	05A0	0000

Legend: — = unimplemented, read as '0'; x = undefined. Reset values are shown in hexadecimal.

REGISTER 7-1: RCON: RESET CONTROL REGISTER

R/W-0	R/W-0	R/W-1	R/W-0	U-0	U-0	R/W-0	R/W-0
TRAPR(1)	IOPUWR(1)	SBOREN	RETEN(2)	—	—	CM(1)	VREGS(3)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR(1)	SWR(1)	SWDTEN(4)	WDTO(1)	SLEEP(1)	IDLE(1)	BOR(1)	POR(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TRAPR:** Trap Reset Flag bit(1)
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit(1)
1 = An illegal opcode detection, an illegal address mode or Uninitialized W register is used as an Address Pointer and caused a Reset
0 = An illegal opcode or Uninitialized W register Reset has not occurred

bit 13 **SBOREN:** Software Enable/Disable of BOR bit
1 = BOR is turned on in software
0 = BOR is turned off in software

bit 12 **RETEN:** Retention Mode Enable bit(2)
1 = Retention mode is enabled while device is in Sleep modes (1.2V regulator enabled)
0 = Retention mode is disabled

bit 11-10 **Unimplemented:** Read as '0'

bit 9 **CM:** Configuration Word Mismatch Reset Flag bit(1)
1 = A Configuration Word Mismatch Reset has occurred
0 = A Configuration Word Mismatch Reset has not occurred

bit 8 **VREGS:** Fast Wake-up from Sleep bit(3)
1 = Fast wake-up is enabled (uses more power)
0 = Fast wake-up is disabled (uses less power)

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin bit(1)
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset (Instruction) Flag bit(1)
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed

Note 1: All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the $\overline{LPCFG}$ Configuration bit is '1' (unprogrammed), the retention regulator is disabled and the RETEN bit has no effect. Retention mode preserves the SRAM contents during Sleep.

3: Re-enabling the regulator after it enters Standby mode will add a delay, TVREG, when waking up from Sleep. Applications that do not use the voltage regulator should set this bit to prevent this delay from occurring.

4: If the FWDTEN<1:0> Configuration bits are '11' (unprogrammed), the WDT is always enabled**,** regardless of the SWDTEN bit setting.

9.6.1 CONSIDERATIONS FOR USB OPERATION

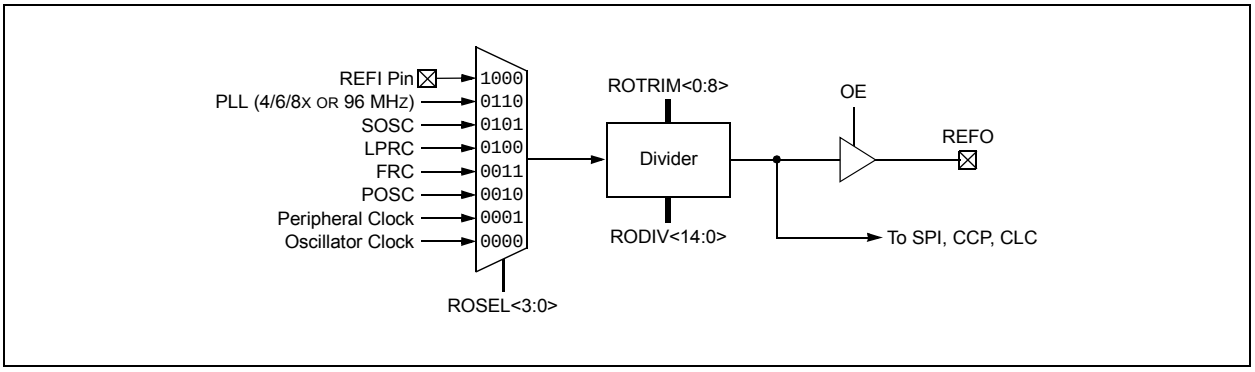
When using the USB On-The-Go module in PIC24FJ1024GA610/GB610 devices, users must always observe these rules in configuring the system clock:

- The system clock frequency must be 16 MHz or 32 MHz. System clock frequencies below 16 MHz are not allowed for USB module operation.
- The Oscillator modes listed in Table 9-3 are the only oscillator configurations that permit USB operation. There is no provision to provide a separate external clock source to the USB module.
- For USB operation, the selected clock source (EC, HS or XT) must meet the USB clock tolerance requirements.
- When the FRCPLL Oscillator mode is used for USB applications, the FRC self-tune system should be used as well. While the FRC is accurate, the only two ways to ensure the level of accuracy, required by the *"USB 2.0 Specification"* throughout the application's operating range, are either the self-tune system or manually changing the TUN<5:0> bits.
- The user must always ensure that the FRC source is configured to provide a frequency of 4 MHz or 8 MHz (RCDIV<2:0> = 001 or 000) and that the USB PLL prescaler is configured appropriately.
- All other Oscillator modes are available; however, USB operation is not possible when these modes are selected. They may still be useful in cases where other power levels of operation are desirable and the USB module is not needed (e.g., the application is Sleeping and waiting for a bus attachment).

9.7 Reference Clock Output

In addition to the CLKO output (FOSC/2), the PIC24FJ1024GA610/GB610 family devices can be configured to provide a reference clock output signal to a port pin. This feature is available in all oscillator configurations and allows the user to select a greater range of clock submultiples to drive external devices in the application. CLKO is enabled by Configuration bit, OSCIOFCN, and is independent of the REFO reference clock. REFO is mappable to any I/O pin that has mapped output capability. Refer to Table 11-4 for more information. The REFO module block diagram is shown on Figure 9-3.

FIGURE 9-3: REFERENCE CLOCK GENERATOR



11.4.5 CONSIDERATIONS FOR PERIPHERAL PIN SELECTION

The ability to control Peripheral Pin Selection introduces several considerations into application design that could be overlooked. This is particularly true for several common peripherals that are available only as remappable peripherals.

The main consideration is that the Peripheral Pin Selects are not available on default pins in the device's default (Reset) state. Since all RPINRx registers reset to '111111' and all RPORx registers reset to '000000', all Peripheral Pin Select inputs are tied to Vss, and all Peripheral Pin Select outputs are disconnected.

This situation requires the user to initialize the device with the proper peripheral configuration before any other application code is executed. Since the IOLOCK bit resets in the unlocked state, it is not necessary to execute the unlock sequence after the device has come out of Reset. For application safety, however, it is best to set IOLOCK and lock the configuration after writing to the control registers.

Because the unlock sequence is timing-critical, it must be executed as an assembly language routine in the same manner as changes to the oscillator configuration. If the bulk of the application is written in 'C', or another high-level language, the unlock sequence should be performed by writing in-line assembly.

Choosing the configuration requires the review of all Peripheral Pin Selects and their pin assignments, especially those that will not be used in the application. In all cases, unused pin-selectable peripherals should be disabled completely. Unused peripherals should have their inputs assigned to an unused RPn/RPIn pin function. I/O pins with unused RPn functions should be configured with the null peripheral output.

The assignment of a peripheral to a particular pin does not automatically perform any other configuration of the pin's I/O circuitry. In theory, this means adding a pin-selectable output to a pin may mean inadvertently driving an existing peripheral input when the output is driven. Users must be familiar with the behavior of other fixed peripherals that share a remappable pin and know when to enable or disable them. To be safe, fixed digital peripherals that share the same pin should be disabled when not in use.

Along these lines, configuring a remappable pin for a specific peripheral does not automatically turn that feature on. The peripheral must be specifically configured for operation and enabled as if it were tied to a fixed pin. Where this happens in the application code (immediately following a device Reset and peripheral configuration or inside the main application routine) depends on the peripheral and its use in the application.

A final consideration is that Peripheral Pin Select functions neither override analog inputs nor reconfigure pins with analog functions for digital I/O. If a pin is configured as an analog input on a device Reset, it must be explicitly reconfigured as a digital I/O when used with a Peripheral Pin Select.

Example 11-4 shows a configuration for bidirectional communication with flow control using UART1. The following input and output functions are used:

- Input Functions: U1RX, $\overline{\text{U1CTS}}$
- Output Functions: U1TX, $\overline{\text{U1RTS}}$

EXAMPLE 11-4: CONFIGURING UART1 INPUT AND OUTPUT FUNCTIONS

```
//  Unlock Registers
asm volatile    ("MOV   #OSCCON, w1   \n"
                 "MOV    #0x46, w2    \n"
                 "MOV    #0x57, w3    \n"
                 "MOV.b  w2, [w1]     \n"
                 "MOV.b  w3, [w1]     \n"
                 "BCLR   OSCCON, #6")  ;

//  or use XC16 built-in macro:
//  __builtin_write_OSCCONL(OSCCON & 0xbf);

//  Configure Input Functions (Table 11-3)
    // Assign U1RX To Pin RP0
    RPINR18bits.U1RXR = 0;

    // Assign U1CTS To Pin RP1
    RPINR18bits.U1CTSR = 1;

//  Configure Output Functions (Table 11-4)
    // Assign U1TX To Pin RP2
    RPOR1bits.RP2R = 3;

    // Assign U1RTS To Pin RP3
    RPOR1bits.RP3R = 4;

//  Lock Registers
asm volatile   ("MOV   #OSCCON, w1   \n"
                "MOV    #0x46, w2    \n"
                "MOV    #0x57, w3    \n"
                "MOV.b  w2, [w1]     \n"
                "MOV.b  w3, [w1]     \n"
                "BSET   OSCCON, #6")  ;

//  or use XC16 built-in macro:
//  __builtin_write_OSCCONL(OSCCON | 0x40);
```

REGISTER 11-42: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP13R5	RP13R4	RP13R3	RP13R2	RP13R1	RP13R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP12R5	RP12R4	RP12R3	RP12R2	RP12R1	RP12R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP13R<5:0>:** RP13 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP13 (see Table 11-4 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP12R<5:0>:** RP12 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP12 (see Table 11-4 for peripheral function numbers).

REGISTER 11-43: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP15R5(1)	RP15R4(1)	RP15R3(1)	RP15R2(1)	RP15R1(1)	RP15R0(1)
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP14R5	RP14R4	RP14R3	RP14R2	RP14R1	RP14R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP15R<5:0>:** RP15 Output Pin Mapping bits(1)
Peripheral Output Number n is assigned to pin, RP15 (see Table 11-4 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP14R<5:0>:** RP14 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP14 (see Table 11-4 for peripheral function numbers).

Note 1: This pin is not available on 64-pin devices.

REGISTER 18-3: I2CxSTAT: I2Cx STATUS REGISTER

R-0, HSC	R-0, HSC	R-0, HSC	U-0	U-0	R/C-0, HSC	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10
bit 15							bit 8

R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D/$\overline{A}$	P	S	R/$\overline{W}$	RBF	TBF
bit 7							bit 0

Legend:	C = Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
HSC = Hardware Settable/Clearable bit			

bit 15 **ACKSTAT:** Acknowledge Status bit (updated in all Master and Slave modes)
1 = Acknowledge was not received from slave
0 = Acknowledge was received from slave

bit 14 **TRSTAT:** Transmit Status bit (when operating as I^2C master; applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress

bit 13 **ACKTIM:** Acknowledge Time Status bit (valid in I^2C Slave mode only)
1 = Indicates I^2C bus is in an Acknowledge sequence, set on 8th falling edge of SCLx clock
0 = Not an Acknowledge sequence, cleared on 9th rising edge of SCLx clock

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Bus Collision Detect bit (Master/Slave mode; cleared when I^2C module is disabled, I2CEN = 0)
1 = A bus collision has been detected during a master or slave transmit operation
0 = No bus collision has been detected

bit 9 **GCSTAT:** General Call Status bit (cleared after Stop detection)
1 = General call address was received
0 = General call address was not received

bit 8 **ADD10:** 10-Bit Address Status bit (cleared after Stop detection)
1 = 10-bit address was matched
0 = 10-bit address was not matched

bit 7 **IWCOL:** I2Cx Write Collision Detect bit
1 = An attempt to write to the I2CxTRN register failed because the I^2C module is busy; must be cleared in software
0 = No collision

bit 6 **I2COV:** I2Cx Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte; I2COV is a "don't care" in Transmit mode, must be cleared in software
0 = No overflow

bit 5 **D/$\overline{A}$:** Data/$\overline{\text{Address}}$ bit (when operating as I^2C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received or transmitted was an address

bit 4 **P:** I2Cx Stop bit
Updated when Start, Reset or Stop is detected; cleared when the I^2C module is disabled, I2CEN = 0.
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last

20.1 Hardware Configuration

20.1.1 DEVICE MODE

20.1.1.1 D+ Pull-up Resistor

PIC24FJ1024GB610 family devices have a built-in 1.5 kΩ resistor on the D+ line that is available when the microcontroller is operating in Device mode. This is used to signal an external host that the device is operating in Full-Speed Device mode. It is engaged by setting the USBEN bit (U1CON<0>) and powering up the USB module (USBPWR = 1). If the OTGEN bit (U1OTGCON<2>) is set, then the D+ pull-up is enabled through the DPPULUP bit (U1OTGCON<7>).

20.1.1.2 The VBUS Pin

In order to meet the *"USB 2.0 Specification"* requirement, relating to the back drive voltage on the D+/D- pins, the USB module incorporates VBUS-level sensing comparators. When the comparators detect the VBUS level below the VA_SESS_VLD level, the hardware will automatically disable the D+ pull-up resistor described in **Section 20.1.1.1 "D+ Pull-up Resistor"**. This allows the device to automatically meet the back drive requirement for D+ and D-, even if the application firmware does not explicitly monitor the VBUS level. Therefore, the VBUS microcontroller pin should not be left floating in USB Device mode application designs, and should normally be connected to the VBUS pin on the USB connector/cable (either directly or through a small resistance ≤ 100 ohms).

20.1.1.3 Power Modes

Many USB applications will likely have several different sets of power requirements and configuration. The most common power modes encountered are:

- Bus Power Only mode
- Self-Power Only mode
- Dual Power with Self-Power Dominance

Bus Power Only mode (Figure 20-2) is effectively the simplest method. All power for the application is drawn from the USB.

To meet the inrush current requirements of the *"USB 2.0 Specification",* the total effective capacitance, appearing across VBUS and ground, must be no more than 10 μF.

In the USB Suspend mode, devices must consume no more than 2.5 mA from the 5V VBUS line of the USB cable. During the USB Suspend mode, the D+ or D- pull-up resistor must remain active, which will consume some of the allowed suspend current.

In Self-Power Only mode (Figure 20-3), the USB application provides its own power, with very little power being pulled from the USB. Note that an attach indication is added to indicate when the USB has been connected and the host is actively powering VBUS.

To meet compliance specifications, the USB module (and the D+ or D- pull-up resistor) should not be enabled until the host actively drives VBUS high. One of the 5.5V tolerant I/O pins may be used for this purpose.

The application should never source any current onto the 5V VBUS pin of the USB cable when the USB module is operated in USB Device mode.

The Dual Power mode with Self-Power Dominance (Figure 20-4) allows the application to use internal power primarily, but switch to power from the USB when no internal power is available. Dual power devices must also meet all of the special requirements for inrush current and Suspend mode current previously described, and must not enable the USB module until VBUS is driven high.

FIGURE 20-2: BUS-POWERED INTERFACE EXAMPLE

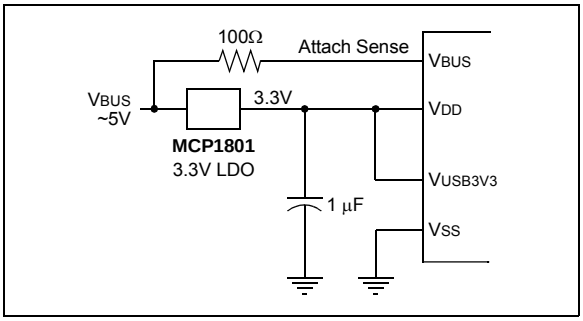


FIGURE 20-3: SELF-POWER ONLY

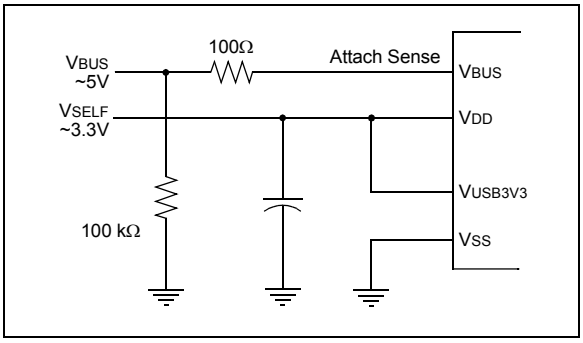
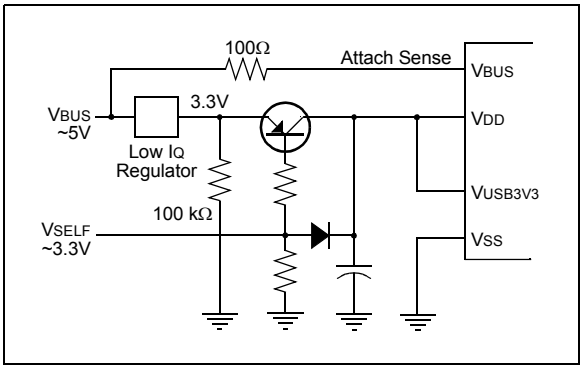


FIGURE 20-4: DUAL POWER EXAMPLE



REGISTER 20-8: U1CON: USB CONTROL REGISTER (HOST MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-x, HSC	R-x, HSC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
JSTATE	SE0	TOKBUSY	USBRST	HOSTEN	RESUME	PPBRST	SOFEN
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **JSTATE:** Live Differential Receiver J-State Flag bit
- 1 = J-state (differential '0' in low speed, differential '1' in full speed) is detected on the USB
- 0 = No J-state is detected

bit 6 **SE0:** Live Single-Ended Zero Flag bit
- 1 = Single-ended zero is active on the USB bus
- 0 = No single-ended zero is detected

bit 5 **TOKBUSY:** Token Busy Status bit
- 1 = Token is being executed by the USB module in On-The-Go state
- 0 = No token is being executed

bit 4 **USBRST:** USB Module Reset bit
- 1 = USB Reset has been generated for a software Reset; application must set this bit for 50 ms, then clear it
- 0 = USB Reset is terminated

bit 3 **HOSTEN:** Host Mode Enable bit
- 1 = USB host capability is enabled; pull-downs on D+ and D- are activated in hardware
- 0 = USB host capability is disabled

bit 2 **RESUME:** Resume Signaling Enable bit
- 1 = Resume signaling is activated; software must set bit for 10 ms and then clear to enable remote wake-up
- 0 = Resume signaling is disabled

bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
- 1 = Resets all Ping-Pong Buffer Pointers to the even BD banks
- 0 = Ping-Pong Buffer Pointers are not reset

bit 0 **SOFEN:** Start-of-Frame Enable bit
- 1 = Start-of-Frame token is sent every one 1 ms
- 0 = Start-of-Frame token is disabled

REGISTER 20-11: U1SOF: USB OTG START-OF-TOKEN THRESHOLD REGISTER (HOST MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **CNT<7:0>:** Start-of-Frame Size bits
Value represents 10 + (packet size of n bytes). For example:
0100 1010 = 64-byte packet
0010 1010 = 32-byte packet
0001 0010 = 8-byte packet

TABLE 21-2: ENHANCED PARALLEL MASTER PORT PIN DESCRIPTIONS

Pin Name (Alternate Function)	Type	Description
PMA<22:16>	O	Address Bus bits<22:16>
PMA15	O	Address Bus bit 15
	I/O	Data Bus bit 15 (16-bit port with Multiplexed Addressing)
(PMCS2)	O	Chip Select 2 (alternate location)
PMA14	O	Address Bus bit 14
	I/O	Data Bus bit 14 (16-bit port with Multiplexed Addressing)
(PMCS1)	O	Chip Select 1 (alternate location)
PMA<13:8>	O	Address Bus bits<13:8>
	I/O	Data Bus bits<13:8> (16-bit port with Multiplexed Addressing)
PMA<7:3>	O	Address Bus bits<7:3>
PMA2 (PMALU)	O	Address Bus bit 2
	O	Address Latch Upper Strobe for Multiplexed Address
PMA1 (PMALH)	I/O	Address Bus bit 1
	O	Address Latch High Strobe for Multiplexed Address
PMA0 (PMALL)	I/O	Address Bus bit 0
	O	Address Latch Low Strobe for Multiplexed Address
PMD<15:8>	I/O	Data Bus bits<15:8> (Demultiplexed Addressing)
PMD<7:4>	I/O	Data Bus bits<7:4>
	O	Address Bus bits<7:4> (4-bit port with 1-Phase Multiplexed Addressing)
PMD<3:0>	I/O	Data Bus bits<3:0>
PMCS1(1)	O	Chip Select 1
PMCS2(1)	O	Chip Select 2
PMWR	I/O	Write Strobe(2)
(PMENB)	I/O	Enable Signal(2)
PMRD	I/O	Read Strobe(2)
(PMRD/$\overline{\text{PMWR}}$)	I/O	Read/$\overline{\text{Write}}$ Signal(2)
PMBE1	O	Byte Indicator
PMBE0	O	Nibble or Byte Indicator
PMACK1	I	Acknowledgment Signal 1
PMACK2	I	Acknowledgment Signal 2

Note 1: These pins are implemented in 100-pin and 121-pin devices only.

2: Signal function depends on the setting of the MODE<1:0> and SM bits (PMCON1<9:8> and PMCSxCF<8>).

REGISTER 22-6: RTCSTATL: RTCC STATUS REGISTER (LOW)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/C-0	U-0	R/C-0	R-0	R-0	R-0
—	—	ALMEVT	—	TSAEVT(1)	SYNC	ALMSYNC	HALFSEC(2)
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5 **ALMEVT:** Alarm Event bit
1 = An alarm event has occurred
0 = An alarm event has not occurred

bit 4 **Unimplemented:** Read as '0'

bit 3 **TSAEVT**: Timestamp A Event bit(1)
1 = A timestamp event has occurred
0 = A timestamp event has not occurred

bit 2 **SYNC:** Synchronization Status bit
1 = Time registers may change during software read
0 = Time registers may be read safely

bit 1 **ALMSYNC:** Alarm Synchronization Status bit
1 = Alarm registers (ALMTIME and ALMDATE) and Alarm Mask bits (AMASK<3:0>) should not be modified, and Alarm Control bits (ALRMEN, ALMRPT<7:0>) may change during software read
0 = Alarm registers and Alarm Control bits may be written/modified safely

bit 0 **HALFSEC:** Half Second Status bit(2)
1 = Second half period of a second
0 = First half period of a second

Note 1: User software may write a '1' to this location to initiate a Timestamp A event; timestamp capture is not valid until TSAEVT reads as '1'.

2: This bit is read-only; it is cleared to '0' on a write to the SECONE<3:0> bits.

TABLE 33-20: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
F20	FRC Accuracy @ 8 MHz	-1.5	+0.15	1.5	%	2.0V ≤ VDD ≤ 3.6V, 0°C ≤ TA ≤ +85°C **(Note 1)**
		-2.0	—	2.0	%	2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ 0°C
		-0.20	+0.05	-0.20	%	2.0V ≤ VDD ≤ 3.6V, 0°C ≤ TA ≤ +85°C, self-tune is enabled and locked **(Note 2)**
F21	LPRC @ 31 kHz	-20	—	20	%	VCAP Output Voltage = 1.8V
F22	OSCTUN Step-Size	—	0.05	—	%/bit	
F23	FRC Self-Tune Lock Time	—	5	8	ms	**(Note 3)**

Note 1: To achieve this accuracy, physical stress applied to the microcontroller package (ex., by flexing the PCB) must be kept to a minimum.

2: Accuracy is measured with respect to the reference source.

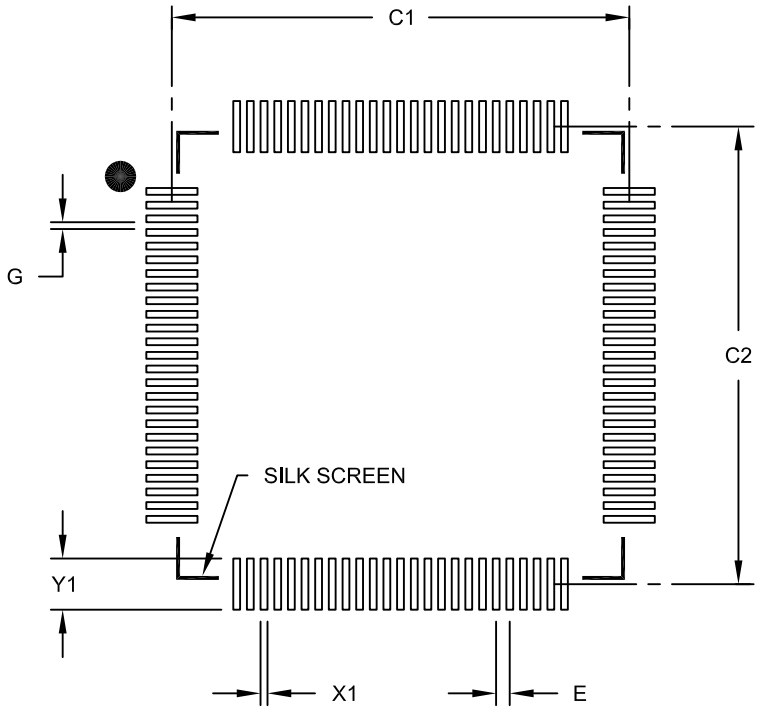
3: Time from reference clock stable, and in range, to FRC tuned within range specified by F20 (with self-tune).

TABLE 33-21: RC OSCILLATOR START-UP TIME

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
FR0	TFRC	FRC Oscillator Start-up Time	—	15	—	μs	
FR1	TLPRC	Low-Power RC Oscillator Start-up Time	—	50	—	μs	

100-Lead Plastic Thin Quad Flatpack (PT)- 12x12x1mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Contact Pad Spacing	C1		13.40	
Contact Pad Spacing	C2		13.40	
Contact Pad Width (X100)	X1			0.20
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2100B

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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