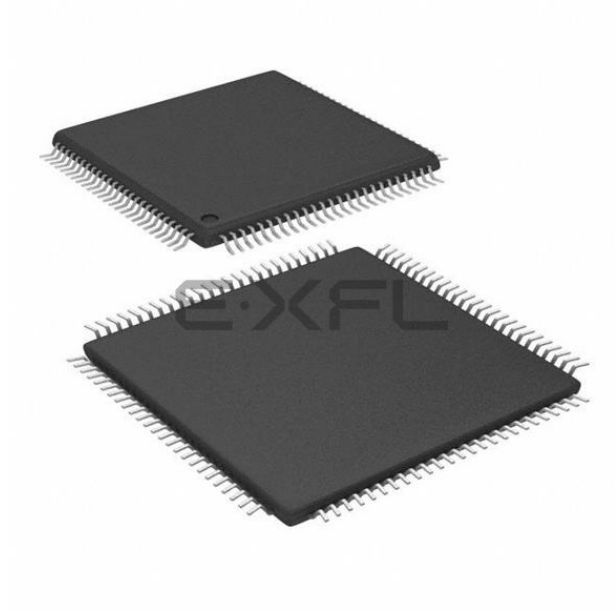
Microchip Technology - PIC24FJ256GB610-I/PT Datasheet



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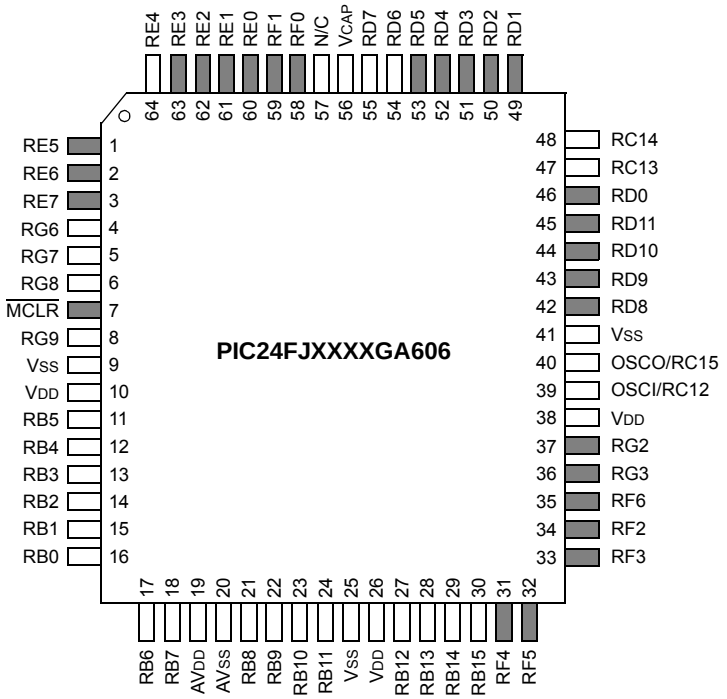
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256gb610-i-pt

Pin Diagrams(2)

64-Pin TQFP
64-Pin QFN(1)



Legend: See Table 2 for a complete description of pin functions. Pinouts are subject to change.
Note 1: It is recommended to connect the metal pad on the bottom of the 64-pin QFN package to VSS.
2: Gray shading indicates 5.5V tolerant input pins.

TABLE 5: COMPLETE PIN FUNCTION DESCRIPTIONS (PIC24FJXXXGB610 TQFP)

Pin	Function	Pin	Function
1	OCM1C/CTED3/RG15	51	**RP16**/USBID/RF3
2	VDD	52	**RP30**/RF2
3	IC4/CTED4/PMD5/RE5	53	**RP15**/RF8
4	SCL3/IC5/PMD6/RE6	54	VBUS/RF7
5	SDA3/IC6/PMD7/RE7	55	VUSB3V3
6	**RPI38**/OCM1D/RC1	56	D-/RG3
7	**RPI39**/OCM2C/RC2	57	D+/RG2
8	**RPI40**/OCM2D/RC3	58	PMPCS1/SCL2/RA2
9	AN16/**RPI41**/OCM3C/PMCS2/RC4	59	SDA2/PMA20/RA3
10	AN17/C1IND/**RP21**/ICM1/OCM1A/PMA5/RG6	60	TDI/PMA21/RA4
11	AN18/C1INC/**RP26**/OCM1B/PMA4/RG7	61	TDO/RA5
12	AN19/C2IND/**RP19**/ICM2/OCM2A/PMA3/RG8	62	VDD
13	$\overline{\text{MCLR}}$	63	OSCI/CLKI/RC12
14	AN20/C1INC/C2INC/C3INC/**RP27**/OCM2B/PMA2/PMALU/RG9	64	OSCO/CLKO/RC15
15	VSS	65	VSS
16	VDD	66	**RPI36**/SCL1/PMA22/RA14
17	TMS/OCM3D/RA0	67	**RPI35**/SDA1/PMBE1/RA15
18	**RPI33**/PMCS1/RE8	68	CLC4OUT/**RP2**/$\overline{\text{U6RTS}}$/U6BCLK/ICM5/RD8
19	AN21/**RPI34**/PMA19/RE9	69	**RP4**/PMACK2/RD9
20	PGEC3/AN5/C1INA/**RP18**/ICM3/OCM3A/RB5	70	**RP3**/PMA15/PMCS2/RD10
21	PGED3/AN4/C1INB/**RP28**/$\overline{\text{USBOEN}}$/OCM3B/RB4	71	**RP12**/PMA14/PMCS1/RD11
22	AN3/C2INA/RB3	72	CLC3OUT/**RP11**/$\overline{\text{U6CTS}}$/ICM6/INT0/RD0
23	AN2/CTCMP/C2INB/**RP13**/CTED13/RB2	73	SOSCI/C3IND/RC13
24	PGEC1/ALTCVREF-/ALTVREF-/AN1/**RP1**/CTED12/RB1	74	SOSCO/C3INC/**RPI37**/PWRLCLK/RC14
25	PGED1/ALTCVREF+/ALTVREF+/AN0/**RP0**/RB0	75	VSS
26	PGEC2/AN6/**RP6**/RB6	76	**RP24**/U5TX/ICM4/RD1
27	PGED2/AN7/**RP7**/U6TX/RB7	77	**RP23**/PMACK1/RD2
28	CVREF-/VREF-/PMA7/RA9	78	**RP22**/ICM7/PMBE0/RD3
29	CVREF+/VREF+/PMA6/RA10	79	**RPI42**/OCM3E/PMD12/RD12
30	AVDD	80	OCM3F/PMD13/RD13
31	AVSS	81	**RP25**/PMWR/PMENB/RD4
32	AN8/**RP8**/PWRGT/RB8	82	**RP20**/PMRD/$\overline{\text{PMWR}}$/RD5
33	AN9/$\overline{\text{TMPR}}$/**RP9**/T1CK/RB9	83	C3INB/U5RX/OC4/PMD14/RD6
34	CVREF/AN10/PMA13/RB10	84	C3INA/$\overline{\text{U5RTS}}$/U5BCLK/OC5/PMD15/RD7
35	AN11/REFI/PMA12/RB11	85	VCAP
36	VSS	86	N/C
37	VDD	87	$\overline{\text{U5CTS}}$/OC6/PMD11/RF0
38	TCK/RA1	88	PMD10/RF1
39	**RP31**/RF13	89	PMD9/RG1
40	**RPI32**/CTED7/PMA18/RF12	90	PMD8/RG0
41	AN12/U6RX/CTED2/PMA11/RB12	91	AN23/OCM1E/RA6
42	AN13/CTED1/PMA10/RB13	92	AN22/OCM1F/PMA17/RA7
43	AN14/**RP14**/CTED5/CTPLS/PMA1/PMALH/RB14	93	PMD0/RE0
44	AN15/**RP29**/CTED6/PMA0/PMALL/RB15	94	PMD1/RE1
45	VSS	95	CTED11/PMA16/RG14
46	VDD	96	OCM2E/RG12
47	**RPI43**/RD14	97	OCM2F/CTED10/RG13
48	**RP5**/RD15	98	PMD2/RE2
49	**RP10**/PMA9/RF4	99	CTED9/PMD3/RE3
50	**RP17**/PMA8/RF5	100	HLVDIN/CTED8/PMD4/RE4

Legend: **RPn** and **RPIn** represent remappable pins for Peripheral Pin Select (PPS) functions.

Note: Pinouts are subject to change.

TABLE 1-3: PIC24FJ1024GA610/GB610 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locator						I/O	Input Buffer	Description
	GA606 64-Pin QFN/TQFP/ QFP	GB606 64-Pin QFN/ TQFP/QFP	GA610 100-Pin TQFP/ QFP	GB610 100-Pin TQFP/ QFP	GA612 121-Pin BGA	GB612 121-Pin BGA			
PMD0	60	60	93	93	A4	A4	I/O	DIG/ ST/TTL	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMD1	61	61	94	94	B4	B4	I/O	DIG/ ST/TTL	
PMD2	62	62	98	98	B3	B3	I/O	DIG/ ST/TTL	
PMD3	63	63	99	99	A2	A2	I/O	DIG/ ST/TTL	
PMD4	64	64	100	100	A1	A1	I/O	DIG/ ST/TTL	
PMD5	1	1	3	3	D3	D3	I/O	DIG/ ST/TTL	
PMD6	2	2	4	4	C1	C1	I/O	DIG/ ST/TTL	
PMD7	3	3	5	5	D2	D2	I/O	DIG/ ST/TTL	
PMD8	—	—	90	90	A5	A5	I/O	DIG/ ST/TTL	
PMD9	—	—	89	89	E6	E6	I/O	DIG/ ST/TTL	
PMD10	—	—	88	88	A6	A6	I/O	DIG/ ST/TTL	
PMD11	—	—	87	87	B6	B6	I/O	DIG/ ST/TTL	
PMD12	—	—	79	79	A9	A9	I/O	DIG/ ST/TTL	
PMD13	—	—	80	80	D8	D8	I/O	DIG/ ST/TTL	
PMD14	—	—	83	83	D7	D7	I/O	DIG/ ST/TTL	
PMD15	—	—	84	84	C7	C7	I/O	DIG/ ST/TTL	
$\overline{\text{PMRD}}$/ $\overline{\text{PMWR}}$	53	53	82	82	B8	B8	I/O	DIG/ ST/TTL	Parallel Master Port Read Strobe/Write Strobe
PMWR/ PMENB	52	52	81	81	C8	C8	I/O	DIG/ ST/TTL	Parallel Master Port Write Strobe/Enable Strobe
PWRGT	21	21	32	32	K4	K4	O	DIG	Real-Time Clock Power Control Output
PWRLCLK	48	48	74	74	B11	B11	I	ST	Real-Time Clock 50/60 Hz Clock Input

Legend: TTL = TTL input buffer
ANA = Analog level input/output
DIG = Digital input/output
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated Transceiver

REGISTER 3-2: CORCON: CPU CORE CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/C-0	R/W-1	U-0	U-0
—	—	—	—	IPL3(1)	PSV(2)	—	—
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit(1)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

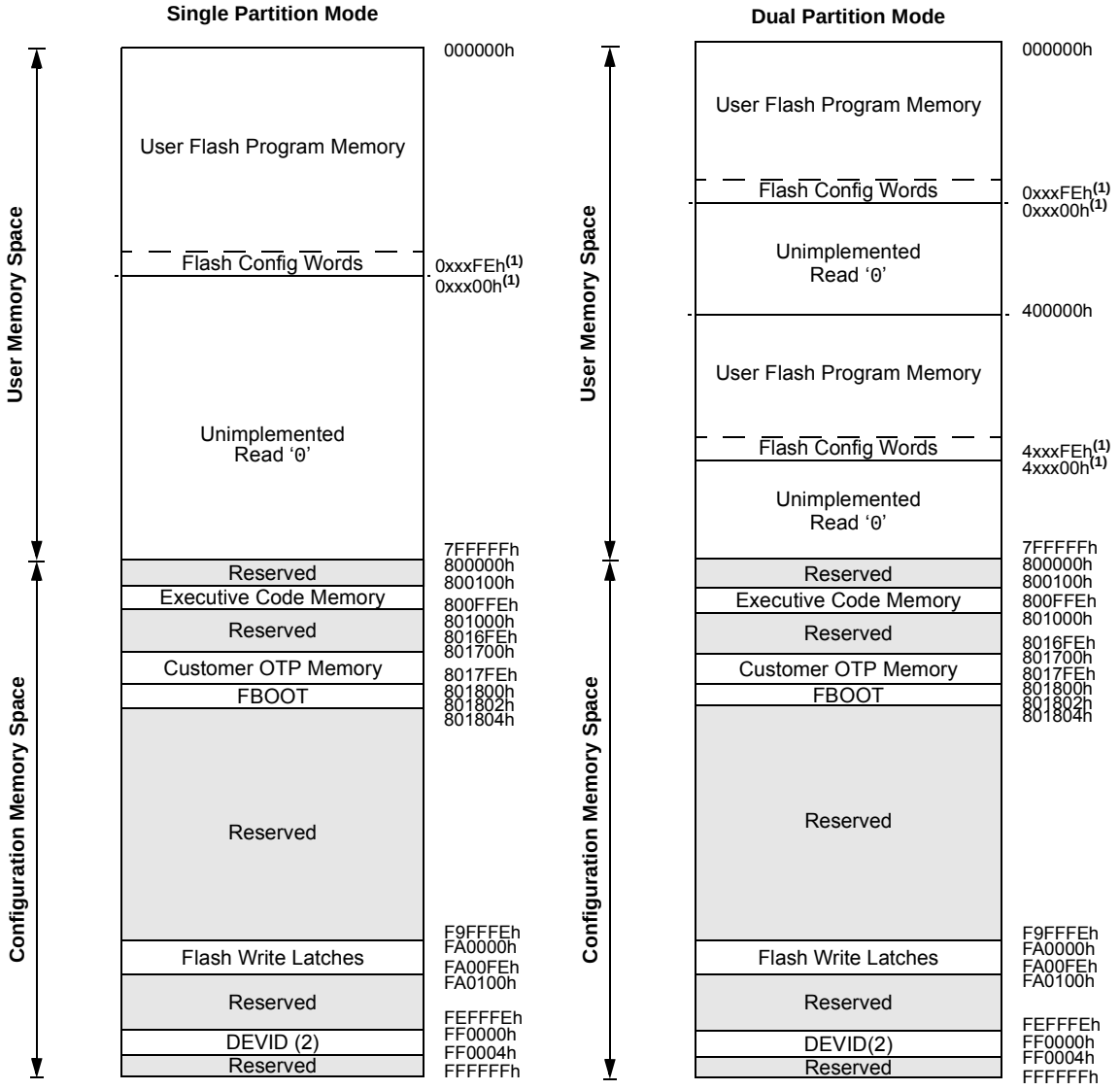
bit 2 **PSV:** Program Space Visibility (PSV) in Data Space Enable
1 = Program space is visible in Data Space
0 = Program space is not visible in Data Space

bit 1-0 **Unimplemented:** Read as '0'

Note 1: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level; see Register 3-1 for bit description.

2: If PSV = 0, any reads from data memory at 0x8000 and above will cause an address trap error instead of reading from the PSV section of program memory. This bit is not individually addressable.

FIGURE 4-1: PROGRAM SPACE MEMORY MAP FOR PIC24FJ1024GA610/GB610 FAMILY DEVICES



Legend: Memory areas are not shown to scale.

Note 1: Exact boundary addresses are determined by the size of the implemented program memory (Table 4-1).

TABLE 4-1: PROGRAM MEMORY SIZES AND BOUNDARIES(1)

Device	Program Memory Upper Boundary (Instruction Words)			Write Blocks(2)	Erase Blocks(2)
	Single Partition Mode	Dual Partition Mode			
		Active Partition	Inactive Partition		
PIC24FJ1024GX6XX	0ABFFEh (352K)	055FFEh (176K)	455FFEh (176K)	2752	344
PIC24FJ512GX6XX	055FFEh (176K)	02AFFEh (88k)	42AFFEh (88k)	1376	172
PIC24FJ256GX6XX	02AFFEh (88K)	0157FEh (44k)	4157FEh (44k)	688	86
PIC24FJ128GX6XX	015FFEh (44K)	00AFFEh (22k)	40AFFEh (22k)	352	44

Note 1: Includes Flash Configuration Words.

2: 1 Write Block = 128 Instruction Words; 1 Erase Block = 1024 Instruction Words.

TABLE 4-7: SFR MAP: 0300h BLOCK

File Name	Address	All Resets	File Name	Address	All Resets
SINGLE OUTPUT CAPTURE/COMPARE/PWM			**SINGLE OUTPUT CAPTURE/COMPARE/PWM (CONTINUED)**		
CCP4CON1L	0300	0000	CCP6STATH	0356	0000
CCP4CON1H	0302	0000	CCP6TMRL	0358	0000
CCP4CON2L	0304	0000	CCP6TMRH	035A	0000
CCP4CON2H	0306	0100	CCP6PRL	035C	FFFF
CCP4CON3L	0308	0000	CCP6PRH	035E	FFFF
CCP4CON3H	030A	0000	CCP6RAL	0360	0000
CCP4STATL	030C	00x0	CCP6RAH	0362	0000
CCP4STATH	030E	0000	CCP6RBL	0364	0000
CCP4TMRL	0310	0000	CCP6RBH	0366	0000
CCP4TMRH	0312	0000	CCP6BUFL	0368	0000
CCP4PRL	0314	FFFF	CCP6BUFH	036A	0000
CCP4PRH	0316	FFFF	CCP7CON1L	036C	0000
CCP4RAL	0318	0000	CCP7CON1H	036E	0000
CCP4RAH	031A	0000	CCP7CON2L	0370	0000
CCP4RBL	031C	0000	CCP7CON2H	0372	0100
CCP4RBH	031E	0000	CCP7CON3L	0374	0000
CCP4BUFL	0320	0000	CCP7CON3H	0376	0000
CCP4BUFH	0322	0000	CCP7STATL	0378	00x0
CCP5CON1L	0324	0000	CCP7STATH	037A	0000
CCP5CON1H	0326	0000	CCP7TMRL	037C	0000
CCP5CON2L	0328	0000	CCP7TMRH	037E	0000
CCP5CON2H	032A	0100	CCP7PRL	0380	FFFF
CCP5CON3L	032C	0000	CCP7PRH	0382	FFFF
CCP5CON3H	032E	0000	CCP7RAL	0384	0000
CCP5STATL	0330	00x0	CCP7RAH	0386	0000
CCP5STATH	0332	0000	CCP7RBL	0388	0000
CCP5TMRL	0334	0000	CCP7RBH	038A	0000
CCP5TMRH	0336	0000	CCP7BUFL	038C	0000
CCP5PRL	0338	FFFF	CCP7BUFH	038E	0000
CCP5PRH	033A	FFFF	**UART**		
CCP5RAL	033C	0000	U1MODE	0398	0000
CCP5RAH	033E	0000	U1STA	039A	0110
CCP5RBL	0340	0000	U1TXREG	039C	x0xx
CCP5RBH	0342	0000	U1RXREG	039E	0000
CCP5BUFL	0344	0000	U1BRG	03A0	0000
CCP5BUFH	0346	0000	U1ADMD	03A2	0000
CCP6CON1L	0348	0000	U2MODE	03AE	0000
CCP6CON1H	034A	0000	U2STA	03B0	0110
CCP6CON2L	034C	0000	U2TXREG	03B2	xxxx
CCP6CON2H	034E	0100	U2RXREG	03B4	0000
CCP6CON3L	0350	0000	U2BRG	03B6	0000
CCP6CON3H	0352	0000	U2ADMD	03B8	0000
CCP6STATL	0354	00x0	U3MODE	03C4	0000

Legend: — = unimplemented, read as '0'; x = undefined. Reset values are shown in hexadecimal.

FIGURE 4-10: PROGRAM SPACE VISIBILITY OPERATION TO ACCESS LOWER WORD

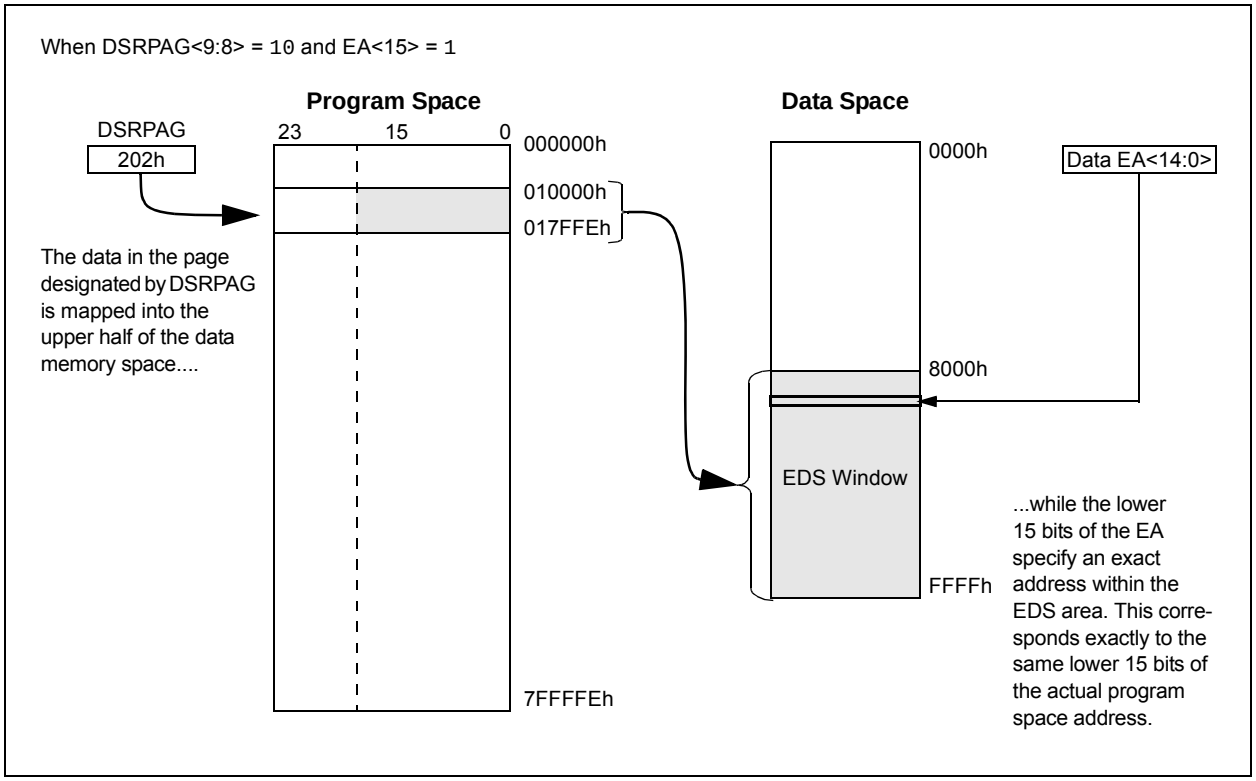
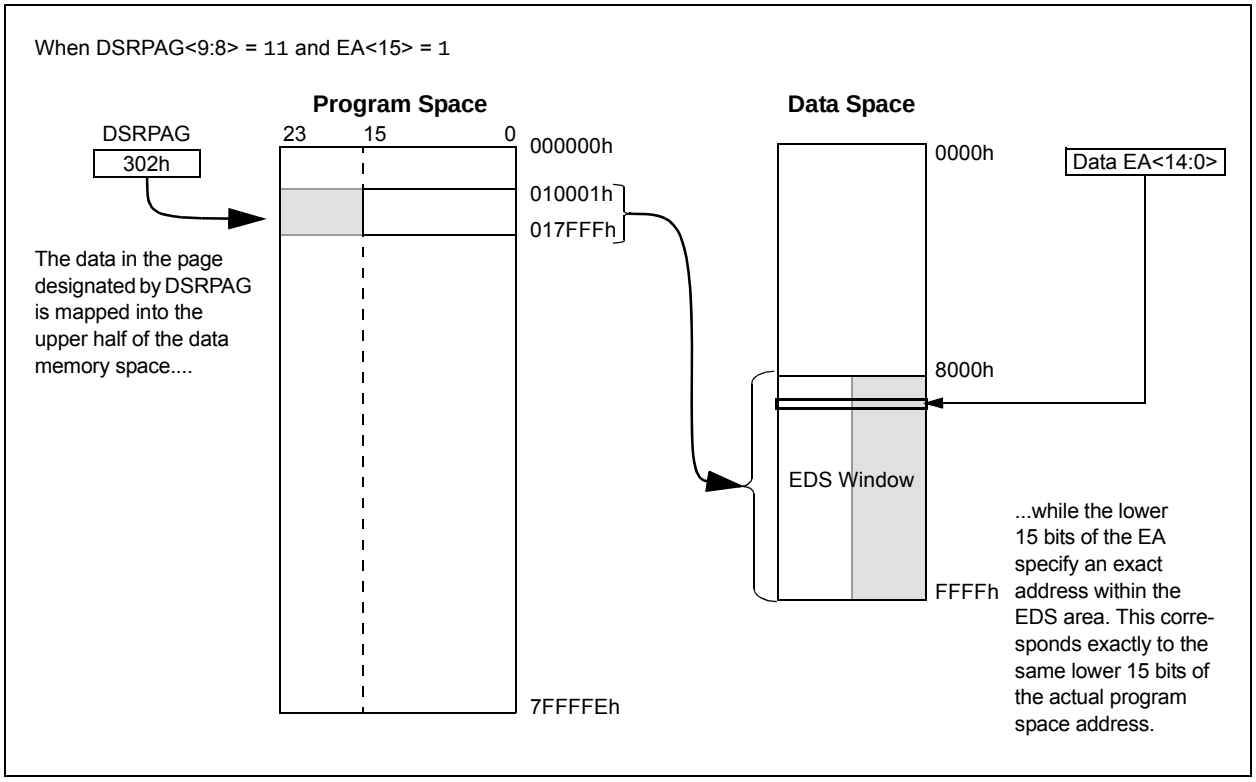


FIGURE 4-11: PROGRAM SPACE VISIBILITY OPERATION TO ACCESS UPPER WORD



REGISTER 9-7: OSCFDIV: OSCILLATOR FRACTIONAL DIVISOR REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRIM<0:7>							
bit 15							bit 8

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
TRIM8	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **TRIM<0:8>:** Trim bits

Provides fractional additive to the DIV<14:0> value for the 1/2 period of the oscillator clock.
0000_0000_0 = 0/512 (0.0) divisor added to DIVx value
0000_0000_1 = 1/512 (0.001953125) divisor added to DIVx value
0000_0001_0 = 2/512 (0.00390625) divisor added to DIVx value
•
•
•
100000000 = 256/512 (0.5000) divisor added to DIVx value
•
•
•
1111_1111_0 = 510/512 (0.99609375) divisor added to DIVx value
1111_1111_1 = 511/512 (0.998046875) divisor added to DIVx value

bit 6-0 **Unimplemented:** Read as '0'

Note 1: TRIMx values greater than zero are ONLY valid when DIVx values are greater than zero.

REGISTER 11-14: RPINR2: PERIPHERAL PIN SELECT INPUT REGISTER 2

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	OCTRIG2R5	OCTRIG2R4	OCTRIG2R3	OCTRIG2R2	OCTRIG2R1	OCTRIG2R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	INT4R5	INT4R4	INT4R3	INT4R2	INT4R1	INT4R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **OCTRIG2R<5:0>:** Assign Output Compare Trigger 2 to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **INT4R<5:0>:** Assign External Interrupt 4 (INT4) to Corresponding RPn or RPIn Pin bits

REGISTER 11-15: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	T3CKR5	T3CKR4	T3CKR3	T3CKR2	T3CKR1	T3CKR0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	T2CKR5	T2CKR4	T2CKR3	T2CKR2	T2CKR1	T2CKR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **T3CKR<5:0>**: Assign Timer3 Clock to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **T2CKR<5:0>:** Assign Timer2 Clock to Corresponding RPn or RPIn Pin bits

REGISTER 20-8: U1CON: USB CONTROL REGISTER (HOST MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-x, HSC	R-x, HSC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
JSTATE	SE0	TOKBUSY	USBRST	HOSTEN	RESUME	PPBRST	SOFEN
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **JSTATE:** Live Differential Receiver J-State Flag bit
- 1 = J-state (differential '0' in low speed, differential '1' in full speed) is detected on the USB
- 0 = No J-state is detected

bit 6 **SE0:** Live Single-Ended Zero Flag bit
- 1 = Single-ended zero is active on the USB bus
- 0 = No single-ended zero is detected

bit 5 **TOKBUSY:** Token Busy Status bit
- 1 = Token is being executed by the USB module in On-The-Go state
- 0 = No token is being executed

bit 4 **USBRST:** USB Module Reset bit
- 1 = USB Reset has been generated for a software Reset; application must set this bit for 50 ms, then clear it
- 0 = USB Reset is terminated

bit 3 **HOSTEN:** Host Mode Enable bit
- 1 = USB host capability is enabled; pull-downs on D+ and D- are activated in hardware
- 0 = USB host capability is disabled

bit 2 **RESUME:** Resume Signaling Enable bit
- 1 = Resume signaling is activated; software must set bit for 10 ms and then clear to enable remote wake-up
- 0 = Resume signaling is disabled

bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
- 1 = Resets all Ping-Pong Buffer Pointers to the even BD banks
- 0 = Ping-Pong Buffer Pointers are not reset

bit 0 **SOFEN:** Start-of-Frame Enable bit
- 1 = Start-of-Frame token is sent every one 1 ms
- 0 = Start-of-Frame token is disabled

REGISTER 21-3: PMCON3: EPMP CONTROL REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTWREN	PTRDEN	PTBE1EN	PTBE0EN	—	AWAITM1	AWAITM0	AWAITE
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PTWREN:** Write/Enable Strobe Port Enable bit
1 = PMWR/PMENB port is enabled
0 = PMWR/PMENB port is disabled

bit 14 **PTRDEN:** Read/Write Strobe Port Enable bit
1 = PMRD/$\overline{\text{PMWR}}$ port is enabled
0 = PMRD/$\overline{\text{PMWR}}$ port is disabled

bit 13 **PTBE1EN:** High Nibble/Byte Enable Port Enable bit
1 = PMBE1 port is enabled
0 = PMBE1 port is disabled

bit 12 **PTBE0EN:** Low Nibble/Byte Enable Port Enable bit
1 = PMBE0 port is enabled
0 = PMBE0 port is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-9 **AWAITM<1:0>:** Address Latch Strobe Wait States bits
11 = Wait of 3½ TCY
10 = Wait of 2½ TCY
01 = Wait of 1½ TCY
00 = Wait of ½ TCY

bit bit 8 **AWAITE:** Address Hold After Address Latch Strobe Wait States bits
1 = Wait of 1¼ TCY
0 = Wait of ¼ TCY

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 24-1: CLCxCONL: CLCx CONTROL REGISTER (LOW) (CONTINUED)

bit 2-0 **MODE<2:0>:** CLCx Mode bits
111 = Cell is a 1-input transparent latch with S and R
110 = Cell is a JK flip-flop with R
101 = Cell is a 2-input D flip-flop with R
100 = Cell is a 1-input D flip-flop with S and R
011 = Cell is an SR latch
010 = Cell is a 4-input AND
001 = Cell is an OR-XOR
000 = Cell is a AND-OR

REGISTER 24-2: CLCxCONH: CLCx CONTROL REGISTER (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	G4POL	G3POL	G2POL	G1POL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3 **G4POL:** Gate 4 Polarity Control bit
1 = The output of Channel 4 logic is inverted when applied to the logic cell
0 = The output of Channel 4 logic is not inverted

bit 2 **G3POL:** Gate 3 Polarity Control bit
1 = The output of Channel 3 logic is inverted when applied to the logic cell
0 = The output of Channel 3 logic is not inverted

bit 1 **G2POL:** Gate 2 Polarity Control bit
1 = The output of Channel 2 logic is inverted when applied to the logic cell
0 = The output of Channel 2 logic is not inverted

bit 0 **G1POL:** Gate 1 Polarity Control bit
1 = The output of Channel 1 logic is inverted when applied to the logic cell
0 = The output of Channel 1 logic is not inverted

25.0 12-BIT A/D CONVERTER WITH THRESHOLD DETECT

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the 12-Bit A/D Converter, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"12-Bit A/D Converter with Threshold Detect"** (DS39739), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

The A/D Converter has the following key features:

- Successive Approximation Register (SAR) Conversion
- Selectable 10-Bit or 12-Bit (default) Conversion Resolution
- Conversion Speeds of up to 200 ksps (12-bit)
- Up to 24 Analog Input Channels (internal and external)
- Multiple Internal Reference Input Channels
- External Voltage Reference Input Pins
- Unipolar Differential Sample-and-Hold (S/H) Amplifier
- Automated Threshold Scan and Compare Operation to Pre-Evaluate Conversion Results
- Selectable Conversion Trigger Source
- Fixed Length (one word per channel), Configurable Conversion Result Buffer
- Four Options for Results Alignment
- Configurable Interrupt Generation
- Enhanced DMA Operations with Indirect Address Generation
- Operation During CPU Sleep and Idle modes

The 12-bit A/D Converter module is an enhanced version of the 10-bit module offered in earlier PIC24 devices. It is a Successive Approximation Register (SAR) Converter, enhanced with 12-bit resolution, a wide range of automatic sampling options, tighter integration with other analog modules and a configurable results buffer.

It also includes a unique Threshold Detect feature that allows the module itself to make simple decisions based on the conversion results, and enhanced operation with the DMA Controller through Peripheral Indirect Addressing (PIA).

A simplified block diagram for the module is shown in Figure 25-1.

25.1 Basic Operation

To perform a standard A/D conversion:

1. Configure the module:
   a) Configure port pins as analog inputs by setting the appropriate bits in the ANSx registers (see **Section 11.2 "Configuring Analog Port Pins (ANSx)"** for more information).
   b) Select the voltage reference source to match the expected range on analog inputs (AD1CON2<15:13>).
   c) Select the positive and negative multiplexer inputs for each channel (AD1CHS<15:0>).
   d) Select the analog conversion clock to match the desired data rate with the processor clock (AD1CON3<7:0>).
   e) Select the appropriate sample/conversion sequence (AD1CON1<7:4> and AD1CON3<12:8>).
   f) For Channel A scanning operations, select the positive channels to be included (AD1CSSH and AD1CSSL registers).
   g) Select how conversion results are presented in the buffer (AD1CON1<9:8> and AD1CON5 register).
   h) Select the interrupt rate (AD1CON2<5:2>).
   i) Turn on A/D module (AD1CON1<15>).
2. Configure the A/D interrupt (if required):
   a) Clear the AD1IF bit (IFS0<13>).
   b) Enable the AD1IE interrupt (IEC0<13>).
   c) Select the A/D interrupt priority (IPC3<6:4>).
3. If the module is configured for manual sampling, set the SAMP bit (AD1CON1<1>) to begin sampling.

REGISTER 25-7: ANCFG: A/D BAND GAP REFERENCE CONFIGURATION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	VBGUSB(1)	VBGADC(1)	VBGCMP(1)	VBGEN(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **VBGUSB:** Band Gap Reference Enable for USB bit(1)
1 = Band gap reference is enabled
0 = Band gap reference is disabled

bit 2 **VBGADC:** Band Gap Reference Enable for A/D bit(1)
1 = Band gap reference is enabled
0 = Band gap reference is disabled

bit 1 **VBGCMP:** Band Gap Reference Enable for CTMU and Comparator bit(1)
1 = Band gap reference is enabled
0 = Band gap reference is disabled

bit 0 **VBGEN:** Band Gap Reference Enable for VREG, BOR, HLVD, FRC, DCO, NVM and A/D Boost bit(1)
1 = Band gap reference is enabled
0 = Band gap reference is disabled

Note 1: When a module requests a band gap reference voltage, that reference will be enabled automatically after a brief start-up time. The user can manually enable the band gap references using the ANCFG register before enabling the module requesting the band gap reference to avoid this startup time (~1 ms).

REGISTER 30-4: FBSLIM CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	U-1	U-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
—	—	—	BSLIM<12:8>				
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
BSLIM<7:0>							
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘1’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-13 **Unimplemented:** Read as ‘1’

bit 12-0 **BSLIM<12:0>:** Active Boot Segment Code Flash Page Address Limit (Inverted) bits

This bit field contains the last active Boot Segment Page + 1 (i.e., first page address of GS). The value is stored as an inverted page address, such that programming additional ‘0’s can only increase the size of BS. If BSLIM<12:0> is set to all ‘1’s (unprogrammed default), active Boot Segment size is zero.

REGISTER 30-6: FOSCSEL CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	U-1	U-1	U-1	U-1	U-1	r-0	r-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
IESO	PLLMODE3	PLLMODE2	PLLMODE1	PLLMODE0	FNOSC2	FNOSC1	FNOSC0
bit 7							bit 0

Legend:	PO = Program Once bit	r = Reserved bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘1’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-10 **Unimplemented:** Read as ‘1’

bit 9-8 **Reserved:** Maintain as ‘0’

bit 7 **IESO:** Two-Speed Oscillator Start-up Enable bit
1 = Starts up the device with FRC, then automatically switches to the user-selected oscillator when ready
0 = Starts up the device with the user-selected oscillator source

bit 6-3 **PLLMODE<3:0>:** Frequency Multiplier Select bits
1111 = No PLL is used (PLLEN bit is unavailable)
1110 = 8x PLL is selected
1101 = 6x PLL is selected
1100 = 4x PLL is selected
0111 = 96 MHz USB PLL is selected (Input Frequency = 48 MHz)
0110 = 96 MHz USB PLL is selected (Input Frequency = 32 MHz)
0101 = 96 MHz USB PLL is selected (Input Frequency = 24 MHz)
0100 = 96 MHz USB PLL is selected (Input Frequency = 20 MHz)
0011 = 96 MHz USB PLL is selected (Input Frequency = 16 MHz)
0010 = 96 MHz USB PLL is selected (Input Frequency = 12 MHz)
0001 = 96 MHz USB PLL is selected (Input Frequency = 8 MHz)
0000 = 96 MHz USB PLL is selected (Input Frequency = 4 MHz)

bit 2-0 **FNOSC<2:0>:** Oscillator Selection bits
111 = Oscillator with Frequency Divider (OSCFDIV)
110 = Digitally Controlled Oscillator (DCO)
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator with PLL (XTPLL, HSPLL, ECPLL)
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator with PLL (FRCPLL)
000 = Fast RC Oscillator (FRC)

TABLE 30-2: DEVICE ID REGISTERS

Address	Name	Bit															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FF0000h	DEVID	FAMID<7:0>								DEV<7:0>							
FF0002h	DEVREV	—												REV<3:0>			

TABLE 30-3: DEVICE ID BIT FIELD DESCRIPTIONS

Bit Field	Register	Description
FAMID<7:0>	DEVID	Encodes the family ID of the device.
DEV<7:0>	DEVID	Encodes the individual ID of the device.
REV<3:0>	DEVREV	Encodes the sequential (numerical) revision identifier of the device.

TABLE 30-4: PIC24FJ1024GA610/GB610 FAMILY DEVICE IDs

Device	DEVID
PIC24FJ128GA606	6000h
PIC24FJ256GA606	6008h
PIC24FJ512GA606	6010h
PIC24FJ1024GA606	6018h
PIC24FJ128GA610	6001h
PIC24FJ256GA610	6009h
PIC24FJ512GA610	6011h
PIC24FJ1024GA610	6019h
PIC24FJ128GB606	6004h
PIC24FJ256GB606	600Ch
PIC24FJ512GB606	6014h
PIC24FJ1024GB606	601Ch
PIC24FJ128GB610	6005h
PIC24FJ256GB610	600Dh
PIC24FJ512GB610	6015h
PIC24FJ1024GB610	601Dh

30.2 Unique Device Identifier (UDID)

All PIC24FJ1024GA610/GB610 family devices are individually encoded during final manufacturing with a Unique Device Identifier, or UDID. The UDID cannot be erased by a bulk erase command or any other user-accessible means. This feature allows for manufacturing traceability of Microchip Technology devices in applications where this is a requirement. It may also be used by the application manufacturer for any number of things that may require unique identification, such as:

- Tracking the device
- Unique serial number
- Unique security key

The UDID comprises five 24-bit program words. When taken together, these fields form a unique 120-bit identifier.

The UDID is stored in five read-only locations, located between 801600h and 801608h in the device configuration space. Table 30-5 lists the addresses of the identifier words.

TABLE 30-5: UDID ADDRESSES

UDID	Address	Description
UDID1	801600	UDID Word 1
UDID2	801602	UDID Word 2
UDID3	801604	UDID Word 3
UDID4	801606	UDID Word 4
UDID5	801608	UDID Word 5

TABLE 33-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage(3)**					
DI10		I/O Pins with ST Buffer	VSS	—	0.2 VDD	V	
DI11		I/O Pins with TTL Buffer	VSS	—	0.15 VDD	V	
DI15		$\overline{MCLR}$	VSS	—	0.2 VDD	V	
DI16		OSCI (XT mode)	VSS	—	0.2 VDD	V	
DI17		OSCI (HS mode)	VSS	—	0.2 VDD	V	
DI18		I/O Pins with I2C Buffer	VSS	—	0.3 VDD	V	
DI19		I/O Pins with SMBus Buffer	VSS	—	0.8	V	SMBus is enabled
	VIH	**Input High Voltage(3)**					
DI20		I/O Pins with ST Buffer:					
		with Analog Functions,	0.8 VDD	—	VDD	V	
		Digital Only	0.8 VDD	—	5.5	V	
DI21		I/O Pins with TTL Buffer:					
		with Analog Functions,	0.25 VDD + 0.8	—	VDD	V	
		Digital Only	0.25 VDD + 0.8	—	5.5	V	
DI25		$\overline{MCLR}$	0.8 VDD	—	VDD	V	
DI26		OSCI (XT mode)	0.7 VDD	—	VDD	V	
DI27		OSCI (HS mode)	0.7 VDD	—	VDD	V	
DI28		I/O Pins with I2C Buffer:					
		with Analog Functions,	0.7 VDD	—	VDD	V	
		Digital Only	0.7 VDD	—	5.5	V	
DI29		I/O Pins with SMBus Buffer:					
		with Analog Functions,	2.1	—	VDD	V	2.5V ≤ VPIN ≤ VDD
		Digital Only	2.1	—	5.5	V	
DI30	ICNPU	**CNx Pull-up Current**	150		450	µA	VDD = 3.3V, VPIN = VSS
DI30A	ICNPD	**CNx Pull-Down Current**	230		500	µA	VDD = 3.3V, VPIN = VDD
	IIL	**Input Leakage Current(2)**					
DI50		I/O Ports	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, pin at high-impedance
DI51		Analog Input Pins	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, pin at high-impedance
DI55		$\overline{MCLR}$	—	—	±1	µA	VSS ≤ VPIN ≤ VDD
DI56		OSCI/CLKI	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, EC, XT and HS modes

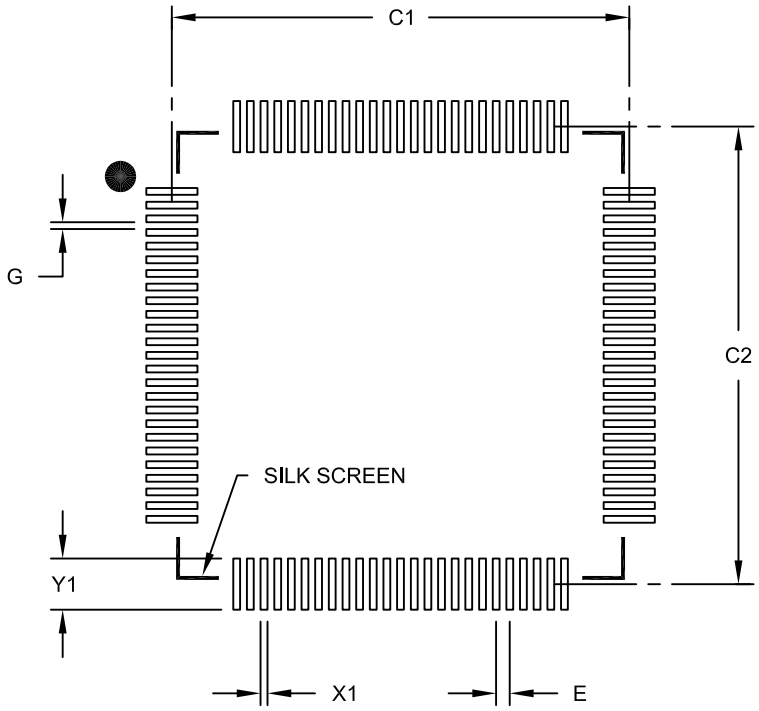
Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Negative current is defined as current sourced by the pin.

3: Refer to Table 1-1 for I/O pin buffer types.

100-Lead Plastic Thin Quad Flatpack (PT)- 12x12x1mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Contact Pad Spacing	C1		13.40	
Contact Pad Spacing	C2		13.40	
Contact Pad Width (X100)	X1			0.20
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2100B