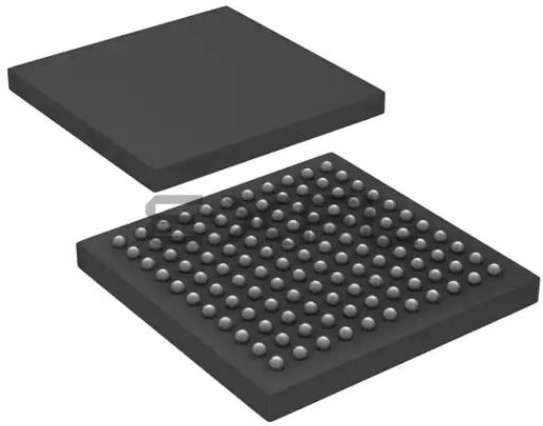
Microchip Technology - PIC24FJ256GB610T-I/BG Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256gb610t-i-bg

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TABLE 1-3: PIC24FJ1024GA610/GB610 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locator						I/O	Input Buffer	Description
	GA606 64-Pin QFN/TQFP/ QFP	GB606 64-Pin QFN/ TQFP/QFP	GA610 100-Pin TQFP/ QFP	GB610 100-Pin TQFP/ QFP	GA612 121-Pin BGA	GB612 121-Pin BGA			
IOCD0	46	46	72	72	D9	D9	I	ST	PORTD Interrupt-on-Change
IOCD1	49	49	76	76	A11	A11	I	ST	
IOCD2	50	50	77	77	A10	A10	I	ST	
IOCD3	51	51	78	78	B9	B9	I	ST	
IOCD4	52	52	81	81	C8	C8	I	ST	
IOCD5	53	53	82	82	B8	B8	I	ST	
IOCD6	54	54	83	83	D7	D7	I	ST	
IOCD7	55	55	84	84	C7	C7	I	ST	
IOCD8	42	42	68	68	E9	E9	I	ST	
IOCD9	43	43	69	69	E10	E10	I	ST	
IOCD10	44	44	70	70	D11	D11	I	ST	
IOCD11	45	45	71	71	C11	C11	I	ST	
IOCD12	—	—	79	79	A9	A9	I	ST	
IOCD13	—	—	80	80	D8	D8	I	ST	
IOCD14	—	—	47	47	L9	L9	I	ST	
IOCD15	—	—	48	48	K9	K9	I	ST	
IOCE0	60	60	93	93	A4	A4	I	ST	PORTE Interrupt-on-Change
IOCE1	61	61	94	94	B4	B4	I	ST	
IOCE2	62	62	98	98	B3	B3	I	ST	
IOCE3	63	63	99	99	A2	A2	I	ST	
IOCE4	64	64	100	100	A1	A1	I	ST	
IOCE5	1	1	3	3	D3	D3	I	ST	
IOCE6	2	2	4	4	C1	C1	I	ST	
IOCE7	3	3	5	5	D2	D2	I	ST	
IOCE8	—	—	18	18	G1	G1	I	ST	
IOCE9	—	—	19	19	G2	G2	I	ST	

Legend: TTL = TTL input buffer
ANA = Analog level input/output
DIG = Digital input/output
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated Transceiver

2.2 Power Supply Pins

2.2.1 DECOUPLING CAPACITORS

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS, is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A 0.1 μF (100 nF), 16V-50V capacitor is recommended. The capacitor should be a low-ESR device with a self-resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μF to 0.001 μF. Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1 μF in parallel with 0.001 μF).
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

2.2.2 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including microcontrollers to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μF to 47 μF.

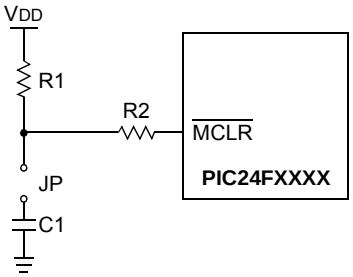
2.3 Master Clear ($\overline{MCLR}$) Pin

The $\overline{MCLR}$ pin provides two specific device functions: device Reset, and device programming and debugging. If programming and debugging are not required in the end application, a direct connection to VDD may be all that is required. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{MCLR}$ pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R1 and C1 will need to be adjusted based on the application and PCB requirements. For example, it is recommended that the capacitor, C1, be isolated from the $\overline{MCLR}$ pin during programming and debugging operations by using a jumper (Figure 2-2). The jumper is replaced for normal run-time operations.

Any components associated with the $\overline{MCLR}$ pin should be placed within 0.25 inch (6 mm) of the pin.

FIGURE 2-2: EXAMPLE OF $\overline{MCLR}$ PIN CONNECTIONS



Note 1: R1 ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the $\overline{MCLR}$ pin VIH and VIL specifications are met.

2: R2 ≤ 470Ω will limit any current flowing into $\overline{MCLR}$ from the external capacitor, C, in the event of a $\overline{MCLR}$ pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the $\overline{MCLR}$ pin VIH and VIL specifications are met.

2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface-mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the internal voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

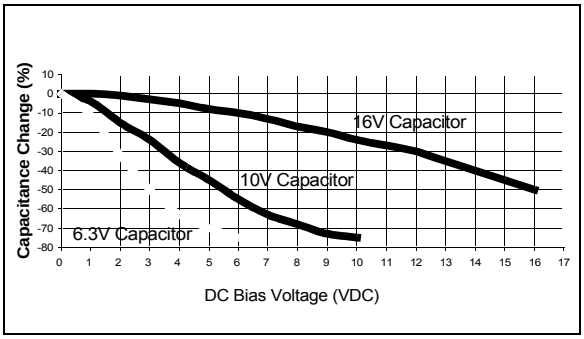
Typical low-cost, 10 μF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as ±10% to ±20% (X5R and X7R) or -20%/+80% (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex: ±15% over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of +22%/-82%. Due to the extreme temperature tolerance, a 10 μF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum internal voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the internal regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

A typical DC bias voltage vs. capacitance graph for X7R type capacitors is shown in Figure 2-4.

FIGURE 2-4: DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS



When selecting a ceramic capacitor to be used with the internal voltage regulator, it is suggested to select a high-voltage rating so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at a minimum of 16V for the 1.8V core voltage. Suggested capacitors are shown in Table 2-1.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming (ICSP) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100Ω.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and pin Voltage Input High (V_{IH}) and Voltage Input Low (V_{IL}) requirements.

For device emulation, ensure that the "Communication Channel Select" pins (i.e., PGECx/PGEDx), programmed into the device, match the physical connections for the ICSP to the Microchip debugger/emulator tool.

For more information on available Microchip development tools connection requirements, refer to **Section 31.0 "Development Support"**.

TABLE 4-4: SFR MAP: 0000h BLOCK

File Name	Address	All Resets	File Name	Address	All Resets
CPU CORE			**INTERRUPT CONTROLLER (CONTINUED)**		
WREG0	0000	0000	IEC1	009A	0000
WREG1	0002	0000	IEC2	009C	0000
WREG2	0004	0000	IEC3	009E	0000
WREG3	0006	0000	IEC4	00A0	0000
WREG4	0008	0000	IEC5	00A2	0000
WREG5	000A	0000	IEC6	00A4	0000
WREG6	000C	0000	IEC7	00A6	0000
WREG7	000E	0000	IPC0	00A8	4444
WREG8	0010	0000	IPC1	00AA	4444
WREG9	0012	0000	IPC2	00AC	4444
WREG10	0014	0000	IPC3	00AE	4444
WREG11	0016	0000	IPC4	00B0	4444
WREG12	0018	0000	IPC5	00B2	4404
WREG13	001A	0000	IPC6	00B4	4444
WREG14	001C	0000	IPC7	00B6	4444
WREG15	001E	0800	IPC8	00B8	0044
SPLIM	0020	xxxx	IPC9	00BA	4444
PCL	002E	0000	IPC10	00BC	4444
PCH	0030	0000	IPC11	00BE	4444
DSRPAG	0032	0000	IPC12	00C0	4444
DSWPAG	0034	0000	IPC13	00C2	0440
RCOUNT	0036	xxxx	IPC14	00C4	4400
SR	0042	0000	IPC15	00C6	4444
CORCON	0044	0004	IPC16	00C8	4444
DISICNT	0052	xxxx	IPC17	00CA	4444
TBLPAG	0054	0000	IPC18	00CC	0044
INTERRUPT CONTROLLER			IPC19	00CE	0040
INTCON1	0080	0000	IPC20	00D0	4440
INTCON2	0082	8000	IPC21	00D2	4444
INTCON4	0086	0000	IPC22	00D4	4444
IFS0	0088	0000	IPC23	00D6	4400
IFS1	008A	0000	IPC24	00D8	4444
IFS2	008C	0000	IPC25	00DA	0440
IFS3	008E	0000	IPC26	00DC	0400
IFS4	0090	0000	IPC27	00DE	4440
IFS5	0092	0000	IPC28	00E0	4444
IFS6	0094	0000	IPC29	00E2	0044
IFS7	0096	0000	INTTREG	00E4	0000
IEC0	0098	0000			

Legend: — = unimplemented, read as '0'; x = undefined. Reset values are shown in hexadecimal.

TABLE 4-10: SFR MAP: 0600h BLOCK

File Name	Address	All Resets	File Name	Address	All Resets
I/O			**PORTD (CONTINUED)**		
PADCON	065E	0000	ANSD	06A6	FFFF
IOCSTAT	0660	0000	IOCPD	06A8	0000
PORTA(1)			IOCND	06AA	0000
TRISA	0662	FFFF	IOCFD	06AC	0000
PORTA	0664	0000	IOCPUD	06AE	0000
LATA	0666	0000	IOCPDD	06B0	0000
ODCA	0668	0000	**PORTE**		
ANSA	066A	FFFF	TRISE	06B2	FFFF
IOCPA	066C	0000	PORTE	06B4	0000
IOCNA	066E	0000	LATE	06B6	0000
IOCFA	0670	0000	ODCE	06B8	0000
IOCPUA	0672	0000	ANSE	06BA	FFFF
IOCPDA	0674	0000	IOCPE	06BC	0000
PORTB			IOCNE	06BE	0000
TRISB	0676	FFFF	IOCFE	06C0	0000
PORTB	0678	0000	IOCPUE	06C2	0000
LATB	067A	0000	IOCPDE	06C4	0000
ODCB	067C	0000	**PORTF**		
ANSB	067E	FFFF	TRISF	06C6	FFFF
IOCPB	0680	0000	PORTF	06C8	0000
IOCNB	0682	0000	LATF	06CA	0000
IOCFB	0684	0000	ODCF	06CC	0000
IOCPUB	0686	0000	IOCPF	06D0	0000
IOCPDB	0688	0000	IOCNF	06D2	0000
PORTC			IOCFF	06D4	0000
TRISC	068A	FFFF	IOCPUF	06D6	0000
PORTC	068C	0000	IOCPDF	06D8	0000
LATC	068E	0000	**PORTG**		
ODCC	0690	0000	TRISG	06DA	FFFF
ANSC	0692	FFFF	PORTG	06DC	0000
IOCPC	0694	0000	LATG	06DE	0000
IOCNC	0696	0000	ODCG	06E0	0000
IOCFC	0698	0000	ANSG	06E2	FFFF
IOCPUC	069A	0000	IOCPG	06E4	0000
IOCPDC	069C	0000	IOCNG	06E6	0000
PORTD			IOCFG	06E8	0000
TRISD	069E	FFFF	IOCPUG	06EA	0000
PORTD	06A0	0000	IOCPDG	06EC	0000
LATD	06A2	0000			
ODCD	06A4	0000			

Legend: — = unimplemented, read as '0'; x = undefined. Reset values are shown in hexadecimal.

Note 1: PORTA and all associated bits are unimplemented in 64-pin devices and read as '0'.

8.3 Interrupt Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

8.3.1 KEY RESOURCES

- **"Interrupts"** (DS70000600) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

8.4 Interrupt Control and Status Registers

PIC24FJ1024GA610/GB610 family devices implement the following registers for the interrupt controller:

- INTCON1
- INTCON2
- INTCON4
- IFS0 through IFS7
- IEC0 through IEC7
- IPC0 through IPC29
- INTTREG

8.4.1 INTCON1-INTCON4

Global interrupt control functions are controlled from INTCON1 and INTCON2. INTCON1 contains the Interrupt Nesting Disable (NSTDIS) bit, as well as the control and status flags for the processor trap sources.

The INTCON2 register controls global interrupt generation, the external interrupt request signal behavior and the use of the Alternate Interrupt Vector Table (AIVT).

The INTCON4 register contains the Software Generated Hard Trap bit (SGHT) and ECC Double-Bit Error (ECCDBE) trap.

8.4.2 IFSx

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal, and is cleared via software.

8.4.3 IECx

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

8.4.4 IPCx

The IPCx registers are used to set the Interrupt Priority Level (IPL) for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

8.4.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into the Vector Number bits (VECNUM<7:0>) and Interrupt Priority Level bits (ILR<3:0>) fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence as they are listed in Table 8-2. For example, the INT0 (External Interrupt 0) is shown as having Vector Number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0<0>, the INT0IE bit in IEC0<0> and the INT0IP bits in the first position of IPC0 (IPC0<2:0>).

8.4.6 STATUS/CONTROL REGISTERS

Although these registers are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. For more information on these registers refer to **"CPU with Extended Data Space (EDS)"** (DS39732) in the *"dsPIC33/PIC24 Family Reference Manual"*.

- The CPU STATUS Register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU Interrupt Priority Level. The user software can change the current CPU Interrupt Priority Level by writing to the IPLx bits.
- The CORCON register contains the IPL3 bit, which together with the IPL<2:0> bits, also indicates the current CPU Interrupt Priority Level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in Register 8-3 through Register 8-6 in the following pages.

REGISTER 9-10: REFOTRIML: REFERENCE OSCILLATOR TRIM REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROTRIM<0:7>							
bit 15							bit 8

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
ROTRIM8	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **ROTRIM<0:8>:** REFO Trim bits
These bits provide a fractional additive to the RODIV<14:0> value for the 1/2 period of the REFO clock.
000000000 = 0/512 (0.0 divisor added to the RODIV<14:0> value)
000000001 = 1/512 (0.001953125 divisor added to the RODIV<14:0> value)
000000010 = 2/512 (0.00390625 divisor added to the RODIV<14:0> value)
•
•
•
100000000 = 256/512 (0.5000 divisor added to the RODIV<14:0> value)
•
•
•
111111110 = 510/512 (0.99609375 divisor added to the RODIV<14:0> value)
111111111 = 511/512 (0.998046875 divisor added to the RODIV<14:0> value)

bit 6-0 **Unimplemented:** Read as ‘0’

REGISTER 11-1: ANSA: PORTA ANALOG FUNCTION SELECTION REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-1	U-0
—	—	—	—	—	ANSA<10:9>(1)		—
bit 15							bit 8

R/W-1	R/W-1	U-0	U-0	U-0	U-0	U-0	U-0
ANSA<7:6>(1)		—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-9 **ANSA<10:9>:** PORTA Analog Function Selection bits(1)
1 = Pin is configured in Analog mode; I/O port read is disabled
0 = Pin is configured in Digital mode; I/O port read is enabled

bit 8 **Unimplemented:** Read as '0'

bit 7-6 **ANSA<7:6>:** PORTA Analog Function Selection bits(1)
1 = Pin is configured in Analog mode; I/O port read is disabled
0 = Pin is configured in Digital mode; I/O port read is enabled

bit 5-0 **Unimplemented:** Read as '0'

Note 1: ANSA<10:9,7> bits are not available on 64-pin devices.

REGISTER 11-2: ANSB: PORTB ANALOG FUNCTION SELECTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANSB<15:8>							
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANSB<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **ANSB<15:0>:** PORTB Analog Function Selection bits
1 = Pin is configured in Analog mode; I/O port read is disabled
0 = Pin is configured in Digital mode; I/O port read is enabled

11.4.5 CONSIDERATIONS FOR PERIPHERAL PIN SELECTION

The ability to control Peripheral Pin Selection introduces several considerations into application design that could be overlooked. This is particularly true for several common peripherals that are available only as remappable peripherals.

The main consideration is that the Peripheral Pin Selects are not available on default pins in the device's default (Reset) state. Since all RPINRx registers reset to '111111' and all RPORx registers reset to '000000', all Peripheral Pin Select inputs are tied to Vss, and all Peripheral Pin Select outputs are disconnected.

This situation requires the user to initialize the device with the proper peripheral configuration before any other application code is executed. Since the IOLOCK bit resets in the unlocked state, it is not necessary to execute the unlock sequence after the device has come out of Reset. For application safety, however, it is best to set IOLOCK and lock the configuration after writing to the control registers.

Because the unlock sequence is timing-critical, it must be executed as an assembly language routine in the same manner as changes to the oscillator configuration. If the bulk of the application is written in 'C', or another high-level language, the unlock sequence should be performed by writing in-line assembly.

Choosing the configuration requires the review of all Peripheral Pin Selects and their pin assignments, especially those that will not be used in the application. In all cases, unused pin-selectable peripherals should be disabled completely. Unused peripherals should have their inputs assigned to an unused RPn/RPIn pin function. I/O pins with unused RPn functions should be configured with the null peripheral output.

The assignment of a peripheral to a particular pin does not automatically perform any other configuration of the pin's I/O circuitry. In theory, this means adding a pin-selectable output to a pin may mean inadvertently driving an existing peripheral input when the output is driven. Users must be familiar with the behavior of other fixed peripherals that share a remappable pin and know when to enable or disable them. To be safe, fixed digital peripherals that share the same pin should be disabled when not in use.

Along these lines, configuring a remappable pin for a specific peripheral does not automatically turn that feature on. The peripheral must be specifically configured for operation and enabled as if it were tied to a fixed pin. Where this happens in the application code (immediately following a device Reset and peripheral configuration or inside the main application routine) depends on the peripheral and its use in the application.

A final consideration is that Peripheral Pin Select functions neither override analog inputs nor reconfigure pins with analog functions for digital I/O. If a pin is configured as an analog input on a device Reset, it must be explicitly reconfigured as a digital I/O when used with a Peripheral Pin Select.

Example 11-4 shows a configuration for bidirectional communication with flow control using UART1. The following input and output functions are used:

- Input Functions: U1RX, $\overline{\text{U1CTS}}$
- Output Functions: U1TX, $\overline{\text{U1RTS}}$

EXAMPLE 11-4: CONFIGURING UART1 INPUT AND OUTPUT FUNCTIONS

```
//  Unlock Registers
asm volatile    ("MOV   #OSCCON, w1   \n"
                 "MOV    #0x46, w2    \n"
                 "MOV    #0x57, w3    \n"
                 "MOV.b  w2, [w1]     \n"
                 "MOV.b  w3, [w1]     \n"
                 "BCLR   OSCCON, #6")  ;

//  or use XC16 built-in macro:
//  __builtin_write_OSCCONL(OSCCON & 0xbf);

//  Configure Input Functions (Table 11-3)
    // Assign U1RX To Pin RP0
    RPINR18bits.U1RXR = 0;

    // Assign U1CTS To Pin RP1
    RPINR18bits.U1CTSR = 1;

//  Configure Output Functions (Table 11-4)
    // Assign U1TX To Pin RP2
    RPOR1bits.RP2R = 3;

    // Assign U1RTS To Pin RP3
    RPOR1bits.RP3R = 4;

//  Lock Registers
asm volatile   ("MOV   #OSCCON, w1   \n"
                "MOV    #0x46, w2    \n"
                "MOV    #0x57, w3    \n"
                "MOV.b  w2, [w1]     \n"
                "MOV.b  w3, [w1]     \n"
                "BSET   OSCCON, #6")  ;

//  or use XC16 built-in macro:
//  __builtin_write_OSCCONL(OSCCON | 0x40);
```

REGISTER 11-22: RPINR12: PERIPHERAL PIN SELECT INPUT REGISTER 12

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	TCKIBR5	TCKIBR4	TCKIBR3	TCKIBR2	TCKIBR1	TCKIBR0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	TCKIAR5	TCKIAR4	TCKIAR3	TCKIAR2	TCKIAR1	TCKIAR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **TCKIBR<5:0>:** Assign MCCP/SCCP Clock Input B to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **TCKIAR<5:0>:** Assign MCCP/SCCP Clock Input A to Corresponding RPn or RPIn Pin bits

REGISTER 11-23: RPINR14: PERIPHERAL PIN SELECT INPUT REGISTER 14

U-0	U-0	r-1	r-1	r-1	r-1	r-1	r-1
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	r-1	r-1	r-1	r-1	r-1	r-1
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **Reserved**: Maintain as ‘1’

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **Reserved**: Maintain as ‘1’

REGISTER 17-11: SPIxURDTL: SPIx UNDERRUN DATA REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
URDATA<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
URDATA<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **URDATA<15:0>:** SPIx Underrun Data bits

These bits are only used when URDTEN = 1. This register holds the data to transmit when a Transmit Underrun condition occurs.

When the MODE<32,16> or WLENGTH<4:0> bits select 16 to 9-bit data, the SPIx only uses URDATA<15:0>. When the MODE<32,16> or WLENGTH<4:0> bits select 8 to 2-bit data, the SPIx only uses URDATA<7:0>.

REGISTER 17-12: SPIxURDTH: SPIx UNDERRUN DATA REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
URDATA<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
URDATA<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **URDATA<31:16>:** SPIx Underrun Data bits

These bits are only used when URDTEN = 1. This register holds the data to transmit when a Transmit Underrun condition occurs.

When the MODE<32,16> or WLENGTH<4:0> bits select 32 to 25-bit data, the SPIx only uses URDATA<15:0>. When the MODE<32,16> or WLENGTH<4:0> bits select 24 to 17-bit data, the SPIx only uses URDATA<7:0>.

TABLE 21-2: ENHANCED PARALLEL MASTER PORT PIN DESCRIPTIONS

Pin Name (Alternate Function)	Type	Description
PMA<22:16>	O	Address Bus bits<22:16>
PMA15	O	Address Bus bit 15
	I/O	Data Bus bit 15 (16-bit port with Multiplexed Addressing)
(PMCS2)	O	Chip Select 2 (alternate location)
PMA14	O	Address Bus bit 14
	I/O	Data Bus bit 14 (16-bit port with Multiplexed Addressing)
(PMCS1)	O	Chip Select 1 (alternate location)
PMA<13:8>	O	Address Bus bits<13:8>
	I/O	Data Bus bits<13:8> (16-bit port with Multiplexed Addressing)
PMA<7:3>	O	Address Bus bits<7:3>
PMA2 (PMALU)	O	Address Bus bit 2
	O	Address Latch Upper Strobe for Multiplexed Address
PMA1 (PMALH)	I/O	Address Bus bit 1
	O	Address Latch High Strobe for Multiplexed Address
PMA0 (PMALL)	I/O	Address Bus bit 0
	O	Address Latch Low Strobe for Multiplexed Address
PMD<15:8>	I/O	Data Bus bits<15:8> (Demultiplexed Addressing)
PMD<7:4>	I/O	Data Bus bits<7:4>
	O	Address Bus bits<7:4> (4-bit port with 1-Phase Multiplexed Addressing)
PMD<3:0>	I/O	Data Bus bits<3:0>
PMCS1(1)	O	Chip Select 1
PMCS2(1)	O	Chip Select 2
PMWR	I/O	Write Strobe(2)
(PMENB)	I/O	Enable Signal(2)
PMRD	I/O	Read Strobe(2)
(PMRD/$\overline{\text{PMWR}}$)	I/O	Read/$\overline{\text{Write}}$ Signal(2)
PMBE1	O	Byte Indicator
PMBE0	O	Nibble or Byte Indicator
PMACK1	I	Acknowledgment Signal 1
PMACK2	I	Acknowledgment Signal 2

Note 1: These pins are implemented in 100-pin and 121-pin devices only.

2: Signal function depends on the setting of the MODE<1:0> and SM bits (PMCON1<9:8> and PMCSxCF<8>).

22.3 Registers

22.3.1 RTCC CONTROL REGISTERS

REGISTER 22-1: RTCCON1L: RTCC CONTROL REGISTER 1 (LOW)

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
RTCEN	—	—	—	WRLOCK	PWCEN	PWCPOL	PWCPOE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
RTCOE	OUTSEL2	OUTSEL1	OUTSEL0	—	—	—	TSAEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **RTCEN:** RTCC Enable bit
1 = RTCC is enabled and counts from selected clock source
0 = RTCC is not enabled

bit 14-12 **Unimplemented:** Read as ‘0’

bit 11 **WRLOCK:** RTCC Register Write Lock
1 = RTCC registers are locked
0 = RTCC registers may be written to by user

bit 10 **PWCEN:** Power Control Enable bit
1 = Power control is enabled
0 = Power control is disabled

bit 9 **PWCPOL:** Power Control Polarity bit
1 = Power control output is active-high
0 = Power control output is active-low

bit 8 **PWCPOE:** Power Control Output Enable bit
1 = Power control output pin is enabled
0 = Power control output pin is disabled

bit 7 **RTCOE:** RTCC Output Enable bit
1 = RTCC output is enabled
0 = RTCC output is disabled

bit 6-4 **OUTSEL<2:0>:** RTCC Output Signal Selection bits
111 = Unused
110 = Unused
101 = Unused
100 = Timestamp A event
011 = Power control
010 = RTCC input clock
001 = Second clock
000 = Alarm event

bit 3-1 **Unimplemented:** Read as ‘0’

bit 0 **TSAEN:** Timestamp A Enable bit
1 = Timestamp event will occur when a low pulse is detected on the $\overline{\text{TMPR}}$ pin
0 = Timestamp is disabled

REGISTER 22-13: ALMDATEL: RTCC ALARM DATE REGISTER (LOW)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-12 **DAYTEN<1:0>:** Binary Coded Decimal Value of Days ‘10’ Digit bits
Contains a value from 0 to 3.

bit 11-8 **DAYONE<3:0>:** Binary Coded Decimal Value of Days ‘1’ Digit bits
Contains a value from 0 to 9.

bit 7-3 **Unimplemented:** Read as ‘0’

bit 2-0 **WDAY<2:0>:** Binary Coded Decimal Value of Weekdays ‘1’ Digit bits
Contains a value from 0 to 6.

REGISTER 22-14: ALMDATEH: RTCC ALARM DATE REGISTER (HIGH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	MTHTEN	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **YRTEN<3:0>:** Binary Coded Decimal Value of Years ‘10’ Digit bits

bit 11-8 **YRONE<3:0>:** Binary Coded Decimal Value of Years ‘1’ Digit bits

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **MTHTEN:** Binary Coded Decimal Value of Months ‘10’ Digit bit
Contains a value from 0 to 1.

bit 3-0 **MTHONE<3:0>:** Binary Coded Decimal Value of Months ‘1’ Digit bits
Contains a value from 0 to 9.

25.4 Achieving Maximum A/D Converter (ADC) Performance

In order to get the shortest overall conversion time (called the "throughput") while maintaining accuracy, several factors must be considered. These are described in detail below.

- Dependence of AVDD – If the AVDD supply is < 2.7V, the Charge Pump Enable bit (PUMPEN, AD1CON3<13>) should be set to '1'. The input channel multiplexer has a varying resistance with AVDD (the lower AVDD, the higher the internal switch resistance). The charge pump provides a higher internal AVDD to keep the switch resistance as low as possible.
- Dependence on TAD – The ADC timing is driven by TAD, not TCYC. Selecting the TAD time correctly is critical to getting the best ADC throughput. It is important to note that the overall ADC throughput is not simply the 'Conversion Time' of the SAR; it is the combination of the Conversion Time, the Sample Time and additional TAD delays for internal synchronization logic.
- Relationship between TCYC and TAD – There is not a fixed 1:1 timing relationship between TCYC and TAD. The fastest possible throughput is fundamentally set by TAD (min), not by TCYC. The TAD time is set as a programmable integer multiple of TCYC by the ADCS<7:0> bits. Referring to Table 33-26, the TAD (min) time is greater than the 4 MHz period of the dedicated ADC RC clock generator. Therefore, TAD must be 2 TCYC in order to use the RC clock for fastest throughput. The TAD (min) is a multiple of 3.597 MHz as opposed to 4 MHz. To run as fast as possible, TCYC must be a multiple of TAD (min) because values of ADCSx are integers. For example, if a standard "color burst" crystal of 14.31818 MHz is used, TCYC is 279.4 ns, which is very close to TAD (min) and the ADC throughput is optimal. Running at 16 MHz will actually reduce the throughput, because TAD will have to be 500 ns as the TCYC of 250 ns violates TAD (min).
- Dependence on driving Source Resistance (RS) – Certain transducers have high output impedance (> 2.5 kΩ). Having a high RS will require longer sampling time to charge the S/H capacitor through the resistance path (see Figure 25-3). The worst case scenario is a full-range voltage step of AVSS to AVDD, with the sampling cap at AVSS. The capacitor time constant is (RS + RIC + RSS) (CHOLD) and the sample time needs to be 6 time constants minimum (8 preferred). Since the ADC logic timing is TAD-based, the sample time (in TAD) must be long enough, over all conditions, to charge/discharge CHOLD. Do not assume one TAD is sufficient sample time; longer times may be required to achieve the accuracy needed by the application. The value of CHOLD is 40 pF.

A small amount of charge is present at the ADC input pin when the sample switch is closed. If RS is high, this will generate a DC error exceeding 1 LSB. Keeping RS < 50Ω is recommenced for best results. The error can also be reduced by increasing sample time (a 2 kΩ value of RS requires a 3 µS sample time to eliminate the error).

- Calculating Throughput – The throughput of the ADC is based on TAD. The throughput is given by:

$$Throughput = \left(\frac{1}{Sample\ Time + SAR\ Conversion\ Time + Clock\ Sync\ Time}\right)$$

where:

Sample Time is the calculated TAD periods for the application.

SAR Conversion Time is 12 TAD for 10-bit and 14 TAD for 12-bit conversions.

Clock Sync Time is 2.5 TAD (worst case scenario).

For example, using an 8 MHz FRC means the TCYC = 250 ns. This requires: TAD = 2 TCYC = 500 ns. Therefore, the throughput is:

$$Throughput = \left(\frac{1}{500\ ns + 14 \cdot 500\ ns + 2.5 \cdot 500\ ns}\right) = 114.28\ KS/sec$$

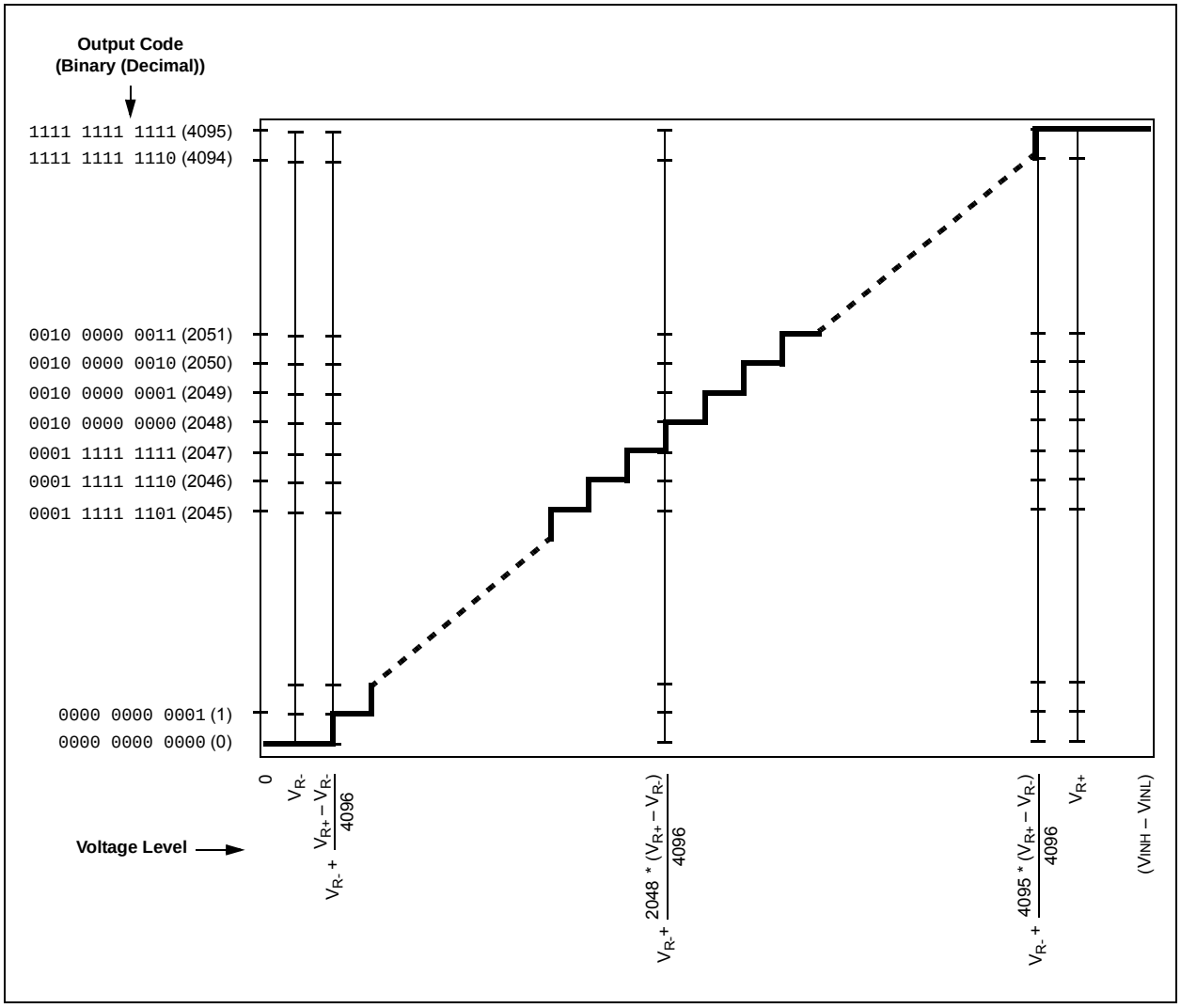
Note that the clock sync delay could be as little as 1.5 TAD, which could produce 121 KS/sec, but that cannot be ensured as the timing relationship is asynchronous and not specified. The worst case timing of 2.5 TAD should be used to calculate throughput.

For example, if a certain transducer has a 20 kΩ output impedance, the maximum sample time is determined by:

$$Sample\ Time = 6 \cdot (RS + RIC + RSS) \cdot CHOLD$$
$$= 6 \cdot (20K + 250 + 350) \cdot 40\ pF$$
$$= 4.95\ \mu S$$

If TAD = 500 ns, this requires a Sample Time of 4.95 us/ 500 ns = 10 TAD (for a full-step voltage on the transducer output).

FIGURE 25-4: 12-BIT A/D TRANSFER FUNCTION



REGISTER 30-7: FOSC CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
FCKSM1	FCKSM0	IOL1WAY	PLLSS(1)	SOSCSEL	OSCIOFCN	POSCMD1	POSCMD0
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘1’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-8 **Unimplemented:** Read as ‘1’

bit 7-6 **FCKSM<1:0>:** Clock Switching and Monitor Selection bits
1x = Clock switching and the Fail-Safe Clock Monitor are disabled
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
00 = Clock switching and the Fail-Safe Clock Monitor are enabled

bit 5 **IOL1WAY:** Peripheral Pin Select Configuration bit
1 = The IOLOCK bit can be set only once (with unlock sequence).
0 = The IOLOCK bit can be set and cleared as needed (with unlock sequence)

bit 4 **PLLSS:** PLL Source Selection Configuration bit(1)
1 = PLL is fed by the Primary Oscillator (EC, XT or HS mode)
0 = PLL is fed by the on-chip Fast RC (FRC) Oscillator

bit 3 **SOSCSEL:** SOSC Selection Configuration bit
1 = Crystal (SOSCI/SOSCO) mode
0 = Digital (SOSCI) mode

bit 2 **OSCIOFCN:** CLKO Enable Configuration bit
1 = CLKO output signal is active on the OSCO pin (when the Primary Oscillator is disabled or configured for EC mode)
0 = CLKO output is disabled

bit 1-0 **POSCMD<1:0>:** Primary Oscillator Configuration bits
11 = Primary Oscillator mode is disabled
10 = HS Oscillator mode is selected (10 MHz-32 MHz)
01 = XT Oscillator mode is selected (1.5 MHz-10 MHz)
00 = External Clock mode is selected

Note 1: When the primary clock source is greater than 8 MHz, this bit must be set to ‘0’ to prevent overclocking the PLL.

TABLE 33-3: DC CHARACTERISTICS: TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Operating Voltage							
DC10	VDD	**Supply Voltage**	2.0	—	3.6	V	BOR is disabled
			VBOR	—	3.6	V	BOR is enabled
DC12	VDR	**RAM Data Retention Voltage(1)**	Greater of: VPORREL or VBOR	—	—	V	VBOR is used only if BOR is enabled (BOREN = 1)
DC16	VPOR	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	VSS	—	—	V	**(Note 2)**
DC17A	SVDD	**Recommended VDD Rise Rate** to Ensure Internal Power-on Reset Signal	1V/20 ms	—	1V/10 µS	sec	**(Note 2, Note 4)**
DC17B	VBOR	**Brown-out Reset Voltage** on VDD Transition, High-to-Low	2.0	2.1	2.2	V	**(Note 3)**

Note 1: This is the limit to which VDD may be lowered and the RAM contents will always be retained.

2: If the VPOR or SVDD parameters are not met, or the application experiences slow power-down VDD ramp rates, it is recommended to enable and use BOR.

3: On a rising VDD power-up sequence, application firmware execution begins at the higher of the VPORREL or VBOR level (when BOREN = 1).

4: VDD rise times outside this window may not internally reset the processor and are not parametrically tested.

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