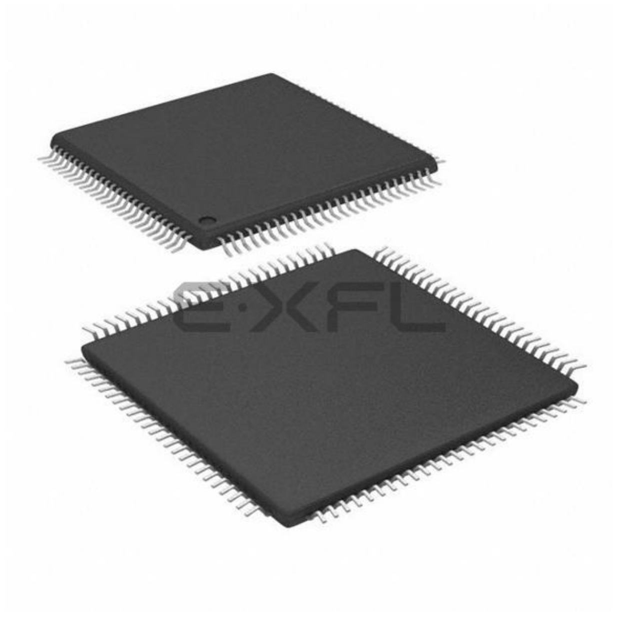

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj256gb610t-i-pt

Pin Diagrams[(1)] (Continued)

PIC24FJXXXGA610 121-Pin BGA

	1	2	3	4	5	6	7	8	9	10	11
A	RE4	RE3	RG13	RE0	RG0	RF1	N/C	N/C	RD12	RD2	RD1
B	N/C	RG15	RE2	RE1	RA7	RF0	VCAP	RD5	RD3	VSS	RC14
C	RE6	VDD	RG12	RG14	RA6	N/C	RD7	RD4	N/C	RC13	RD11
D	RC1	RE7	RE5	N/C	N/C	N/C	RD6	RD13	RD0	N/C	RD10
E	RC4	RC3	RG6	RC2	N/C	RG1	N/C	RA15	RD8	RD9	RA14
F	$\overline{\text{MCLR}}$	RG8	RG9	RG7	VSS	N/C	N/C	VDD	RC12	VSS	RC15
G	RE8	RE9	RA0	N/C	VDD	VSS	VSS	N/C	RA5	RA3	RA4
H	RB5	RB4	N/C	N/C	N/C	VDD	N/C	RF7	RF6	RG2	RA2
J	RB3	RB2	RB7	AVDD	RB11	RA1	RB12	N/C	N/C	RF8	RG3
K	RB1	RB0	RA10	RB8	N/C	RF12	RB14	VDD	RD15	RF3	RF2
L	RB6	RA9	AVSS	RB9	RB10	RF13	RB13	RB15	RD14	RF4	RF5

Legend: See Table 6 for a complete description of pin functions. Pinouts are subject to change.

Note 1: Gray shading indicates 5.5V tolerant input pins.

TABLE 1-3: PIC24FJ1024GA610/GB610 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locator						I/O	Input Buffer	Description
	GA606 64-Pin QFN/TQFP/QFP	GB606 64-Pin QFN/TQFP/QFP	GA610 100-Pin TQFP/QFP	GB610 100-Pin TQFP/QFP	GA612 121-Pin BGA	GB612 121-Pin BGA			
IOCF0	58	58	87	87	B6	B6	I	ST	PORTF Interrupt-on-Change
IOCF1	59	59	88	88	A6	A6	I	ST	
IOCF2	34	—	52	52	K11	K11	I	ST	
IOCF3	33	33	51	51	K10	K10	I	ST	
IOCF4	31	31	49	49	L10	L10	I	ST	
IOCF5	32	32	50	50	L11	L11	I	ST	
IOCF6	35	—	55	—	H9	—	I	ST	
IOCF7	—	34	54	54	H8	H8	I	ST	
IOCF8	—	—	53	53	J10	J10	I	ST	
IOCF12	—	—	40	40	K6	K6	I	ST	
IOCF13	—	—	39	39	L6	L6	I	ST	
IOCG0	—	—	90	90	A5	A5	I	ST	PORTG Interrupt-on-Change
IOCG1	—	—	89	89	E6	E6	I	ST	
IOCG2	37	37	57	57	H10	H10	I	ST	
IOCG3	36	36	56	56	J11	J11	I	ST	
IOCG6	4	4	10	10	E3	E3	I	ST	
IOCG7	5	5	11	11	F4	F4	I	ST	
IOCG8	6	6	12	12	F2	F2	I	ST	
IOCG9	8	8	14	14	F3	F3	I	ST	
IOCG12	—	—	96	96	C3	C3	I	ST	
IOCG13	—	—	97	97	A3	A3	I	ST	
IOCG14	—	—	95	95	C4	C4	I	ST	
IOCG15	—	—	1	1	B2	B2	I	ST	
HLVDIN	64	64	100	100	A1	A1	I	ANA	High/Low-Voltage Detect Input
$\overline{\text{MCLR}}$	7	7	13	13	F1	F1	I	ST	Master Clear (device Reset) Input. This line is brought low to cause a Reset.
OC4	54	54	83	83	D7	D7	O	DIG	Output Compare Outputs
OC5	55	55	84	84	C7	C7	O	DIG	
OC6	58	58	87	87	B6	B6	O	DIG	
OCM1A	4	4	10	10	E3	E3	O	DIG	MCCP1 Outputs
OCM1B	5	5	11	11	F4	F4	O	DIG	
OCM1C	—	—	1	1	B2	B2	O	DIG	
OCM1D	—	—	6	6	D1	D1	O	DIG	
OCM1E	—	—	91	91	C5	C5	O	DIG	
OCM1F	—	—	92	92	B5	B5	O	DIG	

Legend: TTL = TTL input buffer; ST = Schmitt Trigger input buffer; ANA = Analog level input/output; I^2C = I^2C/SMBus input buffer; DIG = Digital input/output; XCVR = Dedicated Transceiver

FIGURE 4-2: RELATIONSHIP BETWEEN PARTITIONS 1/2 AND ACTIVE/INACTIVE PARTITIONS

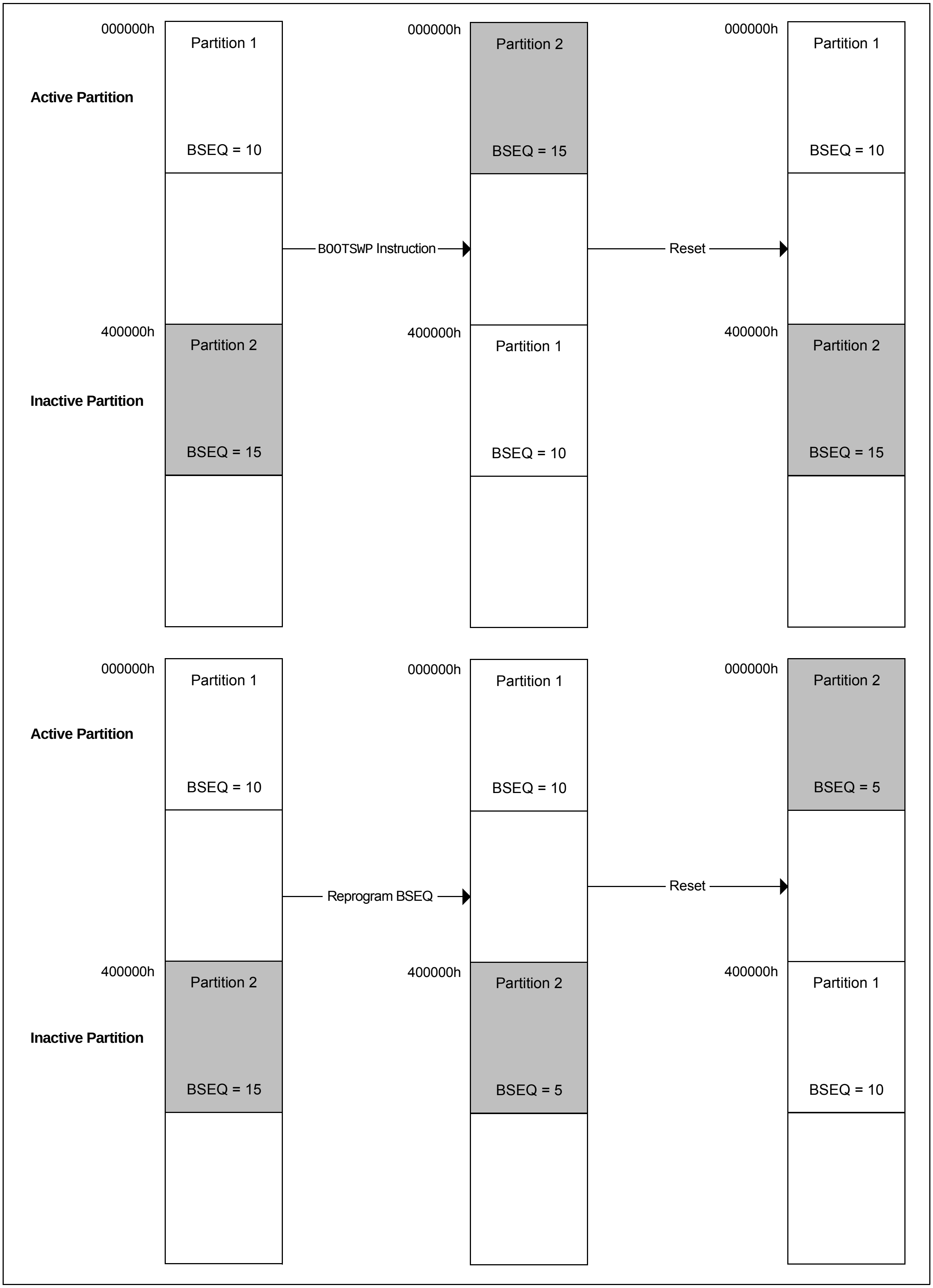


TABLE 4-2: CONFIGURATION WORD ADDRESSES

Configuration Register	Single Partition Mode			
	PIC24FJ1024GX6XX	PIC24FJ512GX6XX	PIC24FJ256GX6XX	PIC24FJ128GX6XX
FSEC	0ABF00h	055F00h	02AF00h	015F00h
FBSLIM	0ABF10h	055F10h	02AF10h	015F10h
FSIGN	0ABF14h	055F14h	02AF14h	015F14h
FOSCSEL	0ABF18h	055F18h	02AF18h	015F18h
FOSC	0ABF1Ch	055F1Ch	02AF1Ch	015F1Ch
FWDT	0ABF20h	055F20h	02AF20h	015F20h
FPOR	0ABF24h	055F24h	02AF24h	015F24h
FICD	0ABF28h	055F28h	02AF28h	015F28h
FDEVOPT1	0ABF2Ch	055F2Ch	02AF2Ch	015F2Ch
FBOOT	801800h			
	Dual Partition Modes(1)			
FSEC(2)	055F00h/455F00h	02AF00h/42AF00h	015700h/415700h	00AF00h/40AF00h
FBSLIM(2)	055F10h/455F10h	02AF10h/42AF10h	015710h/415710h	00AF10h/40AF10h
FSIGN(2)	055F14h/455F14h	02AF14h/42AF14h	015714h/415714h	00AF14h/40AF14h
FOSCSEL	055F18h/455F18h	02AF18h/42AF18h	015718h/415718h	00AF18h/40AF18h
FOSC	055F1Ch/455F1Ch	02AF1Ch/42AF1Ch	01571Ch/41571Ch	00AF1Ch/40AF1Ch
FWDT	055F20h/455F20h	02AF20h/42AF20h	015720h/415720h	00AF20h/40AF20h
FPOR	055F24h/455F24h	02AF24h/42AF24h	015724h/415724h	00AF24h/40AF24h
FICD	055F28h/455F28h	02AF28h/42AF28h	015728h/415728h	00AF28h/40AF28h
FDEVOPT1	055F2Ch/455F2Ch	02AF2Ch/42AF2Ch	01572Ch/41572Ch	00AF2Ch/40AF2Ch
FBTSEQ(3)	055FFCh/455FFCh	02AFFCh/42AFFCh	0157FCh/4157FCh	00AFFCh/40AFFCh
FBOOT	801800h			

Note 1: Addresses shown for Dual Partition modes are for the Active/Inactive Partitions, respectively.

2: Changes to these Inactive Partition Configuration Words affect how the Active Partition accesses the Inactive Partition.

3: FBTSEQ is a 24-bit Configuration Word, using all three bytes of the program memory width.

7.4.1 POR AND LONG OSCILLATOR START-UP TIMES

The oscillator start-up circuitry and its associated delay timers are not linked to the device Reset delays that occur at power-up. Some crystal circuits (especially low-frequency crystals) will have a relatively long start-up time. Therefore, one or more of the following conditions is possible after $\overline{\text{SYSRST}}$ is released:

- The oscillator circuit has not begun to oscillate.
- The Oscillator Start-up Timer has not expired (if a crystal oscillator is used).
- The PLL has not achieved a lock (if PLL is used).

The device will not begin to execute code until a valid clock source has been released to the system. Therefore, the oscillator and PLL start-up delays must be considered when the Reset delay time must be known.

7.4.2 FAIL-SAFE CLOCK MONITOR (FSCM) AND DEVICE RESETS

If the FSCM is enabled, it will begin to monitor the system clock source when $\overline{\text{SYSRST}}$ is released. If a valid clock source is not available at this time, the device will automatically switch to the FRC Oscillator and the user can switch to the desired crystal oscillator in the Trap Service Routine (TSR).

REGISTER 8-1: SR: ALU STATUS REGISTER(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	DC
bit 15							bit 8

R/W-0(3)	R/W-0(3)	R/W-0(3)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2(2)	IPL1(2)	IPL0(2)	RA	N	OV	Z	C
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’= Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits(2,3)

`111` = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
`110` = CPU Interrupt Priority Level is 6 (14)
`101` = CPU Interrupt Priority Level is 5 (13)
`100` = CPU Interrupt Priority Level is 4 (12)
`011` = CPU Interrupt Priority Level is 3 (11)
`010` = CPU Interrupt Priority Level is 2 (10)
`001` = CPU Interrupt Priority Level is 1 (9)
`000` = CPU Interrupt Priority Level is 0 (8)

Note 1: For complete register details, see Register 3-1.

2: The IPL<2:0> Status bits are concatenated with the IPL3 Status bit (CORCON<3>) to form the CPU Interrupt Priority Level (IPL). The value in parentheses indicates the IPL when IPL3 = `1`. User interrupts are disabled when IPL3 = `1`.

3: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = `1`.

9.1 CPU Clocking Scheme

The system clock source can be provided by one of five sources:

- Primary Oscillator (POSC) on the OSCI and OSCO pins
- Secondary Oscillator (SOSC) on the SOSCI and SOSCO pins
- Digitally Controlled Oscillator (DCO)
- Fast Internal RC (FRC) Oscillator
- Low-Power Internal RC (LPRC) Oscillator

The Primary Oscillator and FRC sources have the option of using the internal PLL block, which can generate a 96 MHz USB module PLL clock, or a 4x, 6x or 8x PLL clock. If the 96 MHz PLL is used, the PLL clocks can then be postscaled, if necessary, and used as the system clock. If the 4x, 6x or 8x PLL multipliers are selected, the PLL clock can be used directly as a system clock. Refer to **Section 9.6 "PLL Oscillator Modes and USB Operation"** for additional information. The internal FRC provides an 8 MHz clock source.

Each clock source (POSC, SOSC, DCO, FRC and LPRC) can be used as an input to an additional divider, which can then be used to produce a divided clock source for use as a system clock (OSCFDIV).

The selected clock source is used to generate the processor and peripheral clock sources. The processor clock source is divided by two to produce the internal instruction cycle clock, FCY. In this document, the instruction cycle clock is also denoted by FOSC/2. The internal instruction cycle clock, FOSC/2, can be provided on the OSCO I/O pin for some Primary Oscillator configurations.

9.2 Initial Configuration on POR

The oscillator source (and operating mode) that is used at a device Power-on Reset event is selected using Configuration bit settings. The Oscillator Configuration bit settings are located in the Configuration registers in the program memory (refer to **Section 30.1 "Configuration Bits"** for further details). The Primary Oscillator Configuration bits, POSCMD<1:0> (FOSC<1:0>), and the Initial Oscillator Select Configuration bits, FNOSC<2:0> (FOSCSEL<2:0>), select the oscillator source that is used at a Power-on Reset. The OSCFDIV clock source is the default (unprogrammed) selection; the default input source to the OSCFDIV divider is the FRC clock source. Other oscillators may be chosen by programming these bit locations.

The Configuration bits allow users to choose between the various clock modes shown in Table 9-1.

9.2.1 CLOCK SWITCHING MODE CONFIGURATION BITS

The FCKSM<1:0> Configuration bits (FOSC<7:6>) are used to jointly configure device clock switching and the Fail-Safe Clock Monitor (FSCM). Clock switching is enabled only when FCKSM<1> is programmed ('0'). The FSCM is enabled only when FCKSM<1:0> are both programmed ('00').

REGISTER 11-44: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP17R5	RP17R4	RP17R3	RP17R2	RP17R1	RP17R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP16R5	RP16R4	RP16R3	RP16R2	RP16R1	RP16R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP17R<5:0>:** RP17 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP17 (see Table 11-4 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP16R<5:0>:** RP16 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP16 (see Table 11-4 for peripheral function numbers).

REGISTER 11-45: RPOR9: PERIPHERAL PIN SELECT OUTPUT REGISTER 9

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP19R5	RP19R4	RP19R3	RP19R2	RP19R1	RP19R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP18R5	RP18R4	RP18R3	RP18R2	RP18R1	RP18R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP19R<5:0>:** RP19 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP19 (see Table 11-4 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP18R<5:0>:** RP18 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP18 (see Table 11-4 for peripheral function numbers).

15.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the OCxRS and OCxR registers. The OCxRS and OCxR registers can be written to at any time, but the duty cycle value is not latched until a match between PRy and TMRy occurs (i.e., the period is complete). This provides a double buffer for the PWM duty cycle and is essential for glitchless PWM operation.

Some important boundary parameters of the PWM duty cycle include:

- If OCxR, OCxRS and PRy are all loaded with 0000h, the OCx pin will remain low (0% duty cycle).
- If OCxRS is greater than PRy, the pin will remain high (100% duty cycle).

See Example 15-1 for PWM mode timing details. Table 15-1 and Table 15-2 show example PWM frequencies and resolutions for a device operating at 4 MIPS and 10 MIPS, respectively.

EQUATION 15-2: CALCULATION FOR MAXIMUM PWM RESOLUTION(1)

$$\text{Maximum PWM Resolution (bits)} = \frac{\log_{10}\left(\dfrac{F_{CY}}{F_{PWM} \cdot (\text{Timer Prescale Value})}\right)}{\log_{10}(2)} \text{ bits}$$

Note 1: Based on $F_{CY} = F_{OSC}/2$; Doze mode and PLL are disabled.

EXAMPLE 15-1: PWM PERIOD AND DUTY CYCLE CALCULATIONS(1)

1. Find the Timer Period register value for a desired PWM frequency of 52.08 kHz, where F_{OSC} = 32 MHz with PLL (32 MHz device clock rate) and a Timer2 prescaler setting of 1:1.

   $T_{CY} = 2 * T_{OSC} = 62.5$ ns

   PWM Period = 1/PWM Frequency = 1/52.08 kHz = 19.2 μs

   PWM Period = (PR2 + 1) • T_{CY} • (Timer2 Prescale Value)

   19.2 μs = (PR2 + 1) • 62.5 ns • 1

   PR2 = 306

2. Find the maximum resolution of the duty cycle that can be used with a 52.08 kHz frequency and a 32 MHz device clock rate:

   PWM Resolution = $\log_{10}(F_{CY}/F_{PWM})/\log_{10}2)$ bits

   = $(\log_{10}(16\text{ MHz}/52.08\text{ kHz})/\log_{10}2)$ bits

   = 8.3 bits

Note 1: Based on $T_{CY} = 2 * T_{OSC}$; Doze mode and PLL are disabled.

TABLE 15-1: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 4 MIPS (F_{CY} = 4 MHz)(1)

PWM Frequency	7.6 Hz	61 Hz	122 Hz	977 Hz	3.9 kHz	31.3 kHz	125 kHz
Timer Prescaler Ratio	8	1	1	1	1	1	1
Period Register Value	FFFFh	FFFFh	7FFFh	0FFFh	03FFh	007Fh	001Fh
Resolution (bits)	16	16	15	12	10	7	5

Note 1: Based on $F_{CY} = F_{OSC}/2$; Doze mode and PLL are disabled.

TABLE 15-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 16 MIPS (F_{CY} = 16 MHz)(1)

PWM Frequency	30.5 Hz	244 Hz	488 Hz	3.9 kHz	15.6 kHz	125 kHz	500 kHz
Timer Prescaler Ratio	8	1	1	1	1	1	1
Period Register Value	FFFFh	FFFFh	7FFFh	0FFFh	03FFh	007Fh	001Fh
Resolution (bits)	16	16	15	12	10	7	5

Note 1: Based on $F_{CY} = F_{OSC}/2$; Doze mode and PLL are disabled.

REGISTER 18-2: I2CxCONH: I2Cx CONTROL REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PCIE	SCIE	BOEN	SDAHT(1)	SBCDE	AHEN	DHEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6 **PCIE:** Stop Condition Interrupt Enable bit (I^2C Slave mode only)
1 = Enables interrupt on detection of Stop condition
0 = Stop detection interrupts are disabled

bit 5 **SCIE:** Start Condition Interrupt Enable bit (I^2C Slave mode only)
1 = Enables interrupt on detection of Start or Restart conditions
0 = Start detection interrupts are disabled

bit 4 **BOEN:** Buffer Overwrite Enable bit (I^2C Slave mode only)
1 = I2CxRCV is updated and an ACK is generated for a received address/data byte, ignoring the state of the I2COV bit only if RBF bit = 0
0 = I2CxRCV is only updated when I2COV is clear

bit 3 **SDAHT:** SDAx Hold Time Selection bit(1)
1 = Minimum of 300 ns hold time on SDAx after the falling edge of SCLx
0 = Minimum of 100 ns hold time on SDAx after the falling edge of SCLx

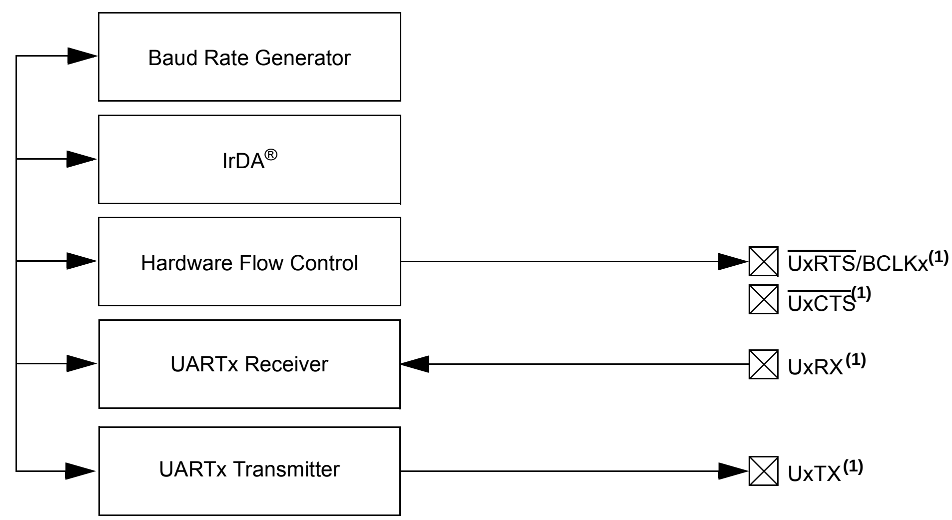
bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I^2C Slave mode only)
If, on the rising edge of SCLx, SDAx is sampled low when the module is outputting a high state, the BCL bit is set and the bus goes Idle. This Detection mode is only valid during data and ACK transmit sequences.
1 = Enables slave bus collision interrupts
0 = Slave bus collision interrupts are disabled

bit 1 **AHEN:** Address Hold Enable bit (I^2C Slave mode only)
1 = Following the 8th falling edge of SCLx for a matching received address byte; SCLREL bit (I2CxCONL<12>) will be cleared and SCLx will be held low
0 = Address holding is disabled

bit 0 **DHEN:** Data Hold Enable bit (I^2C Slave mode only)
1 = Following the 8th falling edge of SCLx for a received data byte; slave hardware clears the SCLREL bit (I2CxCONL<12>) and SCLx is held low
0 = Data holding is disabled

Note 1: This bit must be set to ‘0’ for 1 MHz operation.

FIGURE 19-1: UARTx SIMPLIFIED BLOCK DIAGRAM



Note 1: The UART1, UART2, UART3 and UART4 inputs and outputs must all be assigned to available RPn/RPIn pins before use. See **Section 11.4 "Peripheral Pin Select (PPS)"** for more information.

REGISTER 20-7: U1CON: USB CONTROL REGISTER (DEVICE MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R-x, HSC	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SE0	PKTDIS	—	HOSTEN	RESUME	PPBRST	USBEN
bit 7							bit 0

Legend:	U = Unimplemented bit, read as ‘0’		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6 **SE0:** Live Single-Ended Zero Flag bit
1 = Single-ended zero is active on the USB bus
0 = No single-ended zero is detected

bit 5 **PKTDIS:** Packet Transfer Disable bit
1 = SIE token and packet processing are disabled; automatically set when a SETUP token is received
0 = SIE token and packet processing are enabled

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **HOSTEN:** Host Mode Enable bit
1 = USB host capability is enabled; pull-downs on D+ and D- are activated in hardware
0 = USB host capability is disabled

bit 2 **RESUME:** Resume Signaling Enable bit
1 = Resume signaling is activated
0 = Resume signaling is disabled

bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
1 = Resets all Ping-Pong Buffer Pointers to the even BD banks
0 = Ping-Pong Buffer Pointers are not reset

bit 0 **USBEN:** USB Module Enable bit
1 = USB module and supporting circuitry are enabled (device attached); D+ pull-up is activated in hardware
0 = USB module and supporting circuitry are disabled (device detached)

22.3 Registers

22.3.1 RTCC CONTROL REGISTERS

REGISTER 22-1: RTCCON1L: RTCC CONTROL REGISTER 1 (LOW)

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
RTCEN	—	—	—	WRLOCK	PWCEN	PWCPOL	PWCPOE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
RTCOE	OUTSEL2	OUTSEL1	OUTSEL0	—	—	—	TSAEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **RTCEN:** RTCC Enable bit
1 = RTCC is enabled and counts from selected clock source
0 = RTCC is not enabled

bit 14-12 **Unimplemented:** Read as ‘0’

bit 11 **WRLOCK:** RTCC Register Write Lock
1 = RTCC registers are locked
0 = RTCC registers may be written to by user

bit 10 **PWCEN:** Power Control Enable bit
1 = Power control is enabled
0 = Power control is disabled

bit 9 **PWCPOL:** Power Control Polarity bit
1 = Power control output is active-high
0 = Power control output is active-low

bit 8 **PWCPOE:** Power Control Output Enable bit
1 = Power control output pin is enabled
0 = Power control output pin is disabled

bit 7 **RTCOE:** RTCC Output Enable bit
1 = RTCC output is enabled
0 = RTCC output is disabled

bit 6-4 **OUTSEL<2:0>:** RTCC Output Signal Selection bits
111 = Unused
110 = Unused
101 = Unused
100 = Timestamp A event
011 = Power control
010 = RTCC input clock
001 = Second clock
000 = Alarm event

bit 3-1 **Unimplemented:** Read as ‘0’

bit 0 **TSAEN:** Timestamp A Enable bit
1 = Timestamp event will occur when a low pulse is detected on the $\overline{\text{TMPR}}$ pin
0 = Timestamp is disabled

REGISTER 22-18: TSADATEH: RTCC TIMESTAMP A DATE REGISTER (HIGH)[1]

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	MTHTEN	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12	**YRTEN<3:0>:** Binary Coded Decimal Value of Years ‘10’ Digit bits
bit 11-8	**YRONE<3:0>:** Binary Coded Decimal Value of Years ‘1’ Digit bits
bit 7-5	**Unimplemented:** Read as ‘0’
bit 4	**MTHTEN:** Binary Coded Decimal Value of Months ‘10’ Digit bit Contains a value from 0 to 1.
bit 3-0	**MTHONE<2:0>:** Binary Coded Decimal Value of Months ‘1’ Digit bits Contains a value from 0 to 9.

Note 1: If TSAEN = 0, bits<15:0> can be used for persistence storage throughout a non-Power-on Reset ($\overline{\text{MCLR}}$, WDT, etc.).

REGISTER 24-3: CLCxSEL: CLCx INPUT MUX SELECT REGISTER

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	DS4<2:0>			—	DS3<2:0>		
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	DS2<2:0>			—	DS1<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **DS4<2:0>:** Data Selection MUX 4 Signal Selection bits
111 = MCCP3 Compare Event Interrupt Flag (CCP3IF)
110 = MCCP1 Compare Event Interrupt Flag (CCP1IF)
101 = Unimplemented
100 = CTMU A/D Trigger
011 = SPIx Input (SDIx) corresponding to the CLCx module (see Table 24-1)
010 = Comparator 3 output
001 = Module-specific CLCx output (see Table 24-1)
000 = CLCINB I/O pin

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **DS3<2:0>:** Data Selection MUX 3 Signal Selection bits
111 = MCCP3 Compare Event Interrupt Flag (CCP3IF)
110 = MCCP2 Compare Event Interrupt Flag (CCP2IF)
101 = DMA Channel 1 interrupt
100 = UARTx RX output corresponding to the CLCx module (see Table 24-1)
011 = SPIx Output (SDOx) corresponding to the CLCx module (see Table 24-1)
010 = Comparator 2 output
001 = CLCx output (see Table 24-1)
000 = CLCINA I/O pin

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **DS2<2:0>:** Data Selection MUX 2 Signal Selection bits
111 = MCCP2 Compare Event Interrupt Flag (CCP2IF)
110 = MCCP1 Compare Event Interrupt Flag (CCP1IF)
101 = DMA Channel 0 interrupt
100 = A/D conversion done interrupt
011 = UARTx TX input corresponding to the CLCx module (see Table 24-1)
010 = Comparator 1 output
001 = CLCx output (see Table 24-1)
000 = CLCINB I/O pin

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **DS1<2:0>:** Data Selection MUX 1 Signal Selection bits
111 = Timer3 match event
110 = Timer2 match event
101 = Unimplemented
100 = REFO output
011 = INTRC/LPRC clock source
010 = SOSC clock source
001 = System clock (TCY)
000 = CLCINA I/O pin

25.4 Achieving Maximum A/D Converter (ADC) Performance

In order to get the shortest overall conversion time (called the “throughput”) while maintaining accuracy, several factors must be considered. These are described in detail below.

- Dependence of AV_{DD} – If the AV_{DD} supply is < 2.7V, the Charge Pump Enable bit (PUMPEN, AD1CON3<13>) should be set to ‘1’. The input channel multiplexer has a varying resistance with AV_{DD} (the lower AV_{DD}, the higher the internal switch resistance). The charge pump provides a higher internal AV_{DD} to keep the switch resistance as low as possible.
- Dependence on T_{AD} – The ADC timing is driven by T_{AD}, not T_{CYC}. Selecting the T_{AD} time correctly is critical to getting the best ADC throughput. It is important to note that the overall ADC throughput is not simply the ‘Conversion Time’ of the SAR; it is the combination of the Conversion Time, the Sample Time and additional T_{AD} delays for internal synchronization logic.
- Relationship between T_{CYC} and T_{AD} – There is not a fixed 1:1 timing relationship between T_{CYC} and T_{AD}. The fastest possible throughput is fundamentally set by T_{AD} (min), not by T_{CYC}. The T_{AD} time is set as a programmable integer multiple of T_{CYC} by the ADCS<7:0> bits. Referring to Table 33-26, the T_{AD} (min) time is greater than the 4 MHz period of the dedicated ADC RC clock generator. Therefore, T_{AD} must be 2 T_{CYC} in order to use the RC clock for fastest throughput. The T_{AD} (min) is a multiple of 3.597 MHz as opposed to 4 MHz. To run as fast as possible, T_{CYC} must be a multiple of T_{AD} (min) because values of ADCSx are integers. For example, if a standard “color burst” crystal of 14.31818 MHz is used, T_{CYC} is 279.4 ns, which is very close to T_{AD} (min) and the ADC throughput is optimal. Running at 16 MHz will actually reduce the throughput, because T_{AD} will have to be 500 ns as the T_{CYC} of 250 ns violates T_{AD} (min).
- Dependence on driving Source Resistance (R_S) – Certain transducers have high output impedance (> 2.5 kΩ). Having a high R_S will require longer sampling time to charge the S/H capacitor through the resistance path (see Figure 25-3). The worst case scenario is a full-range voltage step of AV_{SS} to AV_{DD}, with the sampling cap at AV_{SS}. The capacitor time constant is (R_S + R_{IC} + R_{SS}) (C_{HOLD}) and the sample time needs to be 6 time constants minimum (8 preferred). Since the ADC logic timing is T_{AD}-based, the sample time (in T_{AD}) must be long enough, over all conditions, to charge/discharge C_{HOLD}. Do not assume one T_{AD} is sufficient sample time; longer times may be required to achieve the accuracy needed by the application. The value of C_{HOLD} is 40 pF.

A small amount of charge is present at the ADC input pin when the sample switch is closed. If R_S is high, this will generate a DC error exceeding 1 LSB. Keeping R_S < 50Ω is recommenced for best results. The error can also be reduced by increasing sample time (a 2 kΩ value of R_S requires a 3 µS sample time to eliminate the error).

- Calculating Throughput – The throughput of the ADC is based on T_{AD}. The throughput is given by:

$$Throughput = \left(\frac{1}{Sample\ Time + SAR\ Conversion\ Time + Clock\ Sync\ Time}\right)$$

where:

Sample Time is the calculated T_{AD} periods for the application.

SAR Conversion Time is 12 T_{AD} for 10-bit and 14 T_{AD} for 12-bit conversions.

Clock Sync Time is 2.5 T_{AD} (worst case scenario).

For example, using an 8 MHz FRC means the T_{CYC} = 250 ns. This requires: T_{AD} = 2 T_{CYC} = 500 ns. Therefore, the throughput is:

$$Throughput = \left(\frac{1}{500\ ns + 14 \bullet 500\ ns + 2.5 \bullet 500\ ns}\right) = 114.28\ KS/sec$$

Note that the clock sync delay could be as little as 1.5 T_{AD}, which could produce 121 KS/sec, but that cannot be ensured as the timing relationship is asynchronous and not specified. The worst case timing of 2.5 T_{AD} should be used to calculate throughput.

For example, if a certain transducer has a 20 kΩ output impedance, the maximum sample time is determined by:

$$\begin{aligned} Sample\ Time &= 6 \bullet (R_S + R_{IC} + R_{SS}) \bullet C_{HOLD} \\ &= 6 \bullet (20K + 250 + 350) \bullet 40\ pF \\ &= 4.95\ \mu S \end{aligned}$$

If T_{AD} = 500 ns, this requires a Sample Time of 4.95 us/ 500 ns = 10 T_{AD} (for a full-step voltage on the transducer output).

REGISTER 25-5: AD1CON5: A/D CONTROL REGISTER 5

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
ASEN	LPEN	CTMREQ	BGREQ	—	—	ASINT1	ASINT0
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	WM1	WM0	CM1	CM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **ASEN:** Auto-Scan Enable bit
1 = Auto-scan is enabled
0 = Auto-scan is disabled

bit 14 **LPEN:** Low-Power Enable bit
1 = Low power is enabled after scan
0 = Full power is enabled after scan

bit 13 **CTMREQ:** CTMU Request bit
1 = CTMU is enabled when the A/D is enabled and active
0 = CTMU is not enabled by the A/D

bit 12 **BGREQ:** Band Gap Request bit
1 = Band gap is enabled when the A/D is enabled and active
0 = Band gap is not enabled by the A/D

bit 11-10 **Unimplemented:** Read as ‘0’

bit 9-8 **ASINT<1:0>:** Auto-Scan (Threshold Detect) Interrupt Mode bits
11 = Interrupt after Threshold Detect sequence has completed and valid compare has occurred
10 = Interrupt after valid compare has occurred
01 = Interrupt after Threshold Detect sequence has completed
00 = No interrupt

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-2 **WM<1:0>:** Write Mode bits
11 = Reserved
10 = Auto-compare only (conversion results are not saved, but interrupts are generated when a valid match occurs, as defined by the CMx and ASINTx bits)
01 = Convert and save (conversion results are saved to locations as determined by the register bits when a match occurs, as defined by the CMx bits)
00 = Legacy operation (conversion data is saved to a location determined by the Buffer register bits)

bit 1-0 **CM<1:0>:** Compare Mode bits
11 = Outside Window mode: Valid match occurs if the conversion result is outside of the window defined by the corresponding buffer pair
10 = Inside Window mode: Valid match occurs if the conversion result is inside the window defined by the corresponding buffer pair
01 = Greater Than mode: Valid match occurs if the result is greater than the value in the corresponding Buffer register
00 = Less Than mode: Valid match occurs if the result is less than the value in the corresponding Buffer register

28.4 Measuring Die Temperature

The CTMU can be configured to use the A/D to measure the die temperature using dedicated A/D Channel 24. Perform the following steps to measure the diode voltage:

- The internal current source must be set for either 5.5 μA (IRNG<1:0> = 0x2) or 55 μA (IRNG<1:0> = 0x3).
- In order to route the current source to the diode, the EDG1STAT and EDG2STAT bits must be equal (either both '0' or both '1').
- The CTMREQ bit (AD1CON5<13>) must be set to '1'.
- The A/D Channel Select bits must be 24 (0x18) using a single-ended measurement.

The voltage of the diode will vary over temperature according to the graphs shown below (Figure 28-4). Note that the graphs are different, based on the magnitude of the current source selected. The slopes are nearly linear over the range of -40ºC to +100ºC and the temperature can be calculated as follows:

EQUATION 28-2:

For 5.5 μA Current Source:

$$Tdie = \frac{710\ mV - Vdiode}{1.8}$$

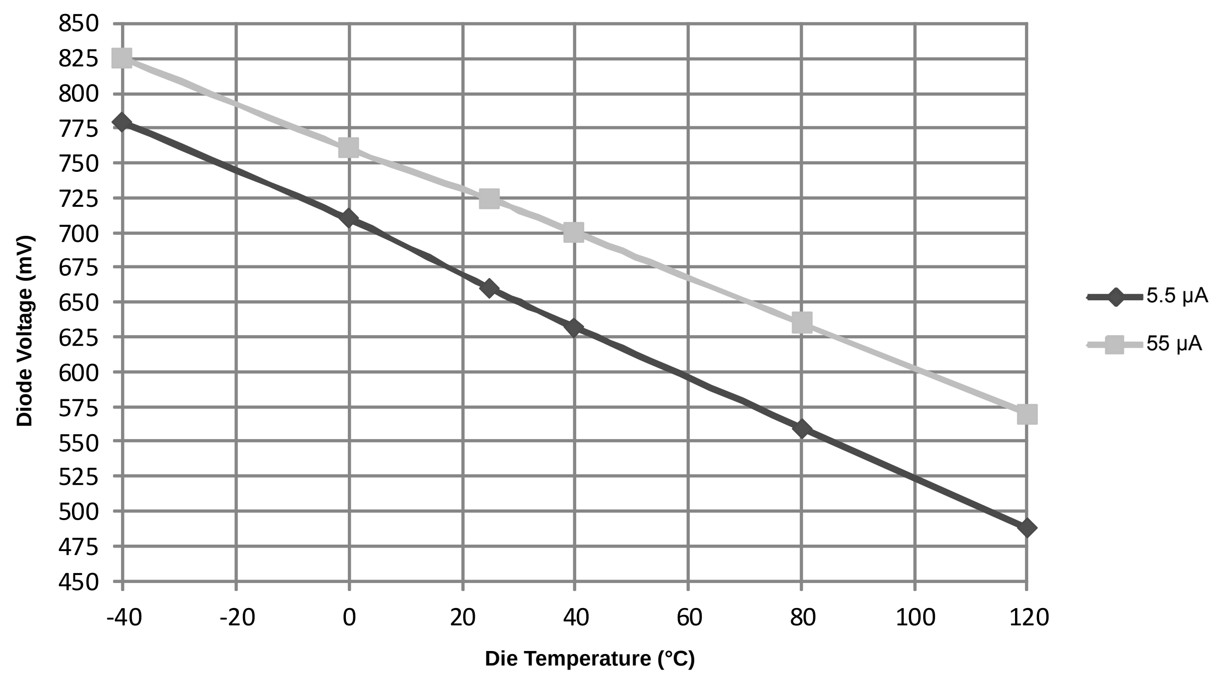
where $Vdiode$ is in mV, $Tdie$ is in ºC

For 55 μA Current Source:

$$Tdie = \frac{760\ mV - Vdiode}{1.55}$$

where $Vdiode$ is in mV, $Tdie$ is in ºC

FIGURE 28-4: DIODE VOLTAGE (mV) vs. DIE TEMPERATURE (TYPICAL)



30.5 Program Verification and Code Protection

PIC24FJ1024GA610/GB610 family devices offer basic implementation of CodeGuard™ Security that supports General Segment (GS) security and Boot Segment (BS) security. This feature helps protect individual Intellectual Property.

Note:	For more information on usage, configuration and operation, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"CodeGuard™ Intermediate Security"** (DS70005182).

30.6 JTAG Interface

PIC24FJ1024GA610/GB610 family devices implement a JTAG interface, which supports boundary scan device testing.

30.7 In-Circuit Serial Programming

PIC24FJ1024GA610/GB610 family microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock (PGECx) and data (PGEDx), and three other lines for power (VDD), ground (VSS) and $\overline{\text{MCLR}}$. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

30.8 Customer OTP Memory

PIC24FJ1024GA610/GB610 family devices provide 256 bytes of One-Time-Programmable (OTP) memory, located at addresses, 801700h through 8017FEh. This memory can be used for persistent storage of application-specific information that will not be erased by reprogramming the device. This includes many types of information, such as (but not limited to):

- Application checksums
- Code revision information
- Product information
- Serial numbers
- System manufacturing dates
- Manufacturing lot numbers

OTP memory cannot be written by program execution (i.e., `TBLWT` instructions); it can only be written during device programming. Data is not cleared by a chip erase.

Note:	Data in the OTP memory section MUST NOT be programmed more than once.

30.9 In-Circuit Debugger

This function allows simple debugging functions when used with MPLAB IDE. Debugging functionality is controlled through the PGECx (Emulation/Debug Clock) and PGEDx (Emulation/Debug Data) pins.

To use the in-circuit debugger function of the device, the design must implement ICSP™ connections to $\overline{\text{MCLR}}$, VDD, VSS and the PGECx/PGEDx pin pair, designated by the ICS<1:0> Configuration bits. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins.

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