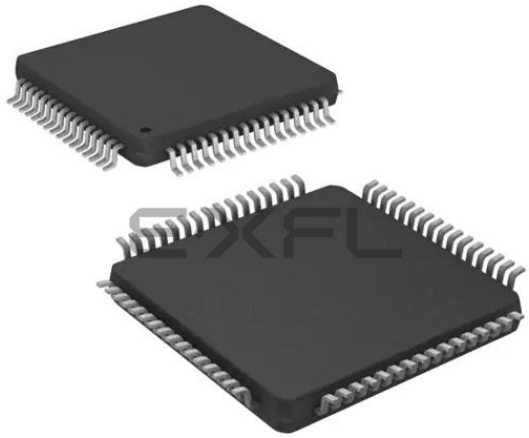

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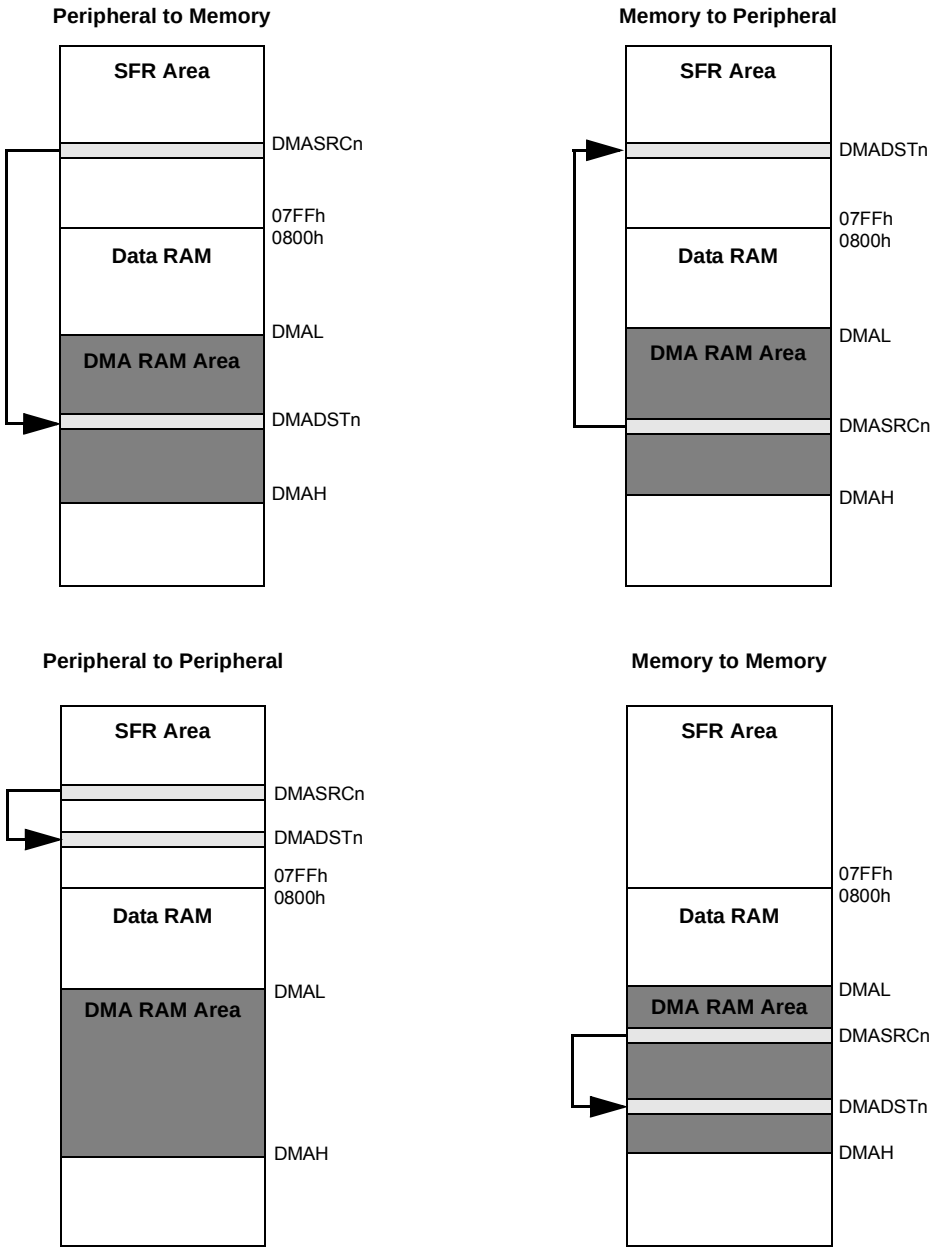
Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, HLVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj512ga606-i-pt

TABLE 4-7: SFR MAP: 0300h BLOCK (CONTINUED)

File Name	Address	All Resets	File Name	Address	All Resets
UART (CONTINUED)			**UART (CONTINUED)**		
U3STA	03C6	0110	U5BRG	03E4	0000
U3TXREG	03C8	xxxx	U5ADMD	03E6	0000
U3RXREG	03CA	0000	U6MODE	03E8	0000
U3BRG	03CC	0000	U6STA	03EA	0110
U3ADMD	03CE	0000	U6TXREG	03EC	xxxx
U4MODE	03D0	0000	U6RXREG	03EE	0000
U4STA	03D2	0110	U6BRG	03F0	0000
U4TXREG	03D4	xxxx	U6ADMD	03F2	0000
U4RXREG	03D6	0000	**SPI**		
U4BRG	03D8	0000	SPI1CON1	03F4	0x00
U4ADMD	03DA	0000	SPI1CON2	03F6	0000
U5MODE	03DC	0000	SPI1CON3	03F8	0000
U5STA	03DE	0110	SPI1STATL	03FC	0028
U5TXREG	03E0	xxxx	SPI1STATH	03FE	0000
U5RXREG	03E2	0000			

Legend: — = unimplemented, read as '0'; x = undefined. Reset values are shown in hexadecimal.

FIGURE 5-2: TYPES OF DMA DATA TRANSFERS



Note: Relative sizes of memory areas are not shown to scale.

7.0 RESETS

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Reset"** (DS39712), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

The Reset module combines all Reset sources and controls the device Master Reset Signal, $\overline{\text{SYSRST}}$. The following is a list of device Reset sources:

- POR: Power-on Reset
- $\overline{\text{MCLR}}$: Master Clear Pin Reset
- SWR: RESET Instruction
- WDT: Watchdog Timer Reset
- BOR: Brown-out Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Opcode Reset
- UWR: Uninitialized W Register Reset

A simplified block diagram of the Reset module is shown in Figure 7-1.

Any active source of Reset will make the $\overline{\text{SYSRST}}$ signal active. Many registers associated with the CPU and peripherals are forced to a known Reset state. Most registers are unaffected by a Reset; their status is unknown on POR and unchanged by all other Resets.

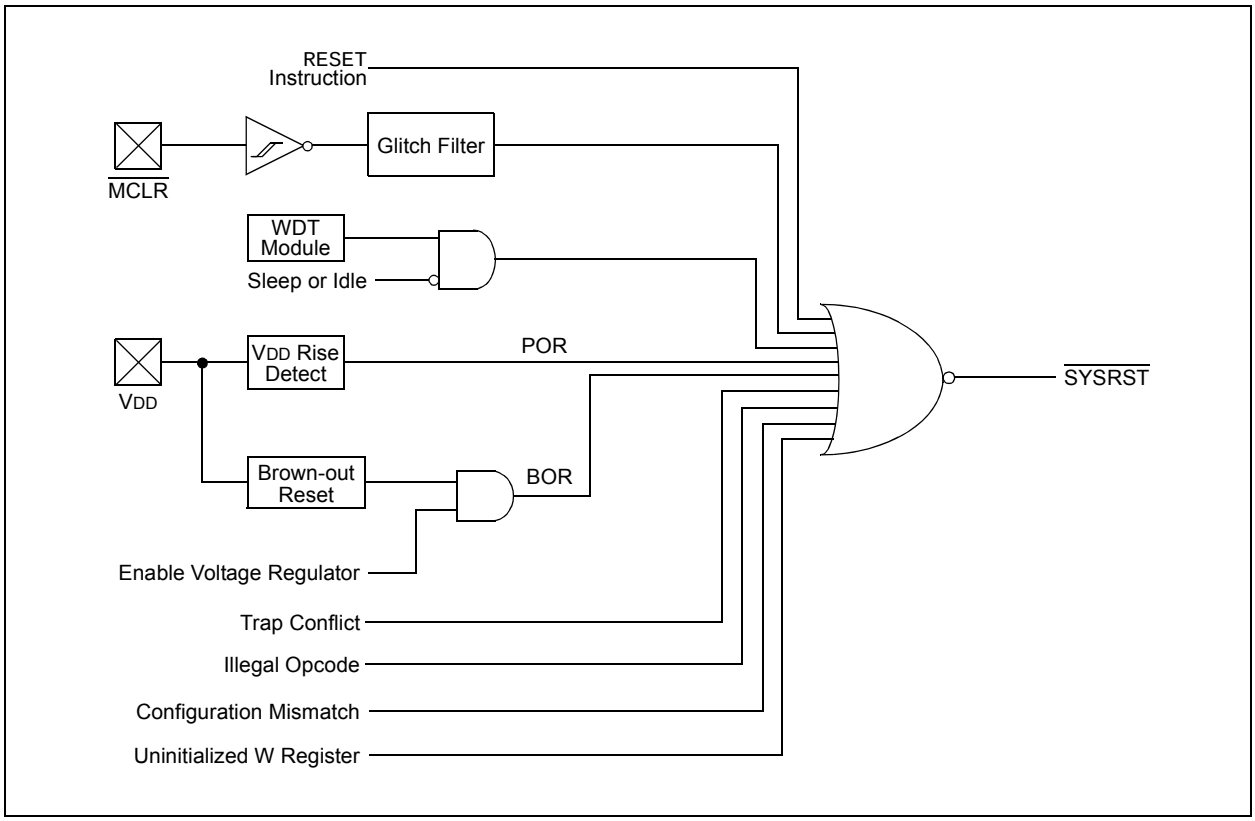
Note:	Refer to the specific peripheral or CPU section of this manual for register Reset states.

All types of device Reset will set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 7-1). A POR will clear all bits, except for the BOR and POR (RCON<1:0>) bits, which are set. The user may set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software will not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this data sheet.

Note:	The status bits in the RCON register should be cleared after they are read so that the next RCON register values after a device Reset will be meaningful.

FIGURE 7-1: RESET SYSTEM BLOCK DIAGRAM



REGISTER 7-1: RCON: RESET CONTROL REGISTER

R/W-0	R/W-0	R/W-1	R/W-0	U-0	U-0	R/W-0	R/W-0
TRAPR(1)	IOPUWR(1)	SBOREN	RETEN(2)	—	—	CM(1)	VREGS(3)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR(1)	SWR(1)	SWDTEN(4)	WDTO(1)	SLEEP(1)	IDLE(1)	BOR(1)	POR(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TRAPR:** Trap Reset Flag bit(1)
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit(1)
1 = An illegal opcode detection, an illegal address mode or Uninitialized W register is used as an Address Pointer and caused a Reset
0 = An illegal opcode or Uninitialized W register Reset has not occurred

bit 13 **SBOREN:** Software Enable/Disable of BOR bit
1 = BOR is turned on in software
0 = BOR is turned off in software

bit 12 **RETEN:** Retention Mode Enable bit(2)
1 = Retention mode is enabled while device is in Sleep modes (1.2V regulator enabled)
0 = Retention mode is disabled

bit 11-10 **Unimplemented:** Read as '0'

bit 9 **CM:** Configuration Word Mismatch Reset Flag bit(1)
1 = A Configuration Word Mismatch Reset has occurred
0 = A Configuration Word Mismatch Reset has not occurred

bit 8 **VREGS:** Fast Wake-up from Sleep bit(3)
1 = Fast wake-up is enabled (uses more power)
0 = Fast wake-up is disabled (uses less power)

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin bit(1)
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset (Instruction) Flag bit(1)
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed

Note 1: All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the $\overline{LPCFG}$ Configuration bit is '1' (unprogrammed), the retention regulator is disabled and the RETEN bit has no effect. Retention mode preserves the SRAM contents during Sleep.

3: Re-enabling the regulator after it enters Standby mode will add a delay, TVREG, when waking up from Sleep. Applications that do not use the voltage regulator should set this bit to prevent this delay from occurring.

4: If the FWDTEN<1:0> Configuration bits are '11' (unprogrammed), the WDT is always enabled**,** regardless of the SWDTEN bit setting.

REGISTER 8-3: INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
NSTDIS	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
—	—	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **NSTDIS:** Interrupt Nesting Disable bit
1 = Interrupt nesting is disabled
0 = Interrupt nesting is enabled

bit 14-5 **Unimplemented:** Read as ‘0’

bit 4 **MATHERR:** Math Error Status bit
1 = Math error trap has occurred
0 = Math error trap has not occurred

bit 3 **ADDRERR:** Address Error Trap Status bit
1 = Address error trap has occurred
0 = Address error trap has not occurred

bit 2 **STKERR:** Stack Error Trap Status bit
1 = Stack error trap has occurred
0 = Stack error trap has not occurred

bit 1 **OSCFAIL:** Oscillator Failure Trap Status bit
1 = Oscillator failure trap has occurred
0 = Oscillator failure trap has not occurred

bit 0 **Unimplemented:** Read as ‘0’

REGISTER 9-2: CLKDIV: CLOCK DIVIDER REGISTER

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
ROI	DOZE2	DOZE1	DOZE0	DOZEN(1)	RCDIV2	RCDIV1	RCDIV0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
CPDIV1	CPDIV0	PLLEN	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ROI:** Recover on Interrupt bit
1 = Interrupts clear the DOZEN bit and reset the CPU peripheral clock ratio to 1:1
0 = Interrupts have no effect on the DOZEN bit

bit 14-12 **DOZE<2:0>:** CPU Peripheral Clock Ratio Select bits
111 = 1:128
110 = 1:64
101 = 1:32
100 = 1:16
011 = 1:8 (default)
010 = 1:4
001 = 1:2
000 = 1:1

bit 11 **DOZEN:** Doze Enable bit(1)
1 = DOZE<2:0> bits specify the CPU peripheral clock ratio
0 = CPU peripheral clock ratio is set to 1:1

bit 10-8 **RCDIV<2:0>:** System Frequency Divider Clock Source Select bits
000 = Fast RC Oscillator (FRC)
001 = Fast RC Oscillator (FRC) with PLL module (FRCPLL)
010 = Primary Oscillator (XT, HS, EC)
011 = Primary Oscillator (XT, HS, EC) with PLL module (XTPLL, HSPLL, ECPLL)
100 = Secondary Oscillator (SOSC)
101 = Low-Power RC Oscillator (LPRC)
110 = Digitally Controlled Oscillator (DCO)
111 = Reserved; do not use

bit 7-6 **CPDIV<1:0>:** System Clock Select bits (postscaler select from 96 MHz PLL, 32 MHz clock branch)
11 = 4 MHz (divide-by-8)(2)
10 = 8 MHz (divide-by-4)(2)
01 = 16 MHz (divide-by-2)
00 = 32 MHz (divide-by-1)

bit 5 **PLLEN:** USB PLL Enable bit
1 = PLL is always active
0 = PLL is only active when a PLL Oscillator mode is selected (OSCCON<14:12> = 011 or 001)

bit 4-0 **Unimplemented:** Read as '0'

Note 1: This bit is automatically cleared when the ROI bit is set and an interrupt occurs.
2: This setting is not allowed while the USB module is enabled.

REGISTER 10-8: PMD8: PERIPHERAL MODULE DISABLE REGISTER 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
U6MD	U5MD	CLC4MD	CLC3MD	CLC2MD	CLC1MD	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **U6MD:** UART6 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 6 **U5MD:** UART5 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 5 **CLC4MD:** CLC4 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 4 **CLC3MD:** CLC3 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 3 **CLC2MD:** CLC2 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 2 **CLC1MD:** CLC1 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 1-0 **Unimplemented:** Read as '0'

REGISTER 16-6: CCPxCON3H: CCPx CONTROL 3 HIGH REGISTERS

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
OETRIG	OSCNT2	OSCNT1	OSCNT0	—	OUTM2(1)	OUTM1(1)	OUTM0(1)
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	POLACE	POLBDF(1)	PSSACE1	PSSACE0	PSSBDF1(1)	PSSBDF0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OETRIG:** CCPx Dead-Time Select bit
1 = For Triggered mode (TRIGEN = 1): Module does not drive enabled output pins until triggered
0 = Normal output pin operation

bit 14-12 **OSCNT<2:0>:** One-Shot Event Count bits
111 = Extends one-shot event by 7 time base periods (8 time base periods total)
110 = Extends one-shot event by 6 time base periods (7 time base periods total)
101 = Extends one-shot event by 5 time base periods (6 time base periods total)
100 = Extends one-shot event by 4 time base periods (5 time base periods total)
011 = Extends one-shot event by 3 time base periods (4 time base periods total)
010 = Extends one-shot event by 2 time base periods (3 time base periods total)
001 = Extends one-shot event by 1 time base period (2 time base periods total)
000 = Does not extend one-shot Trigger event

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **OUTM<2:0>:** PWMx Output Mode Control bits(1)
111 = Reserved
110 = Output Scan mode
101 = Brush DC Output mode, forward
100 = Brush DC Output mode, reverse
011 = Reserved
010 = Half-Bridge Output mode
001 = Push-Pull Output mode
000 = Steerable Single Output mode

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **POLACE:** CCPx Output Pins, OCMxA, OCMxC and OCMxE, Polarity Control bit
1 = Output pin polarity is active-low
0 = Output pin polarity is active-high

bit 4 **POLBDF:** CCPx Output Pins, OCMxB, OCMxD and OCMxF, Polarity Control bit(1)
1 = Output pin polarity is active-low
0 = Output pin polarity is active-high

bit 3-2 **PSSACE<1:0>:** PWMx Output Pins, OCMxA, OCMxC and OCMxE, Shutdown State Control bits
11 = Pins are driven active when a shutdown event occurs
10 = Pins are driven inactive when a shutdown event occurs
0x = Pins are tri-stated when a shutdown event occurs

bit 1-0 **PSSBDF<1:0>:** PWMx Output Pins, OCMxB, OCMxD, and OCMxF, Shutdown State Control bits(1)
11 = Pins are driven active when a shutdown event occurs
10 = Pins are driven inactive when a shutdown event occurs
0x = Pins are in a high-impedance state when a shutdown event occurs

Note 1: These bits are implemented in MCCPx modules only.

REGISTER 17-3: SPIxCON2L: SPIx CONTROL REGISTER 2 LOW

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	WLENGTH<4:0>(1,2)				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

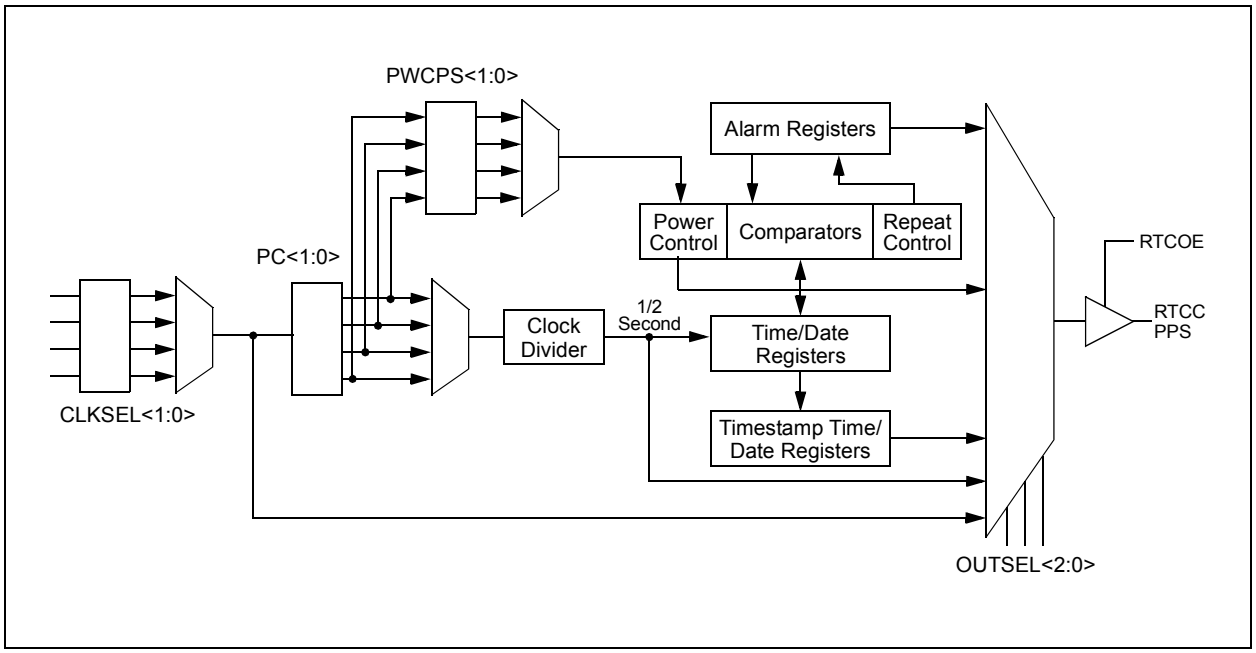
bit 4-0 **WLENGTH<4:0>:** Variable Word Length bits(1,2)

11111 = 32-bit data
11110 = 31-bit data
11101 = 30-bit data
11100 = 29-bit data
11011 = 28-bit data
11010 = 27-bit data
11001 = 26-bit data
11000 = 25-bit data
10111 = 24-bit data
10110 = 23-bit data
10101 = 22-bit data
10100 = 21-bit data
10011 = 20-bit data
10010 = 19-bit data
10001 = 18-bit data
10000 = 17-bit data
01111 = 16-bit data
01110 = 15-bit data
01101 = 14-bit data
01100 = 13-bit data
01011 = 12-bit data
01010 = 11-bit data
01001 = 10-bit data
01000 = 9-bit data
00111 = 8-bit data
00110 = 7-bit data
00101 = 6-bit data
00100 = 5-bit data
00011 = 4-bit data
00010 = 3-bit data
00001 = 2-bit data
00000 = See MODE<32,16> bits in SPIxCON1L<11:10>

Note 1: These bits are effective when AUDEN = 0 only.

2: Varying the length by changing these bits does not affect the depth of the TX/RX FIFO.

FIGURE 22-1: RTCC BLOCK DIAGRAM



23.0 32-BIT PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"32-Bit Programmable Cyclic Redundancy Check (CRC)"** (DS30009729), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

The 32-bit programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-Programmable CRC Polynomial Equation, up to 32 bits
- Programmable Shift Direction (little or big-endian)
- Independent Data and Polynomial Lengths
- Configurable Interrupt Output
- Data FIFO

Figure 23-1 displays a simplified block diagram of the CRC generator. A simple version of the CRC shift engine is displayed in Figure 23-2.

FIGURE 23-1: CRC BLOCK DIAGRAM

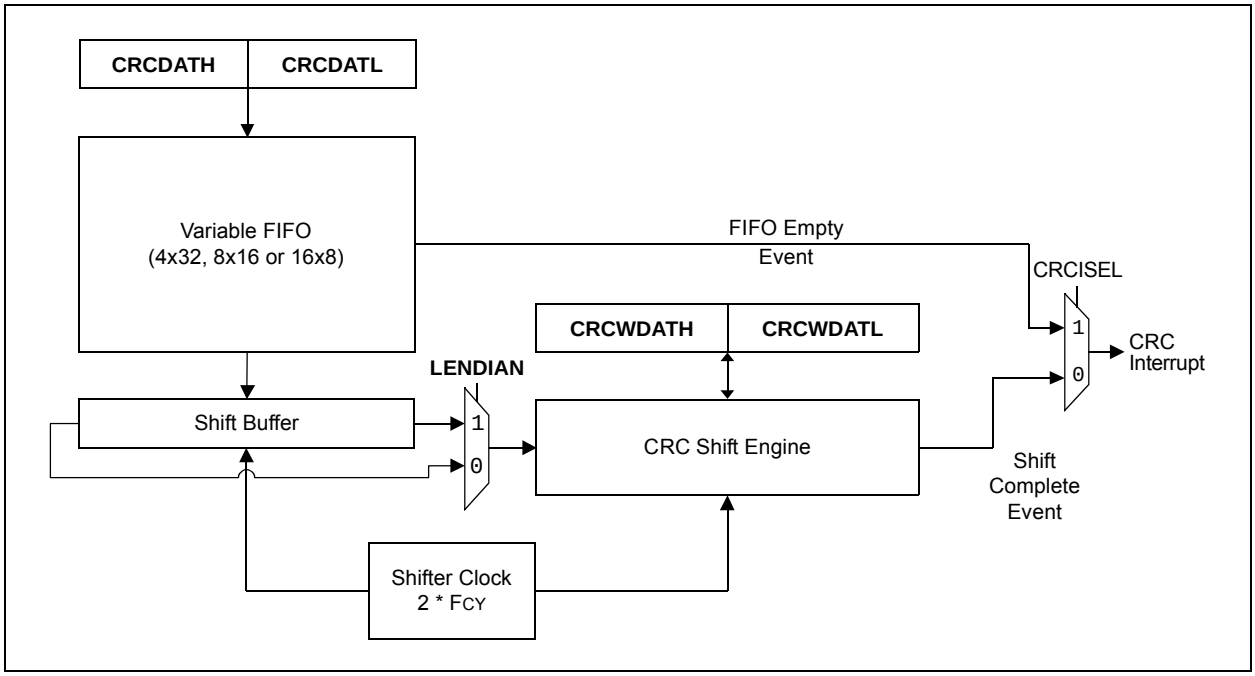
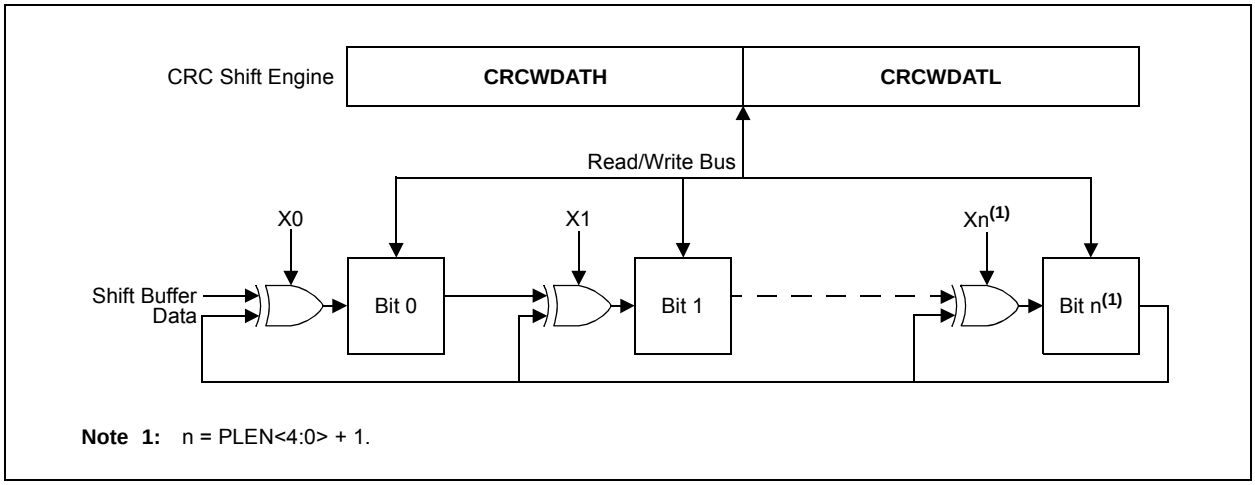


FIGURE 23-2: CRC SHIFT ENGINE DETAIL



Note 1: n = PLEN<4:0> + 1.

23.1 User Interface

23.1.1 POLYNOMIAL INTERFACE

The CRC module can be programmed for CRC polynomials of up to the 32nd order, using up to 32 bits.

Polynomial length, which reflects the highest exponent in the equation, is selected by the PLEN<4:0> bits (CRCCON2<4:0>).

The CRCXORL and CRCXORH registers control which exponent terms are included in the equation. Setting a particular bit includes that exponent term in the equation. Functionally, this includes an XOR operation on the corresponding bit in the CRC engine. Clearing the bit disables the XOR.

For example, consider two CRC polynomials, one a 16-bit and the other a 32-bit equation.

EQUATION 23-1: 16-BIT, 32-BIT CRC POLYNOMIALS

$$X16 + X12 + X5 + 1$$

and

$$X32+X26 + X23 + X22 + X16 + X12 + X11 + X10 + X8 + X7 + X5 + X4 + X2 + X + 1$$

To program these polynomials into the CRC generator, set the register bits, as shown in Table 23-1.

Note that the appropriate positions are set to '1' to indicate that they are used in the equation (for example, X26 and X23). The '0' bit required by the equation is always XORed; thus, X0 is a don't care. For a polynomial of length 32, it is assumed that the 32nd bit will be used. Therefore, the X<31:1> bits do not have the 32nd bit.

23.1.2 DATA INTERFACE

The module incorporates a FIFO that works with a variable data width. Input data width can be configured to any value between 1 and 32 bits using the DWIDTH<4:0> bits (CRCCON2<12:8>). When the data width is greater than 15, the FIFO is 4 words deep. When the DWIDTHx bits are between 15 and 8, the FIFO is 8 words deep. When the DWIDTHx bits are less than 8, the FIFO is 16 words deep.

The data for which the CRC is to be calculated must first be written into the FIFO. Even if the data width is less than 8, the smallest data element that can be written into the FIFO is 1 byte. For example, if the DWIDTHx bits are 5, then the size of the data is DWIDTH<4:0> + 1 or 6. The data is written as a whole byte; the two unused upper bits are ignored by the module.

Once data is written into the MSb of the CRCDAT registers (that is, the MSb as defined by the data width), the value of the VWORD<4:0> bits (CRCCON1<12:8>) increments by one. For example, if the DWIDTHx bits are 24, the VWORDx bits will increment when bit 7 of CRCDATH is written. Therefore, CRCDATL must always be written to before CRCDATH.

The CRC engine starts shifting data when the CRCGO bit (CRCCON1<4>) is set and the value of the VWORDx bits is greater than zero.

Each word is copied out of the FIFO into a buffer register, which decrements the VWORDx bits. The data is then shifted out of the buffer. The CRC engine continues shifting at a rate of two bits per instruction cycle, until the VWORDx bits reach zero. This means that for a given data width, it takes half that number of instructions for each word to complete the calculation. For example, it takes 16 cycles to calculate the CRC for a single word of 32-bit data.

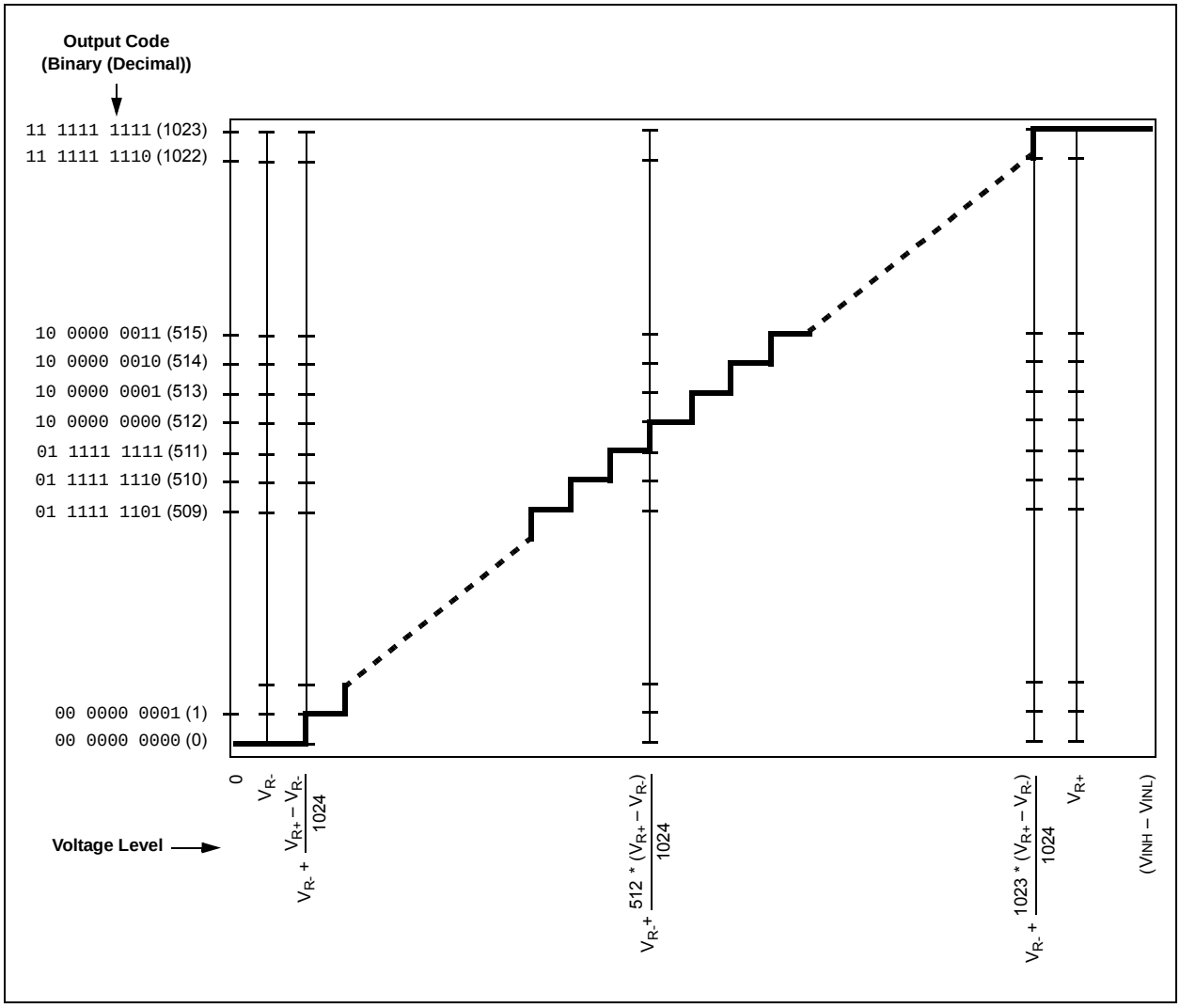
When the VWORDx bits reach the maximum value for the configured value of the DWIDTHx bits (4, 8 or 16), the CRCFUL bit (CRCCON1<7>) becomes set. When the VWORDx bits reach zero, the CRCMPT bit (CRCCON1<6>) becomes set. The FIFO is emptied and the VWORD<4:0> bits are set to '00000' whenever CRCEN is '0'.

At least one instruction cycle must pass after a write to CRCWDAT before a read of the VWORDx bits is done.

TABLE 23-1: CRC SETUP EXAMPLES FOR 16 AND 32-BIT POLYNOMIALS

CRC Control Bits	Bit Values	
	16-Bit Polynomial	32-Bit Polynomial
PLEN<4:0>	01111	11111
X<31:16>	0000 0000 0000 0001	0000 0100 1100 0001
X<15:1>	0001 0000 0010 000	0001 1101 1011 011

FIGURE 25-5: 10-BIT A/D TRANSFER FUNCTION



REGISTER 30-3: FSEC CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

R/PO-1	U-1	U-1	U-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
AIVTDIS	—	—	—	CSS2	CSS1	CSS0	CWRP
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	U-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
GSS1	GSS0	GWRP	—	BSEN	BSS1	BSS0	BWRP
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 23-16 **Unimplemented:** Read as '1'

bit 15 **AIVTDIS:** Alternate Interrupt Vector Table Disable bit
1 = Disables AIVT; INTCON2<8> (AIVTEN) bit is not available
0 = Enables AIVT; INTCON2<8> (AIVTEN) bit is available

bit 14-12 **Unimplemented:** Read as '1'

bit 11-9 **CSS<2:0>:** Configuration Segment Code Protection Level bits
111 = No protection (other than CWRP)
110 = Standard security
10x = Enhanced security
0xx = High security

bit 8 **CWRP:** Configuration Segment Program Write Protection bit
1 = Configuration Segment is not write-protected
0 = Configuration Segment is write-protected

bit 7-6 **GSS<1:0>:** General Segment Code Protection Level bits
11 = No protection (other than GWRP)
10 = Standard security
0x = High security

bit 5 **GWRP:** General Segment Program Write Protection bit
1 = General Segment is not write-protected
0 = General Segment is write-protected

bit 4 **Unimplemented:** Read as '1'

bit 3 **BSEN:** Boot Segment Control bit
1 = No Boot Segment is enabled
0 = Boot Segment size is determined by BSLIM<12:0>

bit 2-1 **BSS<1:0>**: Boot Segment Code Protection Level bits
11 = No protection (other than BWRP)
10 = Standard security
0x = High security

bit 0 **BWRP:** Boot Segment Program Write Protection bit
1 = Boot Segment can be written
0 = Boot Segment is write-protected

REGISTER 30-8: FWDT CONFIGURATION REGISTER

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—	—
bit 23							bit 16

U-1	R/PO-1	R/PO-1	U-1	R/PO-1	U-1	R/PO-1	R/PO-1
—	WDTCLK1	WDTCLK0	—	WDTCMX	—	WDTWIN1	WDTWIN0
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
WINDIS	FWDTEN1	FWDTEN0	FWPSA	WDTPS3	WDTPS2	WDTPS1	WDTPS0
bit 7							bit 0

Legend:	PO = Program Once bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘1’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-15 **Unimplemented:** Read as ‘1’

bit 14-13 **WDTCLK<1:0>:** Watchdog Timer Clock Select bits (when WDTCMX = 1)
- 11 = Always uses LPRC
- 10 = Uses FRC when WINDIS = 0, system clock is not LPRC and device is not in Sleep; otherwise, uses LPRC
- 01 = Always uses SOSC
- 00 = Uses peripheral clock when system clock is not LPRC and device is not in Sleep; otherwise, uses LPRC

bit 12 **Unimplemented:** Read as ‘1’

bit 11 **WDTCMX:** WDT Clock MUX Control bit
- 1 = Enables WDT clock MUX; WDT clock is selected by WDTCLK<1:0>
- 0 = WDT clock is LPRC

bit 10 **Unimplemented:** Read as ‘1’

bit 9-8 **WDTWIN<1:0>:** Watchdog Timer Window Width bits
- 11 = WDT window is 25% of the WDT period
- 10 = WDT window is 37.5% of the WDT period
- 01 = WDT window is 50% of the WDT period
- 00 = WDT window is 75% of the WDT period

bit 7 **WINDIS:** Windowed Watchdog Timer Disable bit
- 1 = Windowed WDT is disabled
- 0 = Windowed WDT is enabled

bit 6-5 **FWDTEN<1:0>:** Watchdog Timer Enable bits
- 11 = WDT is enabled
- 10 = WDT is disabled (control is placed on the SWDTEN bit)
- 01 = WDT is enabled only while device is active and disabled in Sleep; SWDTEN bit is disabled
- 00 = WDT and SWDTEN are disabled

bit 4 **FWPSA:** Watchdog Timer Prescaler bit
- 1 = WDT prescaler ratio of 1:128
- 0 = WDT prescaler ratio of 1:32

REGISTER 30-8: FWDT CONFIGURATION REGISTER (CONTINUED)

bit 3-0 **WDTPS<3:0>:** Watchdog Timer Postscale Select bits

1111 = 1:32,768
1110 = 1:16,384
1101 = 1:8,192
1100 = 1:4,096
1011 = 1:2,048
1010 = 1:1,024
1001 = 1:512
1000 = 1:256
0111 = 1:128
0110 = 1:64
0101 = 1:32
0100 = 1:16
0011 = 1:8
0010 = 1:4
0001 = 1:2
0000 = 1:1

TABLE 33-4: DC CHARACTERISTICS: OPERATING CURRENT (I_{DD})

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Operating Temperature**	**VDD**	**Conditions**
Operating Current (I_{DD})(2)						
DC19	230	365	µA	-40°C to +85°C	2.0V	0.5 MIPS, FOSC = 1 MHz
	250	365	µA	-40°C to +85°C	3.3V	
DC20	430	640	µA	-40°C to +85°C	2.0V	1 MIPS, FOSC = 2 MHz
	440	640	µA	-40°C to +85°C	3.3V	
DC23	1.5	2.4	mA	-40°C to +85°C	2.0V	4 MIPS, FOSC = 8 MHz
	1.65	2.4	mA	-40°C to +85°C	3.3V	
DC24	6.1	7.7	mA	-40°C to +85°C	2.0V	16 MIPS, FOSC = 32 MHz
	6.3	7.7	mA	-40°C to +85°C	3.3V	
DC31	43	130	µA	-40°C to +85°C	2.0V	LPRC (15.5 KIPS), FOSC = 31 kHz
	46	130	µA	-40°C to +85°C	3.3V	
DC32	1.63	2.5	mA	-40°C to +85°C	2.0V	FRC (4 MIPS), FOSC = 8 MHz
	1.65	2.5	mA	-40°C to +85°C	3.3V	
DC33	1.9	3.0	mA	-40°C to +85°C	2.0V	DCO (4 MIPS), FOSC = 8 MHz
	2.0	3.0	mA	-40°C to +85°C	3.3V	

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Typical parameters are for design guidance only and are not tested.

2: The test conditions for all IDD measurements are as follows: OSC1 driven with external square wave from rail-to-rail. All I/O pins are configured as outputs driving low. $\overline{MCLR}$ = VDD; WDT and FSCM are disabled. CPU, program memory and data memory are operational. All peripheral modules are clocked but inactive (PMDx bits are all '1'). JTAG module is disabled.

TABLE 33-5: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	**Typical(1)**	**Max**	**Units**	**Operating Temperature**	**VDD**	**Conditions**
Idle Current (I_{IDLE})(2)						
DC40	95	215	µA	-40°C to +85°C	2.0V	1 MIPS, FOSC = 2 MHz
	105	225	µA	-40°C to +85°C	3.3V	
DC43	290	720	µA	-40°C to +85°C	2.0V	4 MIPS, FOSC = 8 MHz
	315	750	µA	-40°C to +85°C	3.3V	
DC47	1.05	2.7	mA	-40°C to +85°C	2.0V	16 MIPS, FOSC = 32 MHz
	1.16	2.8	mA	-40°C to +85°C	3.3V	
DC50	350	820	µA	-40°C to +85°C	2.0V	FRC (4 MIPS), FOSC = 8 MHz
	360	850	µA	-40°C to +85°C	3.3V	
DC51	26	110	µA	-40°C to +85°C	2.0V	LPRC (15.5 KIPS), FOSC = 31 kHz
	30	110	µA	-40°C to +85°C	3.3V	

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Base IIDLE current is measured with the core off, the clock on and all modules turned off. Peripheral Module Disable SFR registers are '1'. All I/O pins are configured as outputs driving low. JTAG module is disabled.

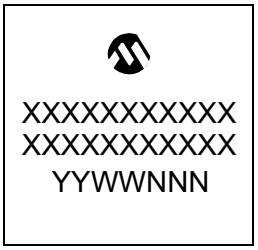
TABLE 33-24: RESET AND BROWN-OUT RESET REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
SY10	TMCL	$\overline{\text{MCLR}}$ Pulse Width (Low)	2	—	—	μs	
SY12	TPOR	Power-on Reset Delay	—	2	—	μs	
SY13	TIOZ	I/O High-Impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset	Lesser of: (3 TCY + 2) or 700	—	(3 TCY + 2)	μs	
SY25	TBOR	Brown-out Reset Pulse Width	1	—	—	μs	VDD ≤ VBOR
SY45	TRST	Internal State Reset Time	—	50	—	μs	
SY71	TPM	Program Memory Wake-up Time	—	20	—	μs	Sleep wake-up with VREGS = 1
			—	1	—	μs	Sleep wake-up with VREGS = 0
SY72	TLVR	Low-Voltage Regulator Wake-up Time	—	90	—	μs	Sleep wake-up with VREGS = 1
			—	70	—	μs	Sleep wake-up with VREGS = 0

34.0 PACKAGING INFORMATION

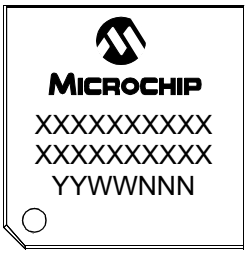
34.1 Package Marking Information

64-Lead QFN (9x9x0.9 mm)

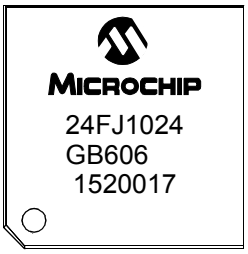


Example

64-Lead TQFP (10x10x1 mm)



Example

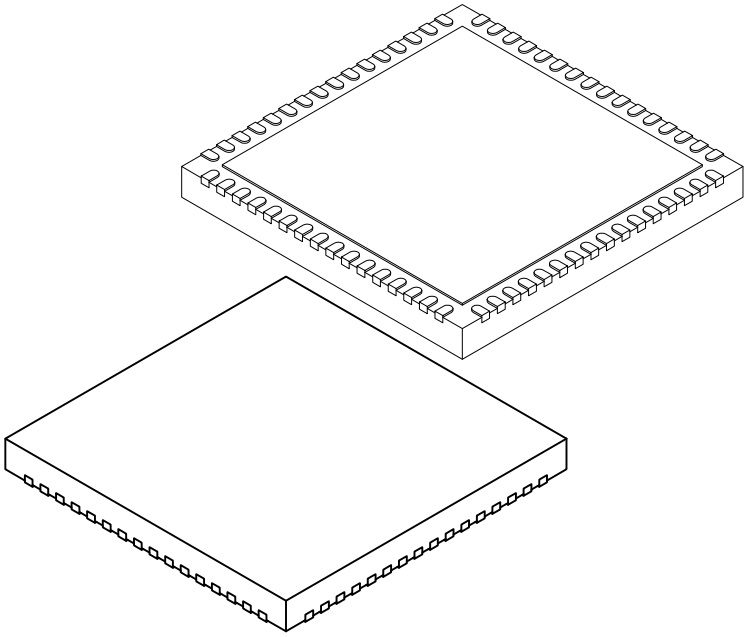


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 7.70 x 7.70 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	7.60	7.70	7.80
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	7.60	7.70	7.80
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-213B Sheet 2 of 2