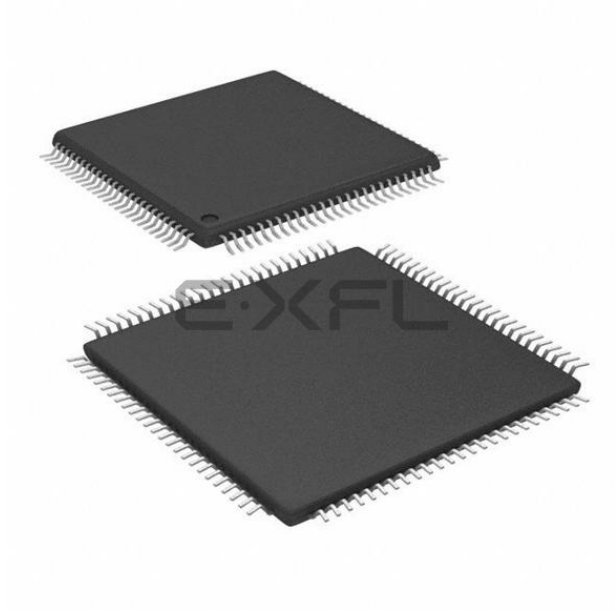
Microchip Technology - PIC24FJ512GB610T-I/PT Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, HLVD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj512gb610t-i-pt

TABLE 1-3: PIC24FJ1024GA610/GB610 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locator						I/O	Input Buffer	Description
	GA606 64-Pin QFN/TQFP/ QFP	GB606 64-Pin QFN/ TQFP/QFP	GA610 100-Pin TQFP/ QFP	GB610 100-Pin TQFP/ QFP	GA612 121-Pin BGA	GB612 121-Pin BGA			
IOCD0	46	46	72	72	D9	D9	I	ST	PORTD Interrupt-on-Change
IOCD1	49	49	76	76	A11	A11	I	ST	
IOCD2	50	50	77	77	A10	A10	I	ST	
IOCD3	51	51	78	78	B9	B9	I	ST	
IOCD4	52	52	81	81	C8	C8	I	ST	
IOCD5	53	53	82	82	B8	B8	I	ST	
IOCD6	54	54	83	83	D7	D7	I	ST	
IOCD7	55	55	84	84	C7	C7	I	ST	
IOCD8	42	42	68	68	E9	E9	I	ST	
IOCD9	43	43	69	69	E10	E10	I	ST	
IOCD10	44	44	70	70	D11	D11	I	ST	
IOCD11	45	45	71	71	C11	C11	I	ST	
IOCD12	—	—	79	79	A9	A9	I	ST	
IOCD13	—	—	80	80	D8	D8	I	ST	
IOCD14	—	—	47	47	L9	L9	I	ST	
IOCD15	—	—	48	48	K9	K9	I	ST	
IOCE0	60	60	93	93	A4	A4	I	ST	PORTE Interrupt-on-Change
IOCE1	61	61	94	94	B4	B4	I	ST	
IOCE2	62	62	98	98	B3	B3	I	ST	
IOCE3	63	63	99	99	A2	A2	I	ST	
IOCE4	64	64	100	100	A1	A1	I	ST	
IOCE5	1	1	3	3	D3	D3	I	ST	
IOCE6	2	2	4	4	C1	C1	I	ST	
IOCE7	3	3	5	5	D2	D2	I	ST	
IOCE8	—	—	18	18	G1	G1	I	ST	
IOCE9	—	—	19	19	G2	G2	I	ST	

Legend: TTL = TTL input buffer
ANA = Analog level input/output
DIG = Digital input/output
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated Transceiver

TABLE 1-3: PIC24FJ1024GA610/GB610 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locator						I/O	Input Buffer	Description
	GA606 64-Pin QFN/TQFP/ QFP	GB606 64-Pin QFN/ TQFP/QFP	GA610 100-Pin TQFP/ QFP	GB610 100-Pin TQFP/ QFP	GA612 121-Pin BGA	GB612 121-Pin BGA			
OCM2A	6	6	12	12	F2	F2	O	DIG	MCCP2 Outputs
OCM2B	8	8	14	14	F3	F3	O	DIG	
OCM2C	—	—	7	7	E4	E4	O	DIG	
OCM2D	—	—	8	8	E2	E2	O	DIG	
OCM2E	—	—	96	96	C3	C3	O	DIG	
OCM2F	—	—	97	97	A3	A3	O	DIG	
OCM3A	11	11	20	20	H1	H1	O	DIG	MCCP3 Outputs
OCM3B	12	12	21	21	H2	H2	O	DIG	
OCM3C	—	—	9	9	E1	E1	O	DIG	
OCM3D	—	—	17	17	G3	G3	O	DIG	
OCM3E	—	—	79	79	A9	A9	O	DIG	
OCM3F	—	—	80	80	D8	D8	O	DIG	
OSCI	39	39	63	63	F9	F9	I	ANA/ ST	Main Oscillator Input Connection
OSCO	40	40	64	64	F11	F11	O	ANA	Main Oscillator Output Connection
PGEC1	15	15	24	24	K1	K1	I	ST	ICSP™ Programming Clock
PGEC2	17	17	26	26	L1	L1	I	ST	
PGEC3	11	11	20	20	H1	H1	I	ST	
PGED1	16	16	25	25	K2	K2	I/O	DIG/ST	ICSP Programming Data
PGED2	18	18	27	27	J3	J3	I/O	DIG/ST	
PGED3	12	12	21	21	H2	H2	I/O	DIG/ST	
PMA0/ PMALL	30	30	44	44	L8	L8	I/O	DIG/ ST/TTL	Parallel Master Port Address<0>/ Address Latch Low
PMA1/ PMALH	29	29	43	43	K7	K7	I/O	DIG/ ST/TTL	Parallel Master Port Address<1>/ Address Latch High
PMA14/ PMCS1	45	45	71	71	C11	C11	I/O	DIG/ ST/TTL	Parallel Master Port Address<14>/ Slave Chip Select/Chip Select 1 Strobe
PMA15/ PMCS2	44	44	70	70	D11	D11	I/O	DIG/ ST/TTL	Parallel Master Port Address<15>/ Chip Select 2 Strobe
PMA6	16	16	29	29	K3	K3	O	DIG	Parallel Master Port Address
PMA7	22	22	28	28	L2	L2	O	DIG	

Legend: TTL = TTL input buffer
ANA = Analog level input/output
DIG = Digital input/output
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated Transceiver

TABLE 1-3: PIC24FJ1024GA610/GB610 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Pin Function	Pin Number/Grid Locator						I/O	Input Buffer	Description
	GA606 64-Pin QFN/TQFP/ QFP	GB606 64-Pin QFN/ TQFP/QFP	GA610 100-Pin TQFP/ QFP	GB610 100-Pin TQFP/ QFP	GA612 121-Pin BGA	GB612 121-Pin BGA			
RP0	16	16	25	25	K2	K2	I/O	DIG/ST	Remappable Peripherals (input or output)
RP1	15	15	24	24	K1	K1	I/O	DIG/ST	
RP2	42	42	68	68	E9	E9	I/O	DIG/ST	
RP3	44	44	70	70	D11	D11	I/O	DIG/ST	
RP4	43	43	69	69	E10	E10	I/O	DIG/ST	
RP5	—	—	48	48	K9	K9	I/O	DIG/ST	
RP6	17	17	26	26	L1	L1	I/O	DIG/ST	
RP7	18	18	27	27	J3	J3	I/O	DIG/ST	
RP8	21	21	32	32	K4	K4	I/O	DIG/ST	
RP9	22	22	33	33	L4	L4	I/O	DIG/ST	
RP10	31	31	49	49	L10	L10	I/O	DIG/ST	
RP11	46	46	72	72	D9	D9	I/O	DIG/ST	
RP12	45	45	71	71	C11	C11	I/O	DIG/ST	
RP13	14	14	23	23	J2	J2	I/O	DIG/ST	
RP14	29	29	43	43	K7	K7	I/O	DIG/ST	
RP15	—	—	53	53	J10	J10	I/O	DIG/ST	
RP16	33	33	51	51	K10	K10	I/O	DIG/ST	
RP17	32	32	50	50	L11	L11	I/O	DIG/ST	
RP18	11	11	20	20	H1	H1	I/O	DIG/ST	
RP19	6	6	12	12	F2	F2	I/O	DIG/ST	
RP20	53	53	82	82	B8	B8	I/O	DIG/ST	
RP21	4	4	10	10	E3	E3	I/O	DIG/ST	
RP22	51	51	78	78	B9	B9	I/O	DIG/ST	
RP23	50	50	77	77	A10	A10	I/O	DIG/ST	
RP24	49	49	76	76	A11	A11	I/O	DIG/ST	
RP25	52	52	81	81	C8	C8	I/O	DIG/ST	
RP26	5	5	11	11	F4	F4	I/O	DIG/ST	
RP27	8	8	14	14	F3	F3	I/O	DIG/ST	
RP28	12	12	21	21	H2	H2	I/O	DIG/ST	
RP29	30	30	44	44	L8	L8	I/O	DIG/ST	
RP30	34	—	52	52	K11	K11	I/O	DIG/ST	
RP31	—	—	39	39	L6	L6	I/O	DIG/ST	

Legend: TTL = TTL input buffer
ANA = Analog level input/output
DIG = Digital input/output
ST = Schmitt Trigger input buffer
I^2C = I^2C/SMBus input buffer
XCVR = Dedicated Transceiver

7.0 RESETS

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Reset"** (DS39712), which is available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

The Reset module combines all Reset sources and controls the device Master Reset Signal, $\overline{\text{SYSRST}}$. The following is a list of device Reset sources:

- POR: Power-on Reset
- $\overline{\text{MCLR}}$: Master Clear Pin Reset
- SWR: RESET Instruction
- WDT: Watchdog Timer Reset
- BOR: Brown-out Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Opcode Reset
- UWR: Uninitialized W Register Reset

A simplified block diagram of the Reset module is shown in Figure 7-1.

Any active source of Reset will make the $\overline{\text{SYSRST}}$ signal active. Many registers associated with the CPU and peripherals are forced to a known Reset state. Most registers are unaffected by a Reset; their status is unknown on POR and unchanged by all other Resets.

Note:	Refer to the specific peripheral or CPU section of this manual for register Reset states.

All types of device Reset will set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 7-1). A POR will clear all bits, except for the BOR and POR (RCON<1:0>) bits, which are set. The user may set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software will not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this data sheet.

Note:	The status bits in the RCON register should be cleared after they are read so that the next RCON register values after a device Reset will be meaningful.

FIGURE 7-1: RESET SYSTEM BLOCK DIAGRAM

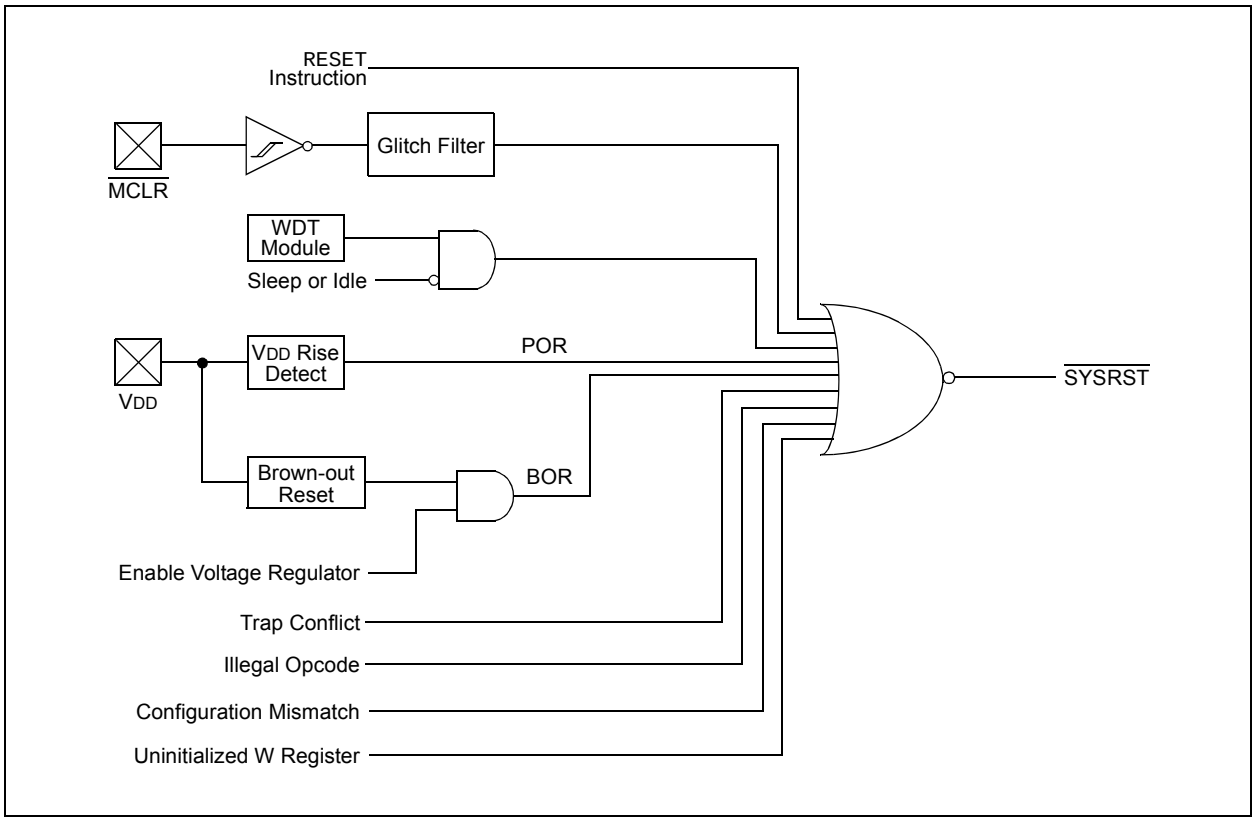


TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	FNOSC<2:0>	Notes
Oscillator with Frequency Division (OSCFDIV)	Internal/External	111	**1, 2, 3**
Digitally Controlled Oscillator (DCO)	Internal	110	**3**
Low-Power RC Oscillator (LPRC)	Internal	101	**3**
Secondary (Timer1) Oscillator (SOSC)	Secondary	100	**3**
Primary Oscillator (XT, HS or EC) with PLL Module	Primary	011	**4**
Primary Oscillator (XT, HS or EC)	Primary	010	**4**
Fast RC Oscillator with PLL Module (FRCPLL)	Internal	001	**3**
Fast RC Oscillator (FRC)	Internal	000	**3**

Note 1: The input oscillator to the OSCFDIV Clock mode is determined by the RCDIV<2:0> (CLKDIV<10:8) bits. At POR, the default value selects the FRC module.

2: This is the default oscillator mode for an unprogrammed (erased) device.

3: OSCO pin function is determined by the OSCIOFCN Configuration bit.

4: The POSCMD<1:0> Configuration bits select the oscillator driver mode (XT, HS or EC).

9.3 Control Registers

The operation of the oscillator is controlled by five Special Function Registers:

- OSCCON
- CLKDIV
- OSCTUN
- OSCDIV
- OSCFDIV

In addition, two registers are used to control the DCO:

- DCOCON
- DCOTUN

The OSCCON register (Register 9-1) is the main control register for the oscillator. It controls clock source switching and allows the monitoring of clock sources. OSCCON is protected by a write lock to prevent inadvertent clock switches. See **Section 9.4 “Clock Switching Operation”** for more information.

The CLKDIV register (Register 9-2) controls the features associated with Doze mode, as well as the postscalers for the OSCFDIV Clock mode and the PLL module.

The OSCTUN register (Register 9-3) allows the user to fine-tune the FRC Oscillator over a range of approximately ±1.5%. It also controls the FRC self-tuning features described in **Section 9.5 “FRC Active Clock Tuning”**.

The OSCDIV and OSCFDIV registers provide control for the system Oscillator Frequency Divider.

9.3.1 DCO OVERVIEW

The DCO (Digitally Controlled Oscillator) is a low-power alternative to the FRC. It can generate a wider selection of operating frequencies and can be trimmed to correct process variations if an exact frequency is required. However, the DCO is not designed for use with USB applications and cannot meet USB timing restrictions.

REGISTER 10-3: PMD3: PERIPHERAL MODULE DISABLE REGISTER 3

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	CMPMD	RTCCMD	PMPMD
bit 15							bit 8

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0
CRCMD	—	—	—	U3MD	I2C3MD	I2C2MD	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **CMPMD:** Triple Comparator Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 9 **RTCCMD:** RTCC Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 8 **PMPMD:** Enhanced Parallel Master Port Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 7 **CRCMD:** CRC Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **U3MD:** UART3 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 2 **I2C3MD:** I2C3 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 1 **I2C2MD:** I2C2 Module Disable bit
1 = Module is disabled
0 = Module power and clock sources are enabled

bit 0 **Unimplemented:** Read as '0'

REGISTER 11-3: ANSC: PORTC ANALOG FUNCTION SELECTION REGISTER

U-0	R/W-1	R/W-1	U-0	U-0	U-0	U-0	U-0
—	ANSC<14:13>		—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-1	U-0	U-0	U-0	U-0
—	—	—	ANSC4(1)	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-13 **ANSC<14:13>:** PORTC Analog Function Selection bits
1 = Pin is configured in Analog mode; I/O port read is disabled
0 = Pin is configured in Digital mode; I/O port read is enabled

bit 12-5 **Unimplemented:** Read as '0'

bit 4 **ANSC4:** PORTC Analog Function Selection bit(1)
1 = Pin is configured in Analog mode; I/O port read is disabled
0 = Pin is configured in Digital mode; I/O port read is enabled

bit 3-0 **Unimplemented:** Read as '0'

Note 1: ANSC4 is not available on 64-pin devices.

REGISTER 11-4: ANSD: PORTD ANALOG FUNCTION SELECTION REGISTER

U-0	U-0	r-1	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-1	R/W-1	U-0	U-0	U-0	U-0	U-0	U-0
ANSD<7:6>		—	—	—	—	—	—
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **Reserved:** Read as '1'

bit 12-8 **Unimplemented:** Read as '0'

bit 7-6 **ANSD<7:6>:** PORTD Analog Function Selection bits
1 = Pin is configured in Analog mode; I/O port read is disabled
0 = Pin is configured in Digital mode; I/O port read is enabled

bit 5-0 **Unimplemented:** Read as '0'

11.4.6 PERIPHERAL PIN SELECT REGISTERS

The PIC24FJ1024GA610/GB610 family of devices implements a total of 40 registers for remappable peripheral configuration:

- Input Remappable Peripheral Registers (24)
- Output Remappable Peripheral Registers (16)

Note: Input and Output register values can only be changed if IOLOCK (OSCCON<6>) = 0. See **Section 11.4.4.1 "Control Register Lock"** for a specific command sequence.

REGISTER 11-12: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	INT1R5	INT1R4	INT1R3	INT1R2	INT1R1	INT1R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	OCTRIG1R5	OCTRIG1R4	OCTRIG1R3	OCTRIG1R2	OCTRIG1R1	OCTRIG1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **INT1R<5:0>:** Assign External Interrupt 1 (INT1) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **OCTRIG1R<5:0>:** Assign Output Compare Trigger 1 to Corresponding RPn or RPIn Pin bits

REGISTER 11-13: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	INT3R5	INT3R4	INT3R3	INT3R2	INT3R1	INT3R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	INT2R5	INT2R4	INT2R3	INT2R2	INT2R1	INT2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **INT3R<5:0>:** Assign External Interrupt 3 (INT3) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **INT2R<5:0>:** Assign External Interrupt 2 (INT2) to Corresponding RPn or RPIn Pin bits

REGISTER 11-24: RPINR15: PERIPHERAL PIN SELECT INPUT REGISTER 15

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	r-1	r-1	r-1	r-1	r-1	r-1
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **Reserved**: Maintain as ‘1’

REGISTER 11-25: RPINR17: PERIPHERAL PIN SELECT INPUT REGISTER 17

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	U3RXR5	U3RXR4	U3RXR3	U3RXR2	U3RXR1	U3RXR0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **U3RXR<5:0>:** Assign UART3 Receive (U3RX) to Corresponding RPn or RPIn Pin bits

bit 7-0 **Unimplemented:** Read as ‘0’

REGISTER 11-50: RPOR14: PERIPHERAL PIN SELECT OUTPUT REGISTER 14

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP29R5	RP29R4	RP29R3	RP29R2	RP29R1	RP29R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP28R5	RP28R4	RP28R3	RP28R2	RP28R1	RP28R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP29R<5:0>:** RP29 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP29 (see Table 11-4 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP28R<5:0>:** RP28 Output Pin Mapping bits
Peripheral Output Number n is assigned to pin, RP28 (see Table 11-4 for peripheral function numbers).

REGISTER 11-51: RPOR15: PERIPHERAL PIN SELECT OUTPUT REGISTER 15

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP31R5(1)	RP31R4(1)	RP31R3(1)	RP31R2(1)	RP31R1(1)	RP31R0(1)
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP30R5(2)	RP30R4(2)	RP30R3(2)	RP30R2(2)	RP30R1(2)	RP30R0(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP31R<5:0>:** RP31 Output Pin Mapping bits(1)
Peripheral Output Number n is assigned to pin, RP31 (see Table 11-4 for peripheral function numbers).

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP30R<5:0>:** RP30 Output Pin Mapping bits(2)
Peripheral Output Number n is assigned to pin, RP30 (see Table 11-4 for peripheral function numbers).

Note 1: These pins are not available in 64-pin devices.
2: These pins are not available on the PIC24FJXXXGB606.

REGISTER 17-4: SPIxSTATL: SPIx STATUS REGISTER LOW

U-0	U-0	U-0	R/C-0, HS	R-0, HSC	U-0	U-0	R-0, HSC
—	—	—	FRMERR	SPIBUSY	—	—	SPITUR(1)
bit 15							bit 8

R-0, HSC	R/C-0, HS	R-1, HSC	U-0	R-1, HSC	U-0	R-0, HSC	R-0, HSC
SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF
bit 7							bit 0

Legend:	C = Clearable bit	HS = Hardware Settable bit	x = Bit is unknown
R = Readable bit	W = Writable bit	'0' = Bit is cleared	HSC = Hardware Settable/Clearable bit
-n = Value at POR	'1' = Bit is set	U = Unimplemented bit, read as '0'	

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **FRMERR**: SPIx Frame Error Status bit
1 = Frame error is detected
0 = No frame error is detected

bit 11 **SPIBUSY:** SPIx Activity Status bit
1 = Module is currently busy with some transactions
0 = No ongoing transactions (at time of read)

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **SPITUR:** SPIx Transmit Underrun Status bit(1)
1 = Transmit buffer has encountered a Transmit Underrun condition
0 = Transmit buffer does not have a Transmit Underrun condition

bit 7 **SRMT:** Shift Register Empty Status bit
1 = No current or pending transactions (i.e., neither SPIxTXB or SPIxTXSR contains data to transmit)
0 = Current or pending transactions

bit 6 **SPIROV:** SPIx Receive Overflow Status bit
1 = A new byte/half-word/word has been completely received when the SPIxRXB is full
0 = No overflow

bit 5 **SPIRBE:** SPIx RX Buffer Empty Status bit
1 = RX buffer is empty
0 = RX buffer is not empty
Standard Buffer Mode:
Automatically set in hardware when SPIxBUF is read from, reading SPIxRXB. Automatically cleared in hardware when SPIx transfers data from SPIxRXSR to SPIxRXB.
Enhanced Buffer Mode:
Indicates RXELM<5:0> = 6'b000000.

bit 4 **Unimplemented:** Read as '0'

bit 3 **SPITBE:** SPIx Transmit Buffer Empty Status bit
1 = SPIxTXB is empty
0 = SPIxTXB is not empty
Standard Buffer Mode:
Automatically set in hardware when SPIx transfers data from SPIxTXB to SPIxTXSR. Automatically cleared in hardware when SPIxBUF is written, loading SPIxTXB.
Enhanced Buffer Mode:
Indicates TXELM<5:0> = 6'b000000.

Note 1: SPITUR is cleared when SPIEN = 0. When IGNTUR = 1, SPITUR provides dynamic status of the Transmit Underrun condition, but does not stop RX/TX operation and does not need to be cleared by software.

FIGURE 17-5: SPIx MASTER, FRAME SLAVE CONNECTION DIAGRAM

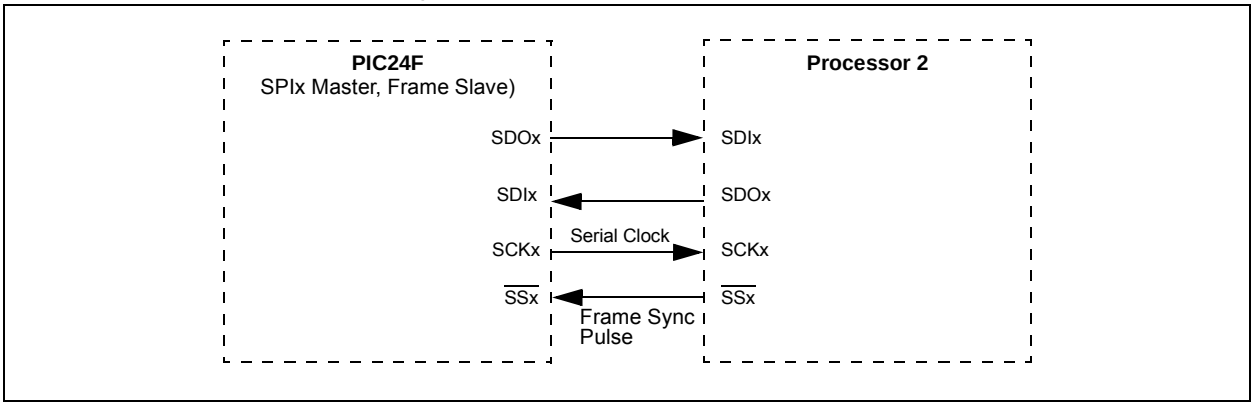


FIGURE 17-6: SPIx SLAVE, FRAME MASTER CONNECTION DIAGRAM

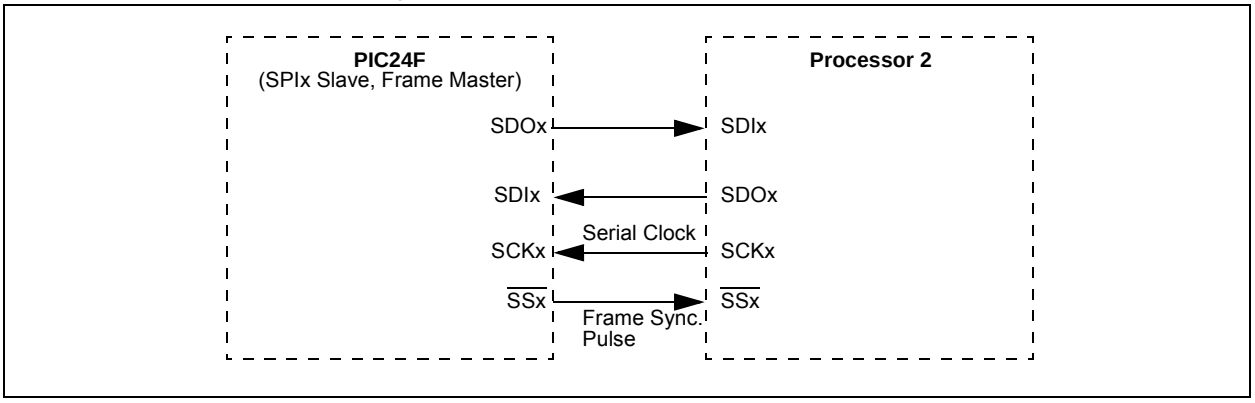
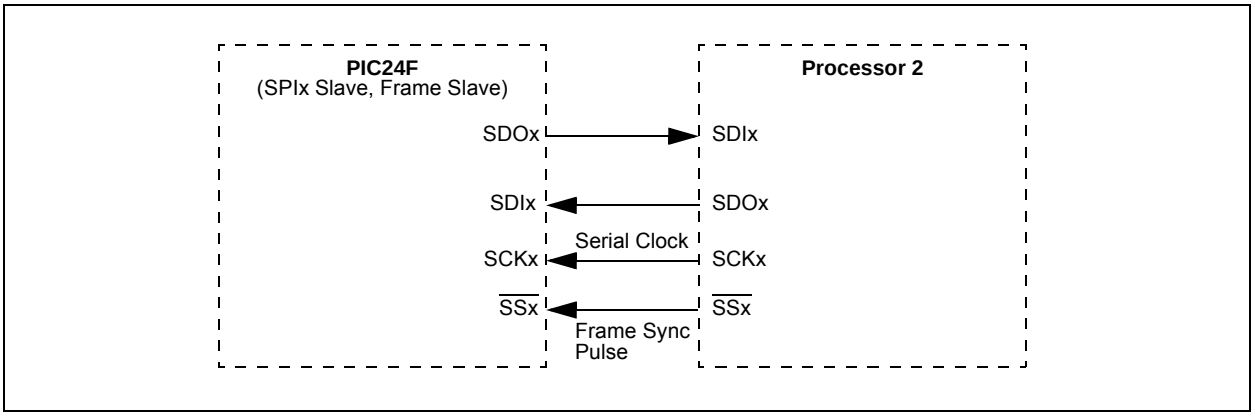


FIGURE 17-7: SPIx SLAVE, FRAME SLAVE CONNECTION DIAGRAM



EQUATION 17-1: RELATIONSHIP BETWEEN DEVICE AND SPIx CLOCK SPEED

$$\text{Baud Rate} = \frac{\text{FPB}}{(2 * (\text{SPIxBRG} + 1))}$$

Where:

FPB is the Peripheral Bus Clock Frequency.

REGISTER 18-2: I2CxCONH: I2Cx CONTROL REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PCIE	SCIE	BOEN	SDAHT(1)	SBCDE	AHEN	DHEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **PCIE:** Stop Condition Interrupt Enable bit (I^2C Slave mode only)
1 = Enables interrupt on detection of Stop condition
0 = Stop detection interrupts are disabled

bit 5 **SCIE:** Start Condition Interrupt Enable bit (I^2C Slave mode only)
1 = Enables interrupt on detection of Start or Restart conditions
0 = Start detection interrupts are disabled

bit 4 **BOEN:** Buffer Overwrite Enable bit (I^2C Slave mode only)
1 = I2CxRCV is updated and an ACK is generated for a received address/data byte, ignoring the state of the I2COV bit only if RBF bit = 0
0 = I2CxRCV is only updated when I2COV is clear

bit 3 **SDAHT:** SDAx Hold Time Selection bit(1)
1 = Minimum of 300 ns hold time on SDAx after the falling edge of SCLx
0 = Minimum of 100 ns hold time on SDAx after the falling edge of SCLx

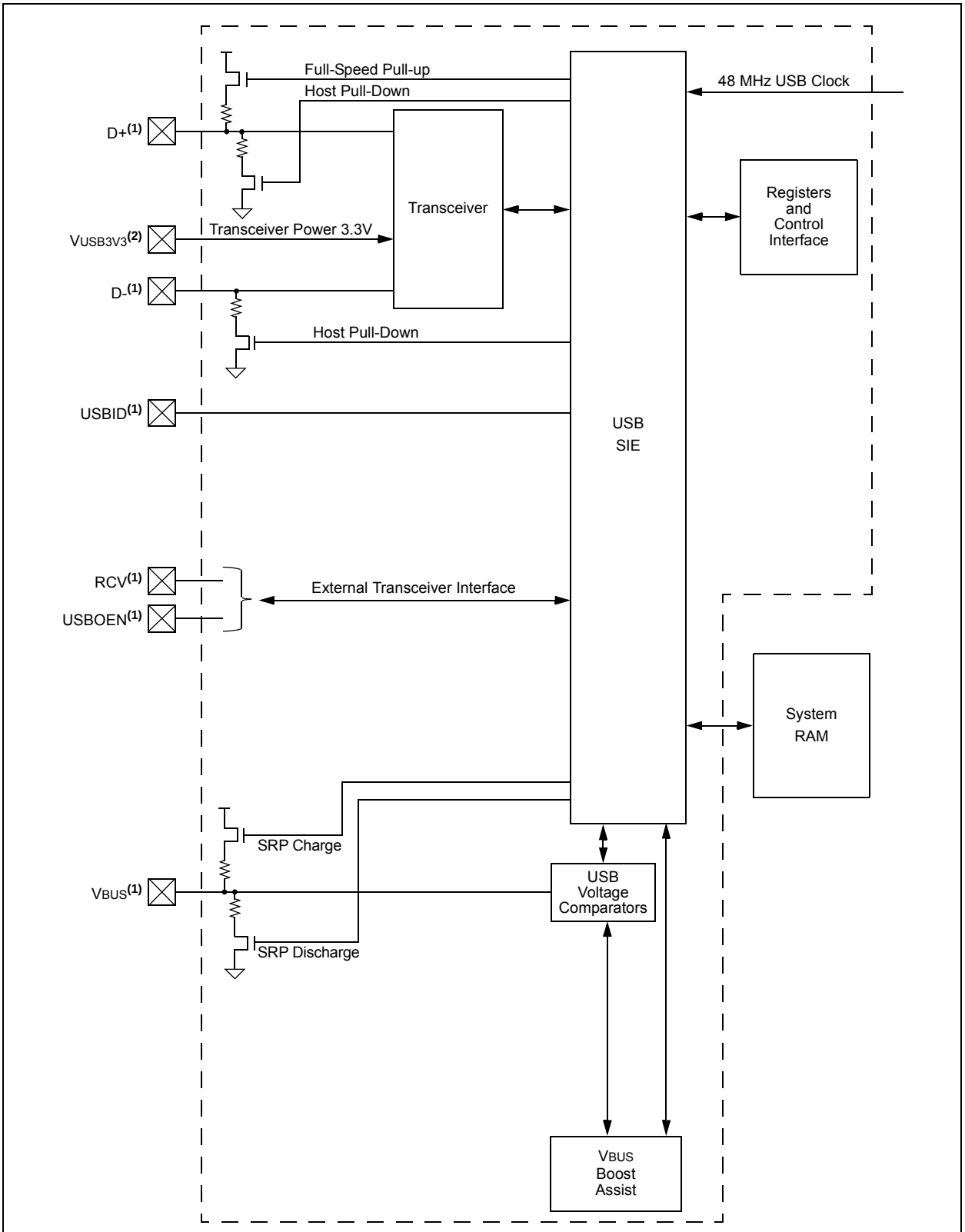
bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I^2C Slave mode only)
If, on the rising edge of SCLx, SDAx is sampled low when the module is outputting a high state, the BCL bit is set and the bus goes Idle. This Detection mode is only valid during data and ACK transmit sequences.
1 = Enables slave bus collision interrupts
0 = Slave bus collision interrupts are disabled

bit 1 **AHEN:** Address Hold Enable bit (I^2C Slave mode only)
1 = Following the 8th falling edge of SCLx for a matching received address byte; SCLREL bit (I2CxCONL<12>) will be cleared and SCLx will be held low
0 = Address holding is disabled

bit 0 **DHEN:** Data Hold Enable bit (I^2C Slave mode only)
1 = Following the 8th falling edge of SCLx for a received data byte; slave hardware clears the SCLREL bit (I2CxCONL<12>) and SCLx is held low
0 = Data holding is disabled

Note 1: This bit must be set to '0' for 1 MHz operation.

FIGURE 20-1: USB OTG MODULE BLOCK DIAGRAM



Note 1: Pins are multiplexed with digital I/O and other device features.

2: Connecting V_{BUS3V3} to V_{DD} is highly recommended, as floating this input can cause increased I_{PD} currents. The pin should be tied to V_{DD} when the USB functions are not used.

20.7.1 USB OTG MODULE CONTROL REGISTERS

REGISTER 20-3: U1OTGSTAT: USB OTG STATUS REGISTER (HOST MODE ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0, HSC	U-0	R-0, HSC	U-0	R-0, HSC	R-0, HSC	U-0	R-0, HSC
ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **ID:** ID Pin State Indicator bit
- 1 = No plug is attached or a Type B cable has been plugged into the USB receptacle
- 0 = A Type A plug has been plugged into the USB receptacle

bit 6 **Unimplemented:** Read as '0'

bit 5 **LSTATE:** Line State Stable Indicator bit
- 1 = The USB line state (as defined by SE0 and JSTATE) has been stable for the previous 1 ms
- 0 = The USB line state has not been stable for the previous 1 ms

bit 4 **Unimplemented:** Read as '0'

bit 3 **SESVD:** Session Valid Indicator bit
- 1 = The VBUS voltage is above VA_SESS_VLD (as defined in the *"USB 2.0 Specification"*) on the A or B-device
- 0 = The VBUS voltage is below VA_SESS_VLD on the A or B-device

bit 2 **SESEND:** B Session End Indicator bit
- 1 = The VBUS voltage is below VB_SESS_END (as defined in the *"USB 2.0 Specification"*) on the B-device
- 0 = The VBUS voltage is above VB_SESS_END on the B-device

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVD:** A VBUS Valid Indicator bit
- 1 = The VBUS voltage is above VA_VBUS_VLD (as defined in the *"USB 2.0 Specification"*) on the A-device
- 0 = The VBUS voltage is below VA_VBUS_VLD on the A-device

REGISTER 22-6: RTCSTATL: RTCC STATUS REGISTER (LOW)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/C-0	U-0	R/C-0	R-0	R-0	R-0
—	—	ALMEVT	—	TSAEVT(1)	SYNC	ALMSYNC	HALFSEC(2)
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5 **ALMEVT:** Alarm Event bit
1 = An alarm event has occurred
0 = An alarm event has not occurred

bit 4 **Unimplemented:** Read as '0'

bit 3 **TSAEVT**: Timestamp A Event bit(1)
1 = A timestamp event has occurred
0 = A timestamp event has not occurred

bit 2 **SYNC:** Synchronization Status bit
1 = Time registers may change during software read
0 = Time registers may be read safely

bit 1 **ALMSYNC:** Alarm Synchronization Status bit
1 = Alarm registers (ALMTIME and ALMDATE) and Alarm Mask bits (AMASK<3:0>) should not be modified, and Alarm Control bits (ALRMEN, ALMRPT<7:0>) may change during software read
0 = Alarm registers and Alarm Control bits may be written/modified safely

bit 0 **HALFSEC:** Half Second Status bit(2)
1 = Second half period of a second
0 = First half period of a second

Note 1: User software may write a '1' to this location to initiate a Timestamp A event; timestamp capture is not valid until TSAEVT reads as '1'.

2: This bit is read-only; it is cleared to '0' on a write to the SECONE<3:0> bits.

22.6.1 POWER CONTROL CLOCK SOURCE

The stability and sample windows are controlled by the PWCSAMPx and PWCSTABx bit fields in the RTCCON3L register (RTCCON3L<15:8> and <7:0>, respectively). As both the stability and sample windows are defined in terms of the RTCC clock, their absolute values vary by the value of the PWC clock base period (TPWCCLK). For example, using a 32.768 kHz SOSC input clock would produce a TPWCCLK of 1/32768 = 30.518 µs. The 8-bit magnitude of PWCSTABx and PWCSAMPx allows for a window size of 0 to 255 TPWCCLK. The period of the PWC clock can also be adjusted with a 1:1, 1:16, 1:64 or 1:256 prescaler, determined by the PWCPS<1:0> bits (RTCCON2L<7:6>).

In addition, certain values for the PWCSTABx and PWCSAMPx fields have specific control meanings in determining power control operations. If either bit field is 00h, the corresponding window is inactive. In addition, if the PWCSTABx field is FFh, the stability window remains active continuously, even if power control is disabled.

22.7 Event Timestamping

The RTCC includes a set of Timestamp registers that may be used for the capture of Time and Date register values when an external input signal is received. The RTCC will trigger a timestamp event when a low pulse occurs on the TMPR pin.

22.7.1 TIMESTAMP OPERATION

The event input is enabled for timestamping using the TSAEN bit (RTCCON1L<0>). When the timestamp event occurs, the present time and date values will be stored in the TSATIMEL/H and TSADATEL/H registers, the TSAEVT status bit (RTCSTATL<3>) will be set and an RTCC interrupt will occur. A new timestamp capture event cannot occur until the user clears the TSAEVT status bit.

Note 1: The TSATIMEL/H and TSADATEL/H register pairs can be used for data storage when TSAEN = 0. The values of TSATIMEL/H and TSADATEL/H will be maintained throughout all types of non-Power-on Resets (MCLR, WDT, etc).

22.7.2 MANUAL TIMESTAMP OPERATION

The current time and date may be captured in the TSATIMEL/H and TSADATEL/H registers by writing a '1' to the TSAEVT bit location while the timestamp functionality is enabled (TSAEN = 1). This write will not set the TSAEVT bit, but it will initiate a timestamp capture. The TSAEVT bit will be set when the capture operation is complete. The user must poll the TSAEVT bit to determine when the capture operation is complete.

After the Timestamp registers have been read, the TSAEVT bit should be cleared to allow further hardware or software timestamp capture events.

REGISTER 25-3: AD1CON3: A/D CONTROL REGISTER 3

R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC(1)	EXTSAM	PUMPEN(2)	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ADRC:** A/D Conversion Clock Source bit(1)
1 = Dedicated ADC RC clock generator (4 MHz nominal)
0 = Clock derived from system clock

bit 14 **EXTSAM:** Extended Sampling Time bit
1 = A/D is still sampling after SAMP = 0
0 = A/D is finished sampling

bit 13 **PUMPEN:** Charge Pump Enable bit(2)
1 = Charge pump for switches is enabled
0 = Charge pump for switches is disabled

bit 12-8 **SAMC<4:0>:** Auto-Sample Time Select bits
11111 = 31 TAD
• • •
00001 = 1 TAD
00000 = 0 TAD

bit 7-0 **ADCS<7:0>:** A/D Conversion Clock Select bits
11111111 = 256 • TCY = TAD
• • •
00000001 = 2 • TCY = TAD
00000000 = TCY = TAD

Note 1: Selecting the internal ADC RC clock requires that ADCSx be '1' or greater. Setting ADCSx = 0 when ADRC = 1 will violate the TAD (min) specification.

2: Enable the charge pump if AVDD is < 2.7V. Longer sample times are required due to the increase of the internal resistance of the MUX if the charge pump is disabled.

REGISTER 25-5: AD1CON5: A/D CONTROL REGISTER 5

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
ASEN	LPEN	CTMREQ	BGREQ	—	—	ASINT1	ASINT0
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	WM1	WM0	CM1	CM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ASEN:** Auto-Scan Enable bit
1 = Auto-scan is enabled
0 = Auto-scan is disabled

bit 14 **LPEN:** Low-Power Enable bit
1 = Low power is enabled after scan
0 = Full power is enabled after scan

bit 13 **CTMREQ:** CTMU Request bit
1 = CTMU is enabled when the A/D is enabled and active
0 = CTMU is not enabled by the A/D

bit 12 **BGREQ:** Band Gap Request bit
1 = Band gap is enabled when the A/D is enabled and active
0 = Band gap is not enabled by the A/D

bit 11-10 **Unimplemented:** Read as '0'

bit 9-8 **ASINT<1:0>:** Auto-Scan (Threshold Detect) Interrupt Mode bits
11 = Interrupt after Threshold Detect sequence has completed and valid compare has occurred
10 = Interrupt after valid compare has occurred
01 = Interrupt after Threshold Detect sequence has completed
00 = No interrupt

bit 7-4 **Unimplemented:** Read as '0'

bit 3-2 **WM<1:0>:** Write Mode bits
11 = Reserved
10 = Auto-compare only (conversion results are not saved, but interrupts are generated when a valid match occurs, as defined by the CMx and ASINTx bits)
01 = Convert and save (conversion results are saved to locations as determined by the register bits when a match occurs, as defined by the CMx bits)
00 = Legacy operation (conversion data is saved to a location determined by the Buffer register bits)

bit 1-0 **CM<1:0>:** Compare Mode bits
11 = Outside Window mode: Valid match occurs if the conversion result is outside of the window defined by the corresponding buffer pair
10 = Inside Window mode: Valid match occurs if the conversion result is inside the window defined by the corresponding buffer pair
01 = Greater Than mode: Valid match occurs if the result is greater than the value in the corresponding Buffer register
00 = Less Than mode: Valid match occurs if the result is less than the value in the corresponding Buffer register

NOTES: