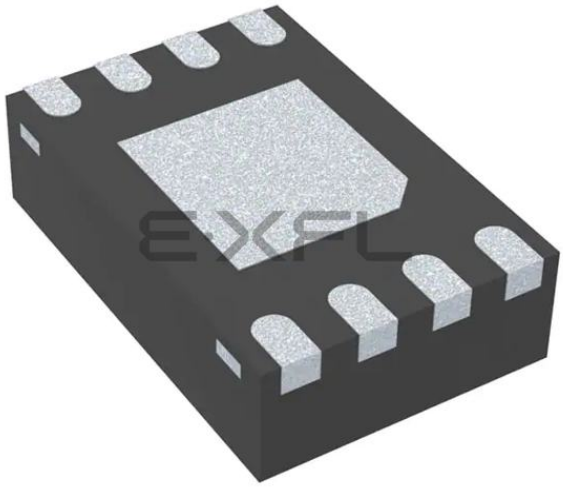

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | - |
| Peripherals | POR, WDT |
| Number of I/O | 5 |
| Program Memory Size | 768B (512 x 12) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 25 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 8-VFDFN Exposed Pad |
| Supplier Device Package | 8-DFN (2x3) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic12f508-i-mc |

# PIC12F508/509/16F505

## 8/14-Pin, 8-Bit Flash Microcontrollers

### Devices Included In This Data Sheet:

- PIC12F508
- PIC12F509
- PIC16F505

### High-Performance RISC CPU:

- Only 33 Single-Word Instructions to Learn
- All Single-Cycle Instructions Except for Program Branches, which are Two-Cycle
- 12-Bit Wide Instructions
- 2-Level Deep Hardware Stack
- Direct, Indirect and Relative Addressing modes for Data and Instructions
- 8-Bit Wide Data Path
- 8 Special Function Hardware Registers
- Operating Speed:
  - DC – 20 MHz clock input (PIC16F505 only)
  - DC – 200 ns instruction cycle (PIC16F505 only)
  - DC – 4 MHz clock input
  - DC – 1000 ns instruction cycle

### Special Microcontroller Features:

- 4 MHz Precision Internal Oscillator:
  - Factory calibrated to ±1%
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Debugging (ICD) Support
- Power-On Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) with Dedicated On-Chip RC Oscillator for Reliable Operation
- Programmable Code Protection
- Multiplexed $\overline{\text{MCLR}}$ Input Pin
- Internal Weak Pull-Ups on I/O Pins
- Power-Saving Sleep mode
- Wake-Wp from Sleep on Pin Change
- Selectable Oscillator Options:
  - INTRC: 4 MHz precision Internal oscillator
  - EXTRC: External low-cost RC oscillator
  - XT: Standard crystal/resonator
  - HS: High-speed crystal/resonator (PIC16F505 only)
  - LP: Power-saving, low-frequency crystal
  - EC: High-speed external clock input (PIC16F505 only)

### Low-Power Features/CMOS Technology:

- Operating Current:
  - < 175 µA @ 2V, 4 MHz, typical
- Standby Current:
  - 100 nA @ 2V, typical
- Low-Power, High-Speed Flash Technology:
  - 100,000 Flash endurance
  - > 40 year retention
- Fully Static Design
- Wide Operating Voltage Range: 2.0V to 5.5V
- Wide Temperature Range:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C

### Peripheral Features (PIC12F508/509):

- 6 I/O Pins:
  - 5 I/O pins with individual direction control
  - 1 input only pin
  - High current sink/source for direct LED drive
  - Wake-on-change
  - Weak pull-ups
- 8-Bit Real-Time Clock/Counter (TMR0) with 8-Bit Programmable Prescaler

### Peripheral Features (PIC16F505):

- 12 I/O Pins:
  - 11 I/O pins with individual direction control
  - 1 input only pin
  - High current sink/source for direct LED drive
  - Wake-on-change
  - Weak pull-ups
- 8-Bit Real-Time Clock/Counter (TMR0) with 8-Bit Programmable Prescaler

## 2.0 PIC12F508/509/16F505 DEVICE VARIETIES

A variety of packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC12F508/509/16F505 Product Identification System at the back of this data sheet to specify the correct part number.

### 2.1 Quick Turn Programming (QTP) Devices

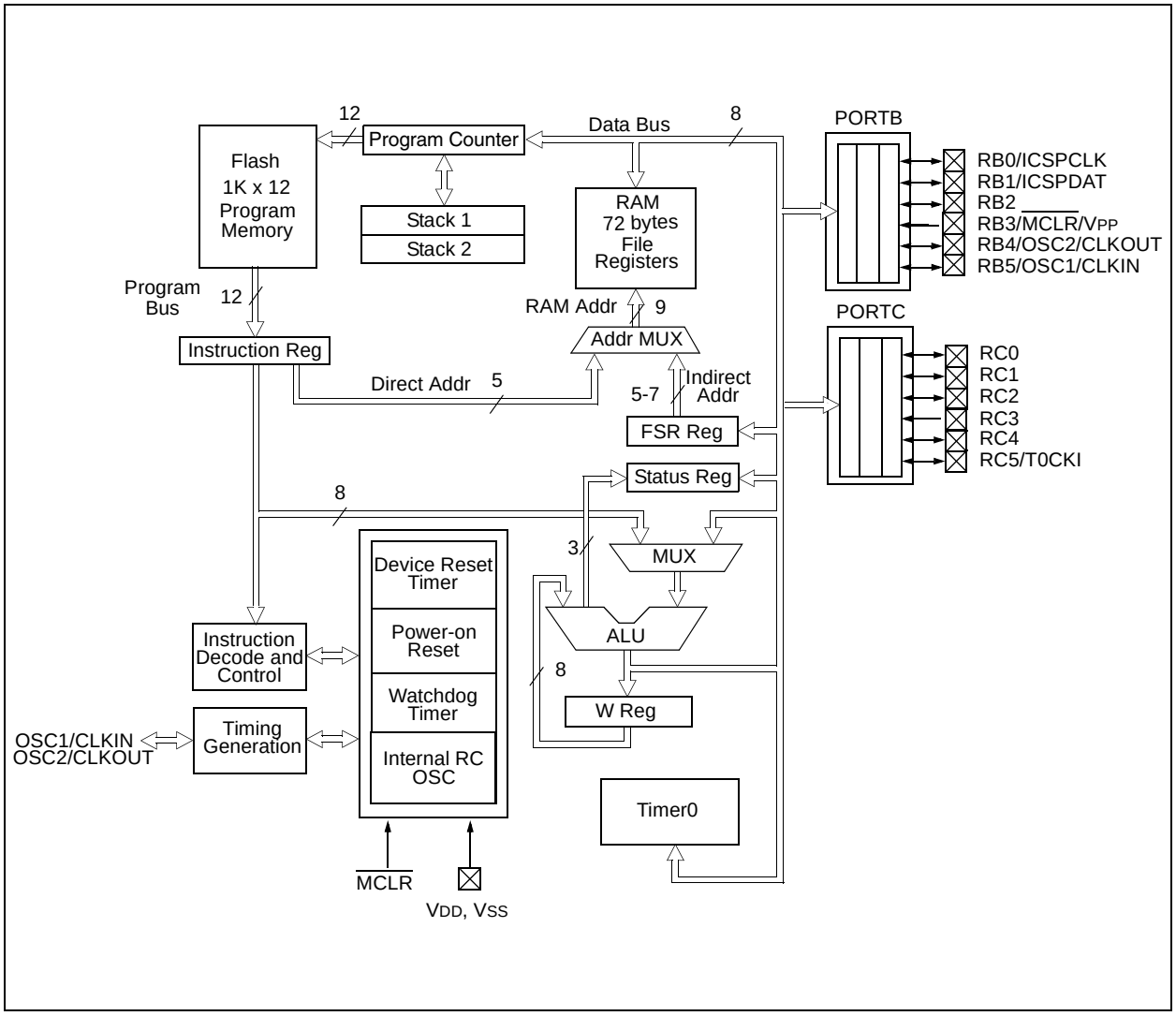
Microchip offers a QTP programming service for factory production orders. This service is made available for users who choose not to program medium-to-high quantity units and whose code patterns have stabilized. The devices are identical to the Flash devices but with all Flash locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

### 2.2 Serialized Quick Turn Programming$^{SM}$ (SQTP$^{SM}$) Devices

Microchip offers a unique programming service, where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number, which can serve as an entry code, password or ID number.

**FIGURE 3-2: PIC16F505 BLOCK DIAGRAM**



**REGISTER 4-2: STATUS REGISTER (ADDRESS: 03h) (PIC16F505)**

| R/W-0 | R/W-0 | R/W-0 | R-1 | R-1 | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| RBWUF | — | PA0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **RBWUF:** PORTB Reset bit
1 = Reset due to wake-up from Sleep on pin change
0 = After power-up or other Reset

bit 6 **Reserved**: Do not use

bit 5 **PA0**: Program Page Preselect bits
1 = Page 1 (200h-3FFh)
0 = Page 0 (000h-1FFh)
Each page is 512 bytes.
Using the PA0 bit as a general purpose read/write bit in devices which do not use it for program page preselect is not recommended, since this may affect upward compatibility with future products.

bit 4 **$\overline{TO}$**: Time-Out bit
1 = After power-up, CLRWDT instruction, or SLEEP instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$**: Power-Down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2 **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC**: Digit Carry/$\overline{Borrow}$ bit (for ADDWF and SUBWF instructions)
ADDWF:
1 = A carry from the 4th low-order bit of the result occurred
0 = A carry from the 4th low-order bit of the result did not occur
SUBWF:
1 = A borrow from the 4th low-order bit of the result did not occur
0 = A borrow from the 4th low-order bit of the result occurred

bit 0 **C**: Carry/$\overline{Borrow}$ bit (for ADDWF, SUBWF and RRF, RLF instructions)

| ADDWF: | SUBWF: | RRF or RLF: |
|---|---|---|
| 1 = A carry occurred | 1 = A borrow did not occur | Load bit with LSb or MSb, respectively |
| 0 = A carry did not occur | 0 = A borrow occurred | |

## 6.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select:
  - Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module.

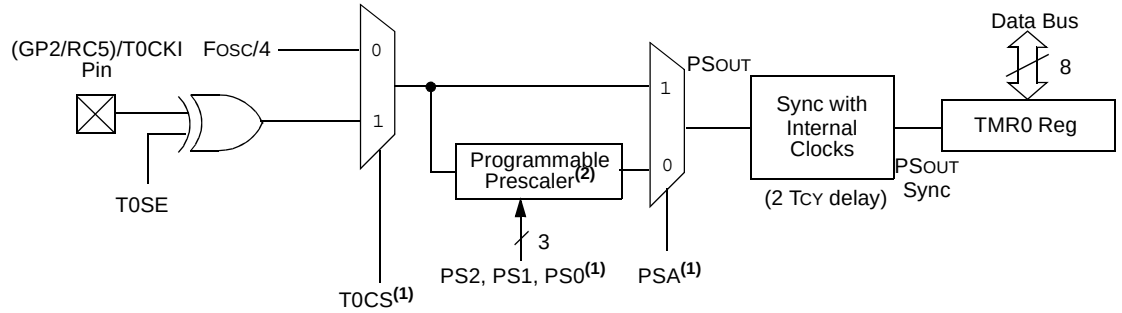
Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The T0SE bit (OPTION<4>) determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in **Section 6.1 "Using Timer0 with an External Clock"**.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit, PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. **Section 6.2 "Prescaler"** details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 6-1.

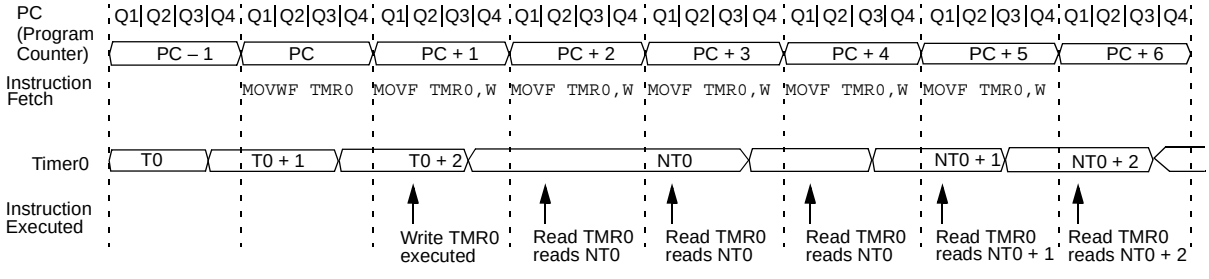
**FIGURE 6-1: TIMER0 BLOCK DIAGRAM**




**Note 1:** Bits T0CS, T0SE, PSA, PS2, PS1 and PS0 are located in the OPTION register.

**2:** The prescaler is shared with the Watchdog Timer (Figure 6-5).

**FIGURE 6-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE**



## 6.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (TOSC) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

### 6.1.1 EXTERNAL CLOCK SYNCHRONIZATION

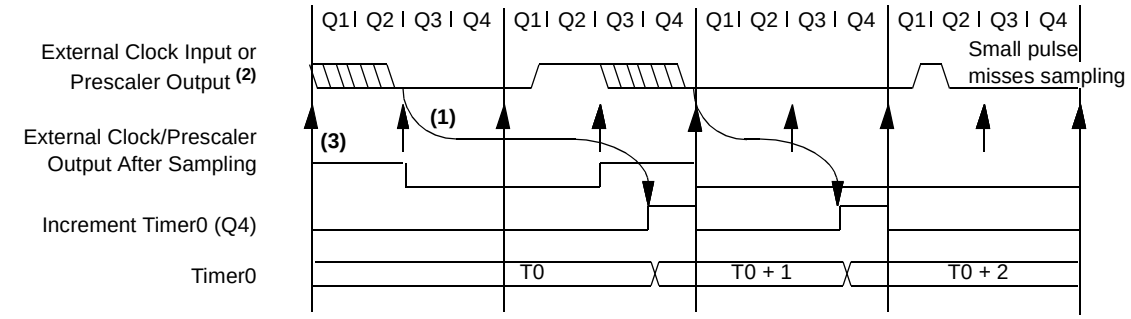
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-4). Therefore, it is necessary for T0CKI to be high for at least 2 TOSC (and a small RC delay of 2 Tt0H) and low for at least 2 TOSC (and a small RC delay of 2 Tt0H). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler, so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4 TOSC (and a small RC delay of 4 Tt0H) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of Tt0H. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

### 6.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 6-4 shows the delay from the external clock edge to the timer incrementing.

**FIGURE 6-4: TIMER0 TIMING WITH EXTERNAL CLOCK**




**Note 1:** Delay from clock input change to Timer0 increment is 3 TOSC to 7 TOSC. (Duration of Q = TOSC). Therefore, the error in measuring the interval between two edges on Timer0 input = ±4 TOSC max.

**2:** External clock if no prescaler selected; prescaler output otherwise.

**3:** The arrows indicate the points in time where sampling occurs.

## 7.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of real-time applications. The PIC12F508/509/16F505 microcontrollers have a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power-saving operating modes and offer code protection. These features are:

- Oscillator Selection
- Reset:
  - Power-on Reset (POR)
  - Device Reset Timer (DRT)
  - Wake-up from Sleep on Pin Change
- Watchdog Timer (WDT)
- Sleep
- Code Protection
- ID Locations
- In-Circuit Serial Programming™
- Clock Out

The PIC12F508/509/16F505 devices have a Watchdog Timer, which can be shut off only through Configuration bit WDTE. It runs off of its own RC oscillator for added reliability. If using HS (PIC16F505), XT or LP selectable oscillator options, there is always an 18 ms (nominal) delay provided by the Device Reset Timer (DRT), intended to keep the chip in Reset until the crystal oscillator is stable. If using INTRC or EXTRC, there is an 18 ms delay only on $V_{DD}$ power-up. With this timer on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low-current Power-Down mode. The user can wake-up from Sleep through a change on input pins or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application, including an internal 4 MHz oscillator. The EXTRC oscillator option saves system cost while the LP crystal option saves power. A set of Configuration bits are used to select various options.

### 7.1 Configuration Bits

The PIC12F508/509/16F505 Configuration Words consist of 12 bits. Configuration bits can be programmed to select various device configurations. Three bits are for the selection of the oscillator type; (two bits on the PIC12F508/509), one bit is the Watchdog Timer enable bit, one bit is the $\overline{MCLR}$ enable bit and one bit is for code protection (Register 7-1, Register 7-2).

**REGISTER 7-1: CONFIGURATION WORD FOR PIC12F508/509(1)**

| — | — | — | — | — | — | — | MCLRE | $\overline{CP}$ | WDTE | FOSC1 | FOSC0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| bit 11 | | | | | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 11-5 **Unimplemented**: Read as '0'

bit 4 **MCLRE:** GP3/$\overline{MCLR}$ Pin Function Select bit
1 = GP3/$\overline{MCLR}$ pin function is $\overline{MCLR}$
0 = GP3/$\overline{MCLR}$ pin function is digital input, $\overline{MCLR}$ internally tied to $V_{DD}$

bit 3 **$\overline{CP}$:** Code Protection bit
1 = Code protection off
0 = Code protection on

bit 2 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0 **FOSC<1:0>:** Oscillator Selection bits
11 = EXTRC = external RC oscillator
10 = INTRC = internal RC oscillator
01 = XT oscillator
00 = LP oscillator

**Note 1:** Refer to the "*PIC12F508/509 Memory Programming Specifications*" (DS41227) to determine how to access the Configuration Word. The Configuration Word is not user addressable during device operation.

**TABLE 7-4: RESET CONDITIONS FOR REGISTERS – PIC16F505**

| Register | Address | Power-on Reset | $\overline{\text{MCLR}}$ Reset, WDT Time-out, Wake-up On Pin Change |
|---|---|---|---|
| W | — | qqqq qqqu(1) | qqqq qqqu(1) |
| INDF | 00h | xxxx xxxx | uuuu uuuu |
| TMR0 | 01h | xxxx xxxx | uuuu uuuu |
| PC | 02h | 1111 1111 | 1111 1111 |
| STATUS | 03h | 0001 1xxx | q00q quuu(2), (3) |
| FSR | 04h | 100x xxxx | 1uuu uuuu |
| OSCCAL | 05h | 1111 111- | uuuu uuu- |
| PORTB | 06h | --xx xxxx | --uu uuuu |
| PORTC | 07h | --xx xxxx | --uu uuuu |
| OPTION | — | 1111 1111 | 1111 1111 |
| TRISB | — | --11 1111 | --11 1111 |
| TRISC | — | --11 1111 | --11 1111 |

**Legend:** u = unchanged, x = unknown, – = unimplemented bit, read as '0', q = value depends on condition.

**Note 1:** Bits <7:2> of W register contain oscillator calibration values due to MOVLW XX instruction at top of memory.

**2:** See Table 7-5 for Reset value for specific conditions.

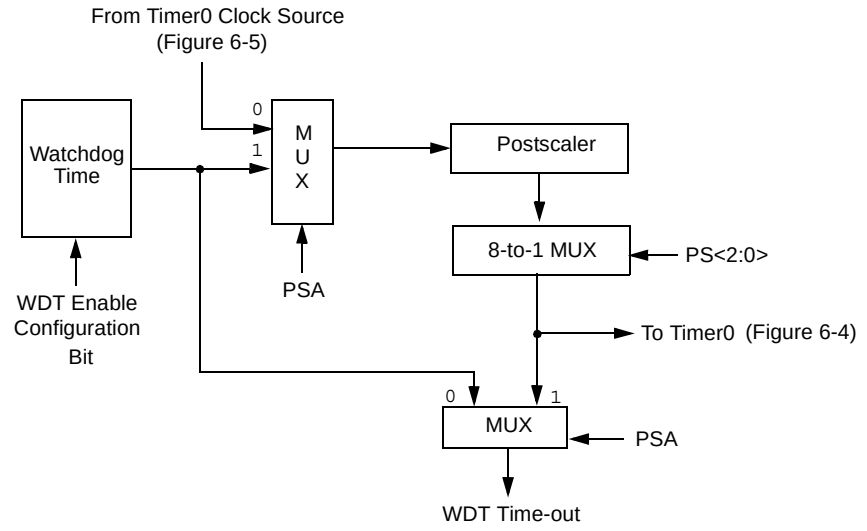
**3:** If Reset was due to wake-up on pin change, then bit 7 = 1. All other Resets will cause bit 7 = 0.

**TABLE 7-5: RESET CONDITION FOR SPECIAL REGISTERS**

| | STATUS Addr: 03h | PCL Addr: 02h |
|---|---|---|
| Power-on Reset | 0001 1xxx | 1111 1111 |
| $\overline{\text{MCLR}}$ Reset during normal operation | 000u uuuu | 1111 1111 |
| $\overline{\text{MCLR}}$ Reset during Sleep | 0001 0uuu | 1111 1111 |
| WDT Reset during Sleep | 0000 0uuu | 1111 1111 |
| WDT Reset normal operation | 0000 uuuu | 1111 1111 |
| Wake-up from Sleep on pin change | 1001 0uuu | 1111 1111 |

**Legend:** u = unchanged, x = unknown, – = unimplemented bit, read as '0'.

**FIGURE 7-11: WATCHDOG TIMER BLOCK DIAGRAM**




**Note 1:** T0CS, T0SE, PSA, PS<2:0> are bits in the OPTION register.

**TABLE 7-7: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-On Reset | Value on All Other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| N/A | OPTION(1) | $\overline{GPWU}$ | $\overline{GPPU}$ | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| N/A | OPTION(2) | $\overline{RBWU}$ | $\overline{RBPU}$ | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |

**Legend:** Shaded boxes = Not used by Watchdog Timer. – = unimplemented, read as '0', u = unchanged.

**Note 1:** PIC12F508/509 only.

**2:** PIC16F505 only.

## 7.9 Power-down Mode (Sleep)

A device may be powered down (Sleep) and later powered up (wake-up from Sleep).

### 7.9.1 SLEEP

The Power-Down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{TO}$ bit (STATUS<4>) is set, the $\overline{PD}$ bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low or high-impedance).

| | |
|---|---|
| **Note:** | A Reset generated by a WDT time-out does not drive the $\overline{MCLR}$ pin low. |

For lowest current consumption while powered down, the T0CKI input should be at $V_{DD}$ or $V_{SS}$ and the (GP3/RB3)/$\overline{MCLR}$/$V_{PP}$ pin must be at a logic high level if $\overline{MCLR}$ is enabled.

### 7.9.2 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:

1. An external Reset input on (GP3/RB3)/$\overline{MCLR}$/$V_{PP}$ pin, when configured as $\overline{MCLR}$.
2. A Watchdog Timer time-out Reset (if WDT was enabled).
3. A change on input pin GP0/RB0, GP1/RB1, GP3/RB3 or RB4 when wake-up on change is enabled.

These events cause a device Reset. The $\overline{TO}$, $\overline{PD}$ and GPWUF/RBWUF bits can be used to determine the cause of device Reset. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up). The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked. The GPWUF/RBWUF bit indicates a change in state while in Sleep at pins GP0/RB0, GP1/RB1, GP3/RB3 or RB4 (since the last file or bit operation on GP/RB port).

| | |
|---|---|
| **Note:** | **Caution:** Right before entering Sleep, read the input pins. When in Sleep, wake-up occurs when the values at the pins change from the state they were in at the last reading. If a wake-up on change occurs and the pins are not read before re-entering Sleep, a wake-up will occur immediately even if no pins change while in Sleep mode. |

The WDT is cleared when the device wakes from Sleep, regardless of the wake-up source.

## 7.10 Program Verification/Code Protection

If the code protection bit has not been programmed, the on-chip program memory can be read out for verification purposes.

The first 64 locations and the last location (OSCCAL) can be read, regardless of the code protection bit setting.

The last memory location can be read regardless of the code protection bit setting on the PIC12F508/509/16F505 devices.

## 7.11 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during Program/Verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '0's.

## 7.12 In-Circuit Serial Programming™

The PIC12F508/509/16F505 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware, or a custom firmware, to be programmed.

The devices are placed into a Program/Verify mode by holding the GP1/RB1 and GP0/RB0 pins low while raising the $\overline{MCLR}$ ($V_{PP}$) pin from $V_{IL}$ to $V_{IHH}$ (see programming specification). GP1/RB1 becomes the programming clock and GP0/RB0 becomes the programming data. Both GP1/RB1 and GP0/RB0 are Schmitt Trigger inputs in this mode.

After Reset, a 6-bit command is then supplied to the device. Depending on the command, 14 bits of program data are then supplied to or from the device, depending if the command was a Load or a Read. For complete details of serial programming, please refer to the PIC12F508/509/16F505 Programming Specifications.

A typical In-Circuit Serial Programming connection is shown in Figure 7-15.

**RETLW** **Return with Literal in W**

Syntax: [ *label* ] RETLW k

Operands: $0 \le k \le 255$

Operation: $k \rightarrow (W)$;
$TOS \rightarrow PC$

Status Affected: None

Description: The W register is loaded with the eight-bit literal ‘k’. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

**RLF** **Rotate Left f through Carry**

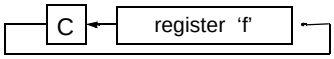
Syntax: [ *label* ] RLF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register ‘f’ are rotated one bit to the left through the Carry flag. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.




**RRF** **Rotate Right f through Carry**

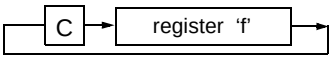
Syntax: [ *label* ] RRF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register ‘f’ are rotated one bit to the right through the Carry flag. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’.




**SLEEP** **Enter SLEEP Mode**

Syntax: [*label* ] SLEEP

Operands: None

Operation: $00h \rightarrow WDT$;
$0 \rightarrow$ WDT prescaler;
$1 \rightarrow \overline{TO}$;
$0 \rightarrow \overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$, RBWUF

Description: Time-out Status bit ($\overline{TO}$) is set. The Power-down Status bit ($\overline{PD}$) is cleared.

RBWUF is unaffected.

The WDT and its prescaler are cleared.

The processor is put into Sleep mode with the oscillator stopped. See **Section 7.9 “Power-down Mode (Sleep)”** on Sleep for more details.

**SUBWF** **Subtract W from f**

Syntax: [*label* ] SUBWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(f) - (W) \rightarrow (dest)$

Status Affected: C, DC, Z

Description: Subtract (2’s complement method) the W register from register ‘f’. If ‘d’ is ‘0’, the result is stored in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.

**SWAPF** **Swap Nibbles in f**

Syntax: [ *label* ] SWAPF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(f<3:0>) \rightarrow (dest<7:4>)$;
$(f<7:4>) \rightarrow (dest<3:0>)$

Status Affected: None

Description: The upper and lower nibbles of register ‘f’ are exchanged. If ‘d’ is ‘0’, the result is placed in W register. If ‘d’ is ‘1’, the result is placed in register ‘f’.

| TRIS | Load TRIS Register |
|---|---|
| Syntax: | [ *label* ] TRIS f |
| Operands: | f = 6 |
| Operation: | (W) → TRIS register f |
| Status Affected: | None |
| Description: | TRIS register 'f' (f = 6 or 7) is loaded with the contents of the W register |

| XORLW | Exclusive OR literal with W |
|---|---|
| Syntax: | [*label* ] XORLW k |
| Operands: | 0 ≤ k ≤ 255 |
| Operation: | (W) .XOR. k → (W) |
| Status Affected: | Z |
| Description: | The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register. |

| XORWF | Exclusive OR W with f |
|---|---|
| Syntax: | [ *label* ] XORWF f,d |
| Operands: | 0 ≤ f ≤ 31<br>d ∈ [0,1] |
| Operation: | (W) .XOR. (f) → (dest) |
| Status Affected: | Z |
| Description: | Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'. |

## 10.2 DC Characteristics: PIC12F508/509/16F505 (Extended)

| DC Characteristics | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature -40°C ≤ TA ≤ +125°C (extended) | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ(1)** | **Max.** | **Units** | **Conditions** |
| D001 | VDD | **Supply Voltage** | 2.0 | | 5.5 | V | See Figure 10-1 |
| D002 | VDR | **RAM Data Retention Voltage(2)** | — | 1.5* | — | V | Device in Sleep mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | — | Vss | — | V | See **Section 7.4 "Power-on Reset (POR)"** for details |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See **Section 7.4 "Power-on Reset (POR)"** for details |
| D010 | IDD | **Supply Current(3,4)** | —<br>— | 175<br>0.625 | 275<br>1.1 | µA<br>mA | FOSC = 4 MHz, VDD = 2.0V<br>FOSC = 4 MHz, VDD = 5.0V |
| | | | —<br>— | 500<br>1.5 | 650<br>2.2 | µA<br>mA | FOSC = 10 MHz, VDD = 3.0V<br>FOSC = 20 MHz, VDD = 5.0V<br>(PIC16F515 only) |
| | | | —<br>— | 11<br>38 | 26<br>110 | µA<br>µA | FOSC = 32 kHz, VDD = 2.0V<br>FOSC = 32 kHz, VDD = 5.0V |
| D020 | IPD | **Power-down Current(5)** | —<br>— | 0.1<br>0.35 | 9.0<br>15.0 | µA<br>µA | VDD = 2.0V<br>VDD = 5.0V |
| D022 | IWDT | **WDT Current(5)** | —<br>— | 1.0<br>7.0 | 18<br>22 | µA<br>µA | VDD = 2.0V<br>VDD = 5.0V |

* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**2:** This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

**3:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

**4:** The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VSS, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

**5:** For standby current measurements, the conditions are the same as IDD, except that the device is in Sleep mode. If a module current is listed, the current is for that specific module enabled and the device in Sleep.

**TABLE 10-6: RESET, WATCHDOG TIMER AND DEVICE RESET TIMER – PIC12F508/509/16F505**

| AC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature -40°C ≤ TA ≤ +85°C (industrial)<br>-40°C ≤ TA ≤ +125°C (extended) | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ(1)** | **Max.** | **Units** | **Conditions** |
| 30 | TMCL | $\overline{\text{MCLR}}$ Pulse Width (low) | 2000* | — | — | ns | VDD = 5.0V |
| 31 | TWDT | Watchdog Timer Time-out Period (no prescaler) | 9*<br>9* | 18*<br>18* | 30*<br>40* | ms<br>ms | VDD = 5.0V (Industrial)<br>VDD = 5.0V (Extended) |
| 32 | TDRT | Device Reset Timer Period(2) | 9*<br>9* | 18*<br>18* | 30*<br>40* | ms<br>ms | VDD = 5.0V (Industrial)<br>VDD = 5.0V (Extended) |
| 34 | TIOZ | I/O High-impedance from $\overline{\text{MCLR}}$ low | — | — | 2000* | ns | |

* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 11-2: IDD VS. FOSC OVER VDD (HS MODE, PIC16F505 only)**

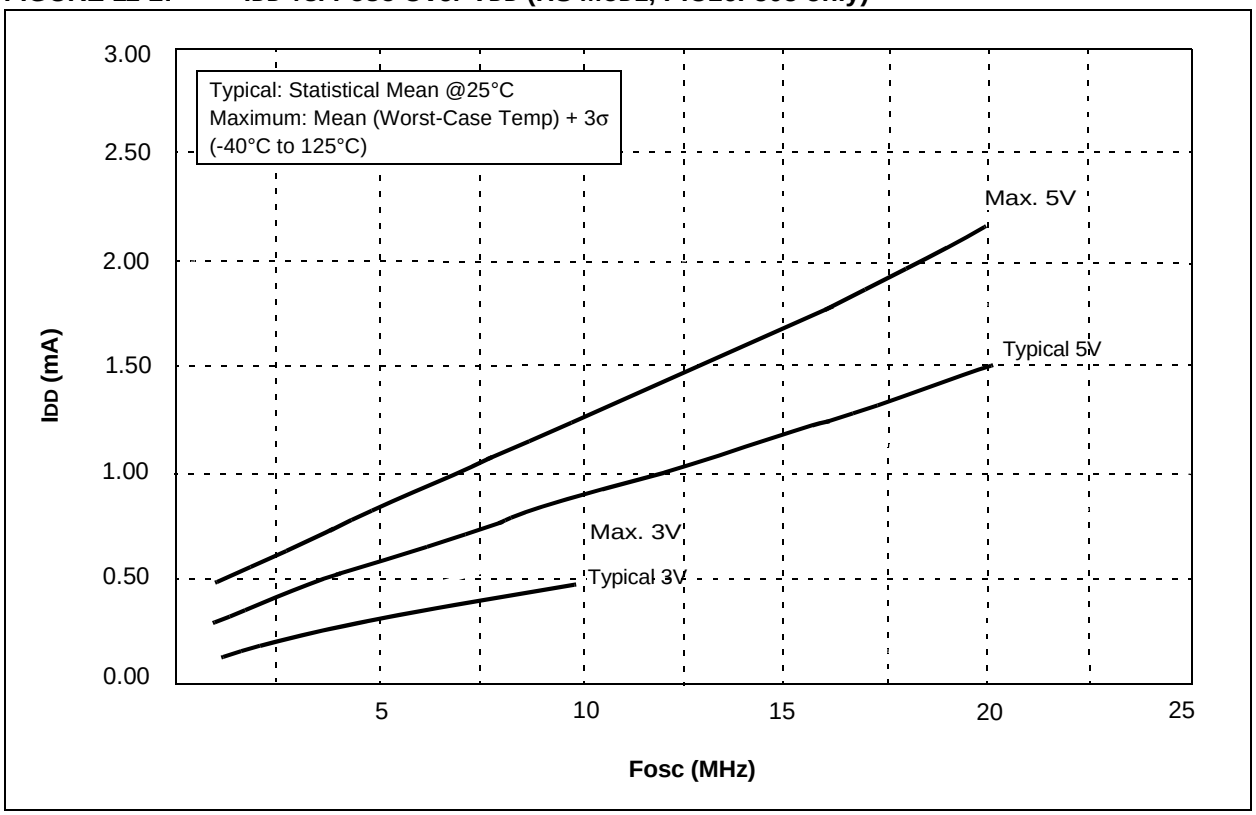
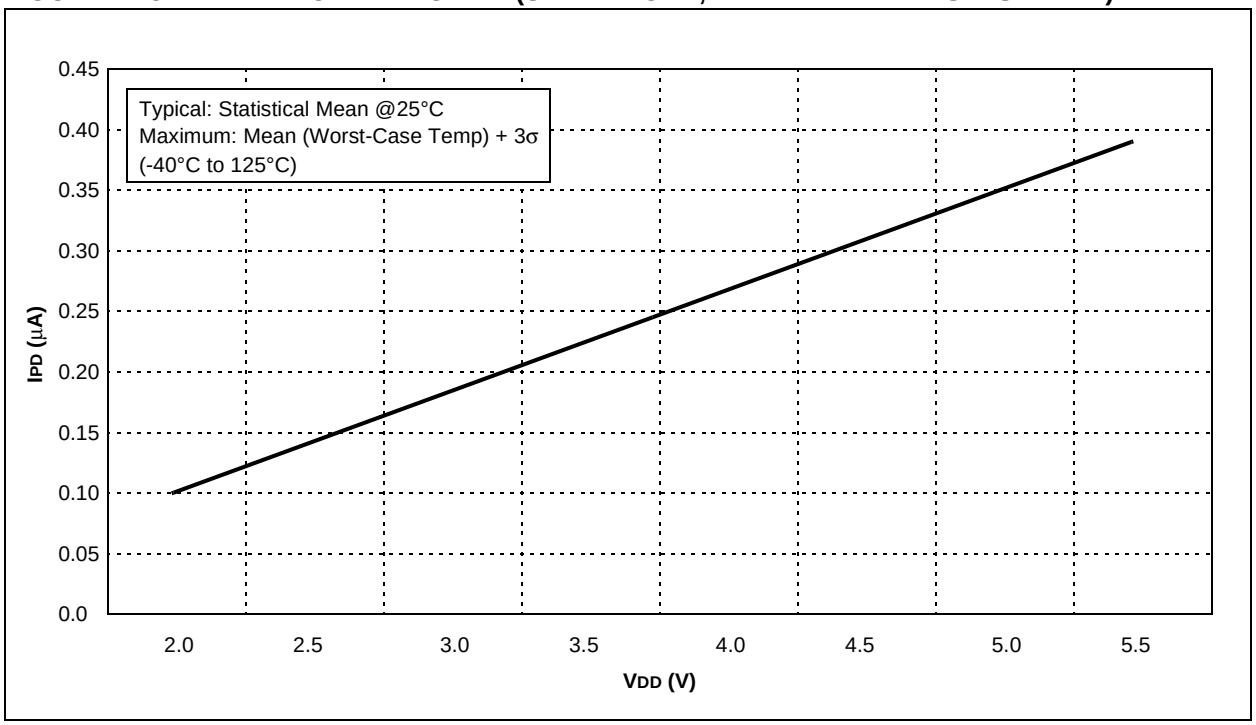
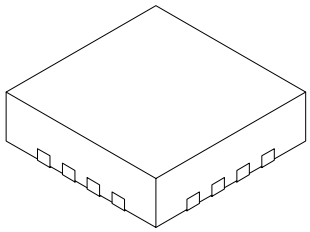



**FIGURE 11-3: TYPICAL IPD VS. VDD (SLEEP MODE, ALL PERIPHERALS DISABLED)**



### 16-Lead Plastic Quad Flat, No Lead Package (MG) - 3x3x0.9 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 16 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.85 | 0.90 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Width | E2 | 1.00 | 1.10 | 1.50 |
| Overall Length | D | | 3.00 BSC | |
| Exposed Pad Length | D2 | 1.00 | 1.10 | 1.50 |
| Contact Width | b | 0.18 | 0.25 | 0.30 |
| Contact Length | L | 0.25 | 0.35 | 0.45 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-142A Sheet 2 of 2

**NOTES:**

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