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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	768B (512 x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-TSSOP, 8-MSOP (0.118", 3.00mm Width)
Supplier Device Package	8-MSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f508-i-ms

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



8/14-Pin, 8-Bit Flash Microcontrollers

Devices Included In This Data Sheet:

• PIC12F508 • PIC12F509 • PIC16F505

High-Performance RISC CPU:

- Only 33 Single-Word Instructions to Learn
- All Single-Cycle Instructions Except for Program Branches, which are Two-Cycle
- 12-Bit Wide Instructions
- 2-Level Deep Hardware Stack
- Direct, Indirect and Relative Addressing modes for Data and Instructions
- 8-Bit Wide Data Path
- 8 Special Function Hardware Registers
- Operating Speed:
 - DC 20 MHz clock input (PIC16F505 only)
 - DC 200 ns instruction cycle (PIC16F505 only)
 - DC 4 MHz clock input
 - DC 1000 ns instruction cycle

Special Microcontroller Features:

- 4 MHz Precision Internal Oscillator:
- Factory calibrated to ±1%
- In-Circuit Serial Programming[™] (ICSP[™])
- In-Circuit Debugging (ICD) Support
- Power-On Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) with Dedicated On-Chip RC Oscillator for Reliable Operation
- Programmable Code Protection
- Multiplexed MCLR Input Pin
- Internal Weak Pull-Ups on I/O Pins
- Power-Saving Sleep mode
- Wake-Wp from Sleep on Pin Change
- Selectable Oscillator Options:
 - INTRC: 4 MHz precision Internal oscillator
 - EXTRC: External low-cost RC oscillator
 - XT: Standard crystal/resonator
 - HS: High-speed crystal/resonator (PIC16F505 only)
 - LP: Power-saving, low-frequency crystal
 - EC: High-speed external clock input (PIC16F505 only)

Low-Power Features/CMOS Technology:

- Operating Current:
 - < 175 μA @ 2V, 4 MHz, typical
- Standby Current:
 - 100 nA @ 2V, typical
- Low-Power, High-Speed Flash Technology:
 - 100,000 Flash endurance
 - > 40 year retention
- Fully Static Design
- Wide Operating Voltage Range: 2.0V to 5.5V
- Wide Temperature Range:
 - Industrial: -40°C to +85°C
 - Extended: -40°C to +125°C

Peripheral Features (PIC12F508/509):

- 6 I/O Pins:
 - 5 I/O pins with individual direction control
 - 1 input only pin
 - High current sink/source for direct LED drive
 - Wake-on-change
 - Weak pull-ups
- 8-Bit Real-Time Clock/Counter (TMR0) with 8-Bit Programmable Prescaler

Peripheral Features (PIC16F505):

- 12 I/O Pins:
 - 11 I/O pins with individual direction control
 - 1 input only pin
 - High current sink/source for direct LED drive
 - Wake-on-change
 - Weak pull-ups
- 8-Bit Real-Time Clock/Counter (TMR0) with 8-Bit Programmable Prescaler

1.0 GENERAL DESCRIPTION

The PIC12F508/509/16F505 devices from Microchip Technology are low-cost, high-performance, 8-bit, fully-static, Flash-based CMOS microcontrollers. They employ a RISC architecture with only 33 single-word/ single-cycle instructions. All instructions are single cycle (200 µs) except for program branches, which take two cycles. The PIC12F508/509/16F505 devices deliver performance an order of magnitude higher than their competitors in the same price category. The 12-bit wide instructions are highly symmetrical, resulting in a typical 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC12F508/509/16F505 products are equipped with special features that reduce system cost and power requirements. The Power-on Reset (POR) and Device Reset Timer (DRT) eliminate the need for external Reset circuitry. There are four oscillator configurations to choose from (six on the PIC16F505), including INTRC Internal Oscillator mode and the power-saving LP (Low-Power) Oscillator mode. Power-Saving Sleep mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The PIC12F508/509/16F505 devices are available in the cost-effective Flash programmable version, which is suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in Flash programmable microcontrollers, while benefiting from the Flash programmable flexibility.

The PIC12F508/509/16F505 products are supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a 'C' compiler, a low-cost development programmer and a full featured programmer. All the tools are supported on $\text{IBM}^{\textcircled{B}}$ PC and compatible machines.

1.1 Applications

The PIC12F508/509/16F505 devices fit in applications ranging from personal care appliances and security systems to low-power remote transmitters/receivers. The Flash technology makes customizing application programs (transmitter codes, appliance settings, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make these microcontrollers perfect for applications with space limitations. Low cost, low power, high performance, ease-of-use and I/O flexibility make the PIC12F508/509/16F505 devices very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, logic and PLDs in larger systems and coprocessor applications).

		PIC12F508	PIC12F509	PIC16F505
Clock	Maximum Frequency of Operation (MHz)	4	4	20
Memory	Flash Program Memory (words)	512	1024	1024
	Data Memory (bytes)	25	41	72
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0
	Wake-up from Sleep on Pin Change	Yes	Yes	Yes
Features	I/O Pins	5	5	11
	Input Pins	1	1	1
	Internal Pull-ups	Yes	Yes	Yes
	In-Circuit Serial Programming	Yes	Yes	Yes
	Number of Instructions	33	33	33
	Packages	8-pin PDIP, SOIC, MSOP, DFN	8-pin PDIP, SOIC, MSOP, DFN	14-pin PDIP, SOIC, TSSOP

TABLE 1-1: PIC12F508/509/16F505 DEVICES

The PIC12F508/509/16F505 devices have Power-on Reset, selectable Watchdog Timer, selectable code-protect, high I/O current capability and precision internal oscillator.

The PIC12F508/509/16F505 devices use serial programming with data pin RB0/GP0 and clock pin RB1/GP1.

Nama	Eurotion	Input	Output	Description	
Name	Function	Туре	Туре	Description	
GP0/ICSPDAT	GP0	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal	
				weak pull-up and wake-up from Sleep on pin change.	
	ICSPDAT	ST	CMOS	In-Circuit Serial Programming™ data pin.	
GP1/ICSPCLK	GP1	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.	
	ICSPCLK	ST	CMOS	In-Circuit Serial Programming clock pin.	
GP2/T0CKI	GP2	TTL	CMOS	Bidirectional I/O pin.	
	TOCKI	ST	—	Clock input to TMR0.	
GP3/MCLR/Vpp	GP3	TTL	—	Input pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.	
	MCLR	ST	_	Master Clear (Reset). When configured as MCLR, this pin is an active-low Reset to the device. Voltage on MCLR/VPP must not exceed VDD during normal device operation or the device will enter Programming mode. Weak pull-up always on if configured as MCLR.	
	Vpp	ΗV	—	Programming voltage input.	
GP4/OSC2	GP4	TTL	CMOS	Bidirectional I/O pin.	
	OSC2	_	XTAL	Oscillator crystal output. Connections to crystal or resonator in Crystal Oscillator mode (XT and LP modes only, GPIO in other modes).	
GP5/OSC1/CLKIN	GP5	TTL	CMOS	Bidirectional I/O pin.	
	OSC1	XTAL	_	Oscillator crystal input.	
	CLKIN	ST	—	External clock source input.	
Vdd	Vdd	—	Р	Positive supply for logic and I/O pins.	
Vss	Vss		Р	Ground reference for logic and I/O pins.	

TABLE 3-2:	PIC12F508/509 PINOUT DESCRIP	NOIT

Legend: I = Input, O = Output, I/O = Input/Output, P = Power, — = Not used, TTL = TTL input, ST = Schmitt Trigger input, HV = High Voltage



3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the PC is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-3 and Example 3-1.

3.2 Instruction Flow/Pipelining

An instruction cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute take another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the PC to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the PC incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).



FIGURE 3-3: CLOCK/INSTRUCTION CYCLE

EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



All instructions are single cycle, except for any program branches. These take two cycles, since the fetch instruction is "flushed" from the pipeline, while the new instruction is being fetched and then executed.

4.7 **Program Counter**

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

For a GOTO instruction, bits 8:0 of the PC are provided by the GOTO instruction word. The Program Counter (PCL) is mapped to PC<7:0>. Bit 5 of the STATUS register provides page information to bit 9 of the PC (Figure 4-6).

For a CALL instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-6).

Instructions where the PCL is the destination, or modify PCL instructions, include MOVWF PC, ADDWF PC and BSF PC, 5.

Note: Because PC<8> is cleared in the CALL instruction or any modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-6: LOADING OF PC BRANCH INSTRUCTIONS



4.7.1 EFFECTS OF RESET

The PC is set upon a Reset, which means that the PC addresses the last location in the last page (i.e., the oscillator calibration instruction). After executing MOVLW XX, the PC will roll over to location 00h and begin executing user code.

The STATUS register page preselect bits are cleared upon a Reset, which means that page 0 is pre-selected.

Therefore, upon a Reset, a GOTO instruction will automatically cause the program to jump to page 0 until the value of the page bits is altered.

4.8 Stack

The PIC12F508/509/16F505 devices have a 2-deep, 12-bit wide hardware PUSH/POP stack.

A CALL instruction will PUSH the current value of Stack 1 into Stack 2 and then PUSH the current PC value, incremented by one, into Stack Level 1. If more than two sequential CALLs are executed, only the most recent two return addresses are stored.

A RETLW instruction will POP the contents of Stack Level 1 into the PC and then copy Stack Level 2 contents into Stack Level 1. If more than two sequential RETLWS are executed, the stack will be filled with the address previously stored in Stack Level 2. Note that the W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

Note 1:	There are no Status bits to indicate stack								
	overflo	ws or	stad	ck underflow	conditions.				
2:	There	are	no	instruction	mnemonics				

called PUSH or POP. These are actions that occur from the execution of the CALL and RETLW instructions.

NOTES:

REGISTER 7-1: CONFIGURATION WORD FOR PIC12F508/509⁽¹⁾

—	—	—	—	—	—	—	MCLRE	CP	WDTE	FOSC1	FOSC0
bit 11									-		bit 0
Legend:	Legend:										
R = Read	dable bit		W = Writa	able bit		U = Unin	nplemented	l bit, rea	d as '0'		
-n = Valu	e at POR		'1' = Bit is	s set		'0' = Bit i	s cleared		x = Bit is	unknown	
bit 11-5	Unimple	mented: F	Read as '0	,							
bit 4	MCLRE:	GP3/MCL	R Pin Fun	ction Sele	ect bit						
	1 = GP3/	MCLR pin	function is	MCLR							
	0 = GP3/	MCLR pin	function is	s digital in	put, MCL	R internal	ly tied to V	DD			
bit 3	CP: Code	e Protectic	on bit								
	1 = Code	protection	n off								
	0 = Code	protection	n on								
bit 2	WDTE: Watchdog Timer Enable bit										
	1 = WDT enabled										
	0 = WDI disabled										
bit 1-0	FOSC<1:0>: Oscillator Selection bits										
	11 = EXIKU = EXTERNAL KU OSCIIIATOR 10 - INTRC - internal RC oscillator										
	01 = XT oscillator										
	00 = LP o	oscillator									
Note 1:	Refer to access t	the " <i>PIC1</i> the Config	2 <i>F508/50</i> 9 uration Wo	9 <i>Memory</i> ord. The C	<i>Program</i> Configurat	<i>ming Spe</i> ion Word	<i>cifications</i> " is not user	(DS412) address	27) to dete able during	ermine hov g device o	v to peration.

TABLE 7-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR – PIC12F508/509/16F505⁽²⁾

Osc Type	Resonator Freq.	esonator Cap. Range C Freq. C1					
LP	32 kHz ⁽¹⁾	32 kHz ⁽¹⁾ 15 pF 15 pF					
ХТ	200 kHz 1 MHz 4 MHz	47-68 pF 15 pF 15 pF	47-68 pF 15 pF 15 pF				
HS ⁽³⁾	20 MHz	15-47 pF	15-47 pF				
Note 1:	For VDD > 4.5V, C1 = C2 \approx 30 pF is recommended.						
2:	These values are for design guidance only. Rs may be required to avoid over- driving crystals with low drive level specifi- cation. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.						
1 3:	PIC16F505 only.						

7.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator or a simple oscillator circuit with TTL gates can be used as an external crystal oscillator circuit. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with parallel resonance, or one with series resonance.

Figure 7-3 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 k Ω resistor provides the negative feedback for stability. The 10 k Ω potentiometers bias the 74AS04 in the linear region. This circuit could be used for external oscillator designs.

FIGURE 7-3:

EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT



Figure 7-4 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 Ω resistors provide the negative feedback to bias the inverters in their linear region.



EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



7.2.4 EXTERNAL RC OSCILLATOR

For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit-to-unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used.

Figure 7-5 shows how the R/C combination is connected to the PIC12F508/509/16F505 devices. For REXT values below 3.0 k Ω , the oscillator operation may become unstable, or stop completely. For very high REXT values (e.g., 1 M Ω), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping REXT between 5.0 k Ω and 100 k Ω .

FIGURE 7-15: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



Increment f

INCF

DECF	Decrement f
Syntax:	[label] DECF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in \ [0,1] \end{array}$
Operation:	$(f) - 1 \rightarrow (dest)$
Status Affected:	Z
Description:	Decrement register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

Decrement f, Skip if 0

[label] DECFSZ f,d

(f) $-1 \rightarrow d$; skip if result = 0

The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in

If the result is '0', the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle

 $\begin{array}{l} 0 \leq f \leq 31 \\ d \in \ [0,1] \end{array}$

None

register 'f'.

instruction.

DECFSZ

Operands:

Operation:

Description:

Status Affected:

Syntax:

Syntax:	[<i>label</i>] INCF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in \ [0,1] \end{array}$
Operation:	(f) + 1 \rightarrow (dest)
Status Affected:	Z
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.
INCFSZ	Increment f, Skip if 0
Syntax:	[label] INCFSZ f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in \ [0,1] \end{array}$
Operation:	(f) + 1 \rightarrow (dest), skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.
	If the result is '0', then the next instruction, which is already

GOTO	Unconditional Branch
Syntax:	[<i>label</i>] GOTO k
Operands:	$0 \le k \le 511$
Operation:	$k \rightarrow PC < 8:0>;$ STATUS<6:5> $\rightarrow PC < 10:9>$
Status Affected:	None
Description:	GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS<6:5>. GOTO is a two- cycle instruction.

IORLW	Inclusive OR literal with W						
Syntax:	[<i>label</i>] IORLW k						
Operands:	$0 \le k \le 255$						
Operation:	(W) .OR. (k) \rightarrow (W)						
Status Affected:	Z						
Description:	The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.						

9.2 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for all PIC MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline
 assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

9.3 MPLAB C18 and MPLAB C30 C Compilers

The MPLAB C18 and MPLAB C30 Code Development Systems are complete ANSI C compilers for Microchip's PIC18 and PIC24 families of microcontrollers and the dsPIC30 and dsPIC33 family of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

9.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

9.5 MPLAB ASM30 Assembler, Linker and Librarian

MPLAB ASM30 Assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

9.6 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC[®] DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C18 and MPLAB C30 C Compilers, and the MPASM and MPLAB ASM30 Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

10.2 DC Characteristics: PIC12F508/509/16F505 (Extended)

DC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ (extended)					
Param No.	Sym.	Characteristic	Min.	Typ ⁽¹⁾	Max.	Units	Conditions
D001	Vdd	Supply Voltage	2.0		5.5	V	See Figure 10-1
D002	Vdr	RAM Data Retention Voltage ⁽²⁾	_	1.5*	—	V	Device in Sleep mode
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	Vss	—	V	See Section 7.4 "Power-on Reset (POR)" for details
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 7.4 "Power-on Reset (POR)" for details
D010	IDD	Supply Current ^(3,4)	-	175 0.625	275 1.1	μA mA	Fosc = 4 MHz, VDD = 2.0V Fosc = 4 MHz, VDD = 5.0V
			_	500 1.5	650 2.2	μA mA	Fosc = 10 MHz, VDD = 3.0V Fosc = 20 MHz, VDD = 5.0V (PIC16F515 only)
			_	11 38	26 110	μΑ μΑ	Fosc = 32 kHz, VDD = 2.0V Fosc = 32 kHz, VDD = 5.0V
D020	IPD	Power-down Current ⁽⁵⁾	—	0.1	9.0	μA	VDD = 2.0V
			—	0.35	15.0	μA	VDD = 5.0V
D022	Iwdt	WDT Current ⁽⁵⁾	— —	1.0 7.0	18 22	μΑ μΑ	VDD = 2.0V VDD = 5.0V

These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- 2: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.
- **3:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
- 4: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
- 5: For standby current measurements, the conditions are the same as IDD, except that the device is in Sleep mode. If a module current is listed, the current is for that specific module enabled and the device in Sleep.



FIGURE 11-2: IDD VS. FOSC Over VDD (HS MODE, PIC16F505 only)













the case of other types of Reset events.









12.1 Package Marking Information (Continued)

14-Lead PDIP (300 mil)	Example	
	PIC16F505) -I/P €3 0215 ○ ☎ 0610017	

14-Lead SOIC (3.90 mm)



Example	
PIC16F505-E	
/SLU125	
W 0610017	

14-Lead TSSOP (4.4 mm)



Example

16F	505-I	
\mathbf{v}	0610	
-	017	

16-Lead QFN



Example



TABLE 12-1: 8-LEAD 2X3 DFN (MC) TOP MARKING

Part Number	Marking
PIC12F508 (T) - I/MC	BN0
PIC12F508-E/MC	BP0
PIC12F509 (T) - I/MC	BQ0
PIC12F509-E/MC	BR0

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	С		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

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