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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	5
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	41 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	8-TSSOP, 8-MSOP (0.118", 3.00mm Width)
Supplier Device Package	8-MSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f509-e-ms

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1.0 GENERAL DESCRIPTION

The PIC12F508/509/16F505 devices from Microchip Technology are low-cost, high-performance, 8-bit, fully-static, Flash-based CMOS microcontrollers. They employ a RISC architecture with only 33 single-word/ single-cycle instructions. All instructions are single cycle (200 µs) except for program branches, which take two cycles. The PIC12F508/509/16F505 devices deliver performance an order of magnitude higher than their competitors in the same price category. The 12-bit wide instructions are highly symmetrical, resulting in a typical 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC12F508/509/16F505 products are equipped with special features that reduce system cost and power requirements. The Power-on Reset (POR) and Device Reset Timer (DRT) eliminate the need for external Reset circuitry. There are four oscillator configurations to choose from (six on the PIC16F505), including INTRC Internal Oscillator mode and the power-saving LP (Low-Power) Oscillator mode. Power-Saving Sleep mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The PIC12F508/509/16F505 devices are available in the cost-effective Flash programmable version, which is suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in Flash programmable microcontrollers, while benefiting from the Flash programmable flexibility.

The PIC12F508/509/16F505 products are supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a 'C' compiler, a low-cost development programmer and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

1.1 Applications

The PIC12F508/509/16F505 devices fit in applications ranging from personal care appliances and security systems to low-power remote transmitters/receivers. The Flash technology makes customizing application programs (transmitter codes, appliance settings, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make these microcontrollers perfect for applications with space limitations. Low cost, low power, high performance, ease-of-use and I/O flexibility make the PIC12F508/509/16F505 devices very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, logic and PLDs in larger systems and coprocessor applications).

TABLE 1-1: PIC12F508/509/16F505 DEVICES

		PIC12F508	PIC12F509	PIC16F505
Clock	Maximum Frequency of Operation (MHz)	4	4	20
Memory	Flash Program Memory (words)	512	1024	1024
	Data Memory (bytes)	25	41	72
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0
	Wake-up from Sleep on Pin Change	Yes	Yes	Yes
Features	I/O Pins	5	5	11
	Input Pins	1	1	1
	Internal Pull-ups	Yes	Yes	Yes
	In-Circuit Serial Programming	Yes	Yes	Yes
	Number of Instructions	33	33	33
	Packages	8-pin PDIP, SOIC, MSOP, DFN	8-pin PDIP, SOIC, MSOP, DFN	14-pin PDIP, SOIC, TSSOP

The PIC12F508/509/16F505 devices have Power-on Reset, selectable Watchdog Timer, selectable code-protect, high I/O current capability and precision internal oscillator.
The PIC12F508/509/16F505 devices use serial programming with data pin RB0/GP0 and clock pin RB1/GP1.

NOTES:

FIGURE 3-2: PIC16F505 BLOCK DIAGRAM

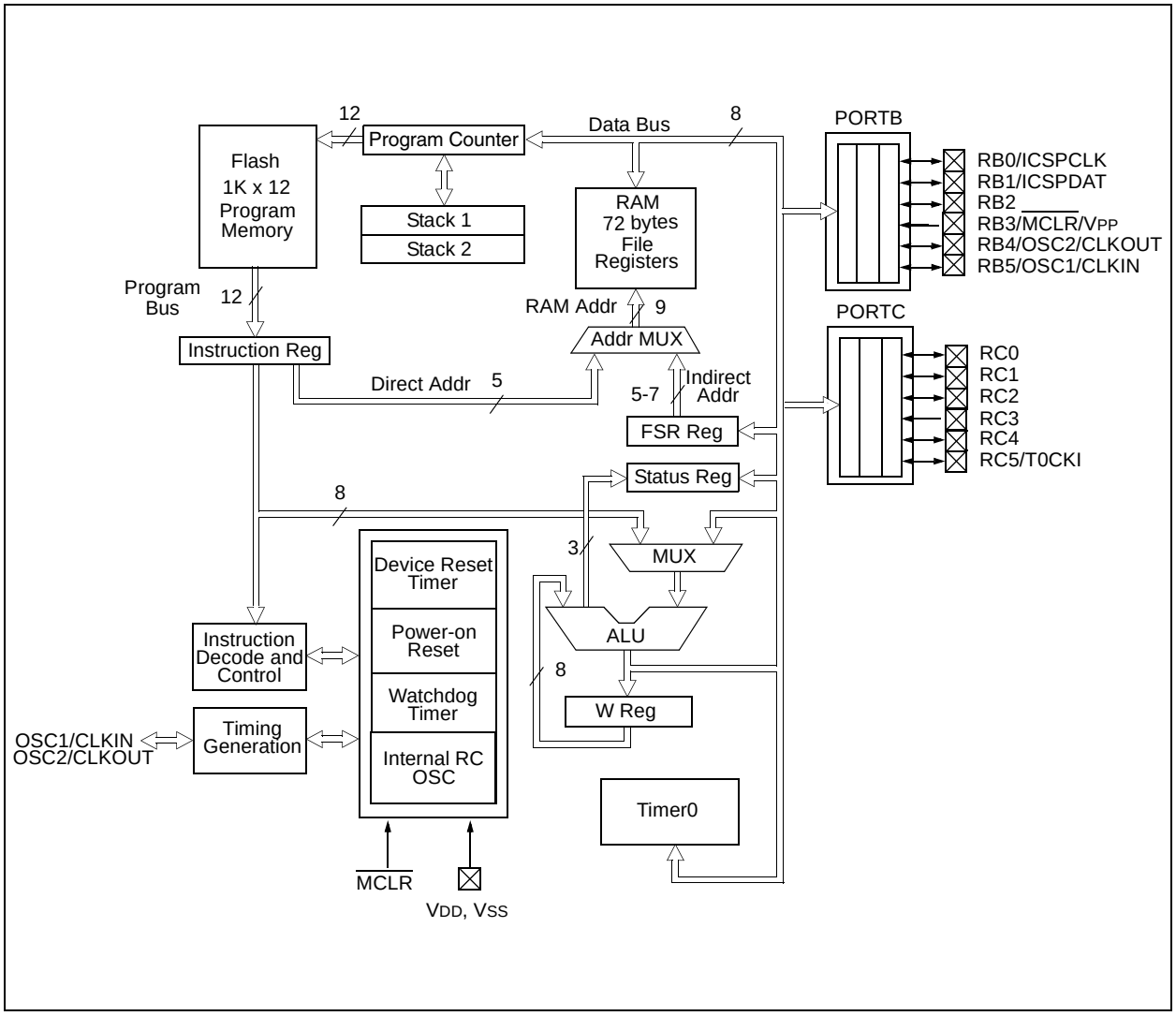


TABLE 3-3: PIC16F505 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RB0/ICSPDAT	RB0	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	ICSPDAT	ST	CMOS	In-Circuit Serial Programming™ data pin.
RB1/ICSPCLK	RB1	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	ICSPCLK	ST	CMOS	In-Circuit Serial Programming clock pin.
RB2	RB2	TTL	CMOS	Bidirectional I/O pin.
RB3/$\overline{\text{MCLR}}$/V_{PP}	RB3	TTL	—	Input port. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	$\overline{\text{MCLR}}$	ST	—	Master Clear (Reset). When configured as $\overline{\text{MCLR}}$, this pin is an active-low Reset to the device. Voltage on $\overline{\text{MCLR}}$/V_{PP} must not exceed V_{DD} during normal device operation or the device will enter Programming mode. Weak pull-up always on if configured as $\overline{\text{MCLR}}$.
	V_{PP}	HV	—	Programming voltage input.
RB4/OSC2/CLKOUT	RB4	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	OSC2	—	XTAL	Oscillator crystal output. Connections to crystal or resonator in Crystal Oscillator mode (XT, HS and LP modes only).
	CLKOUT	—	CMOS	In EXTRC and INTRC modes, the pin output can be configured for CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RB5/OSC1/CLKIN	RB5	TTL	CMOS	Bidirectional I/O pin.
	OSC1	XTAL	—	Crystal input.
	CLKIN	ST	—	External clock source input.
RC0	RC0	TTL	CMOS	Bidirectional I/O pin.
RC1	RC1	TTL	CMOS	Bidirectional I/O pin.
RC2	RC2	TTL	CMOS	Bidirectional I/O pin.
RC3	RC3	TTL	CMOS	Bidirectional I/O pin.
RC4	RC4	TTL	CMOS	Bidirectional I/O pin.
RC5/T0CKI	RC5	TTL	CMOS	Bidirectional I/O pin.
	T0CKI	ST	—	Clock input to TMR0.
V_{DD}	V_{DD}	—	P	Positive supply for logic and I/O pins.
V_{SS}	V_{SS}	—	P	Ground reference for logic and I/O pins.

Legend: I = Input, O = Output, I/O = Input/Output, P = Power, — = Not used, TTL = TTL input, ST = Schmitt Trigger input, HV = High Voltage

4.3.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions to control the operation of the device (Table 4-1).

The Special Function Registers can be classified into two sets. The Special Function Registers associated with the “core” functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

TABLE 4-1: SPECIAL FUNCTION REGISTER (SFR) SUMMARY (PIC12F508/509)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset(2)	Page #
00h	INDF	Uses Contents of FSR to Address Data Memory (not a physical register)								xxxx xxxx	28
01h	TMR0	8-bit Real-Time Clock/Counter								xxxx xxxx	35
02h(1)	PCL	Low-order 8 bits of PC								1111 1111	27
03h	STATUS	GPWUF	—	PA0(5)	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0-01 1xxx(3)	22
04h	FSR	Indirect Data Memory Address Pointer								111x xxxx	28
04h(4)	FSR	Indirect Data Memory Address Pointer								110x xxxx	28
05h	OSCCAL	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	1111 111-	26
06h	GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	31
N/A	TRISGPIO	—	—	I/O Control Register						--11 1111	31
N/A	OPTION	$\overline{GPWU}$	$\overline{GPPU}$	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	24

Legend: – = unimplemented, read as ‘0’, x = unknown, u = unchanged, q = value depends on condition.

Note 1: The upper byte of the Program Counter is not directly accessible. See **Section 4.7 “Program Counter”** for an explanation of how to access these bits.

2: Other (non Power-up) Resets include external Reset through $\overline{MCLR}$, Watchdog Timer and wake-up on pin change Reset.

3: If Reset was due to wake-up on pin change, then bit 7 = 1. All other Resets will cause bit 7 = 0.

4: PIC12F509 only.

5: This bit is used on the PIC12F509. For code compatibility do not use this bit on the PIC12F508.

TABLE 4-2: SPECIAL FUNCTION REGISTER (SFR) SUMMARY (PIC16F505)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset(2)	Page #
00h	INDF	Uses Contents of FSR to Address Data Memory (not a physical register)								xxxx xxxx	28
01h	TMR0	8-bit Real-Time Clock/Counter								xxxx xxxx	35
02h(1)	PCL	Low-order 8 bits of PC								1111 1111	27
03h	STATUS	RBWUF	—	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0-01 1xxx	22
04h	FSR	Indirect Data Memory Address Pointer								100x xxxx	28
05h	OSCCAL	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	1111 111-	26
06h	PORTB	—	—	RB5	RB4	RB3	RB2	RB1	RB0	--xx xxxx	31
07h	PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xxxx	31
N/A	TRISB	—	—	I/O Control Register						--11 1111	31
N/A	TRISC	—	—	I/O Control Register						--11 1111	31
N/A	OPTION	$\overline{RBWU}$	$\overline{RBPU}$	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	25

Legend: – = unimplemented, read as '0', x = unknown, u = unchanged, q = value depends on condition.

Note 1: If Reset was due to wake-up on pin change, then bit 7 = 1. All other Resets will cause bit 7 = 0.

2: Other (non Power-up) Resets include external reset through $\overline{MCLR}$, Watchdog Timer and wake-up on pin change Reset.

NOTES:

TABLE 5-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
N/A	TRISGPIO(1)	—	—	I/O Control Register						--11 1111	--11 1111
N/A	TRISB(2)	—	—	I/O Control Register						--11 1111	--11 1111
N/A	TRISC(2)	—	—	I/O Control Register						--11 1111	--11 1111
N/A	OPTION(1)	$\overline{\text{GPWU}}$	$\overline{\text{GPPU}}$	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
N/A	OPTION(2)	$\overline{\text{RBWU}}$	$\overline{\text{RBPU}}$	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
03h	STATUS(1)	GPWUF	—	PAO	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0-01 1xxx	q00q quuu(3)
03h	STATUS(2)	RBWUF	—	PAO	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0-01 1xxx	q00q quuu(3)
06h	GPIO(1)	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	--uu uuuu
06h	PORTB(2)	—	—	RB5	RB4	RB3	RB2	RB1	RB0	--xx xxxx	--uu uuuu
07h	PORTC(2)	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xxxx	--uu uuuu

Legend: Shaded cells are not used by Port registers, read as '0'. – = unimplemented, read as '0', x = unknown, u = unchanged, q = depends on condition.

Note 1: PIC12F508/509 only.

2: PIC16F505 only.

3: If Reset was due to wake-up on pin change, then bit 7 = 1. All other Resets will cause bit 7 = 0.

FIGURE 7-7: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

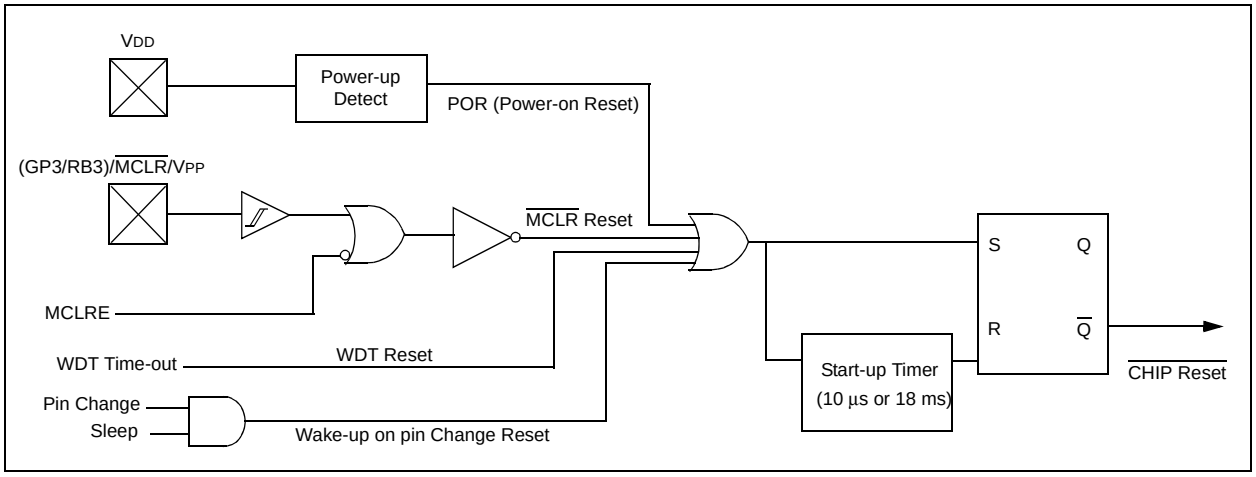


FIGURE 7-8: TIME-OUT SEQUENCE ON POWER-UP (MCLR PULLED LOW)

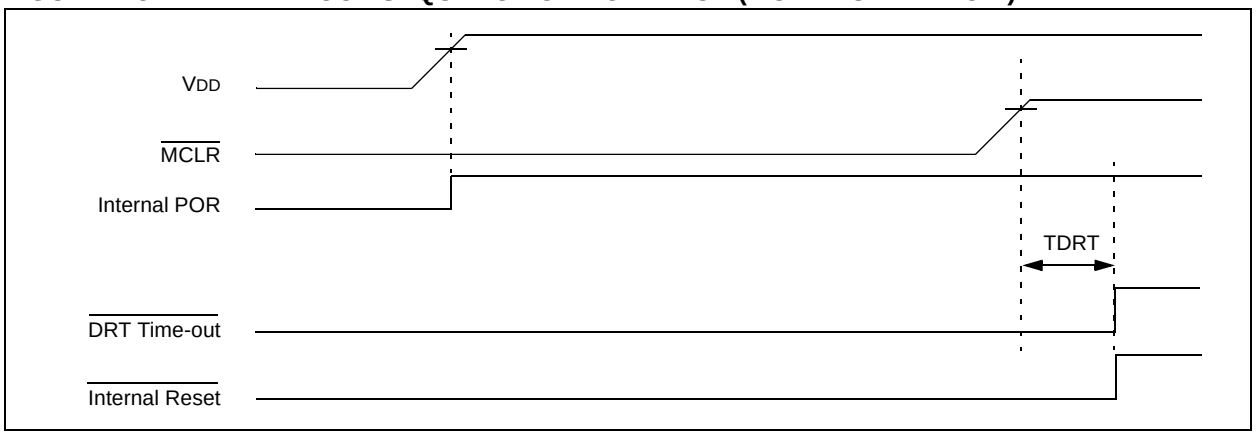


FIGURE 7-9: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): FAST VDD RISE TIME

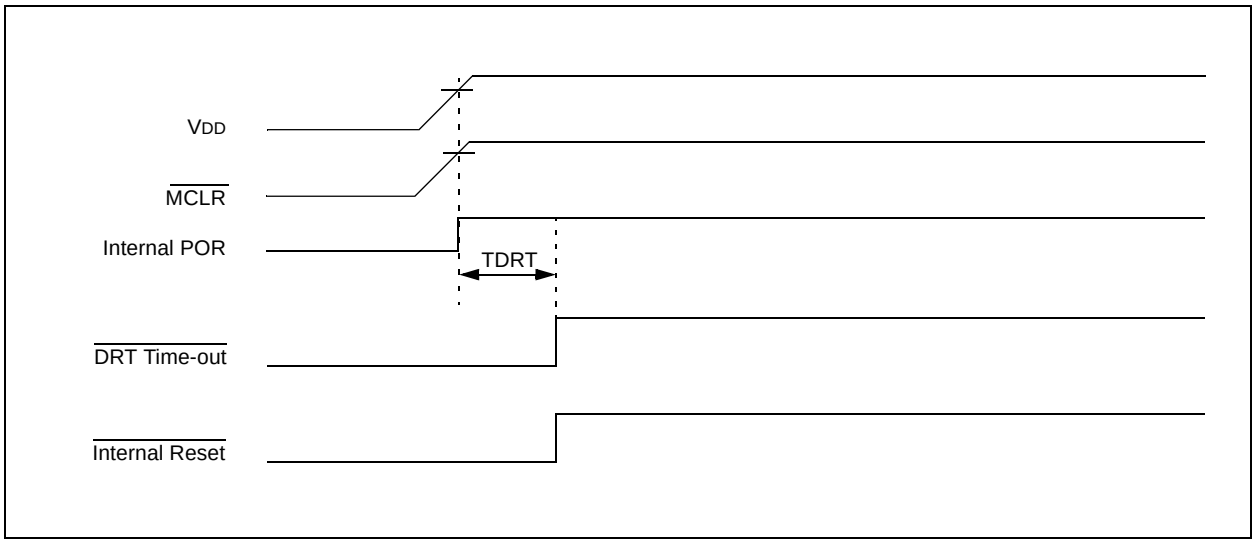
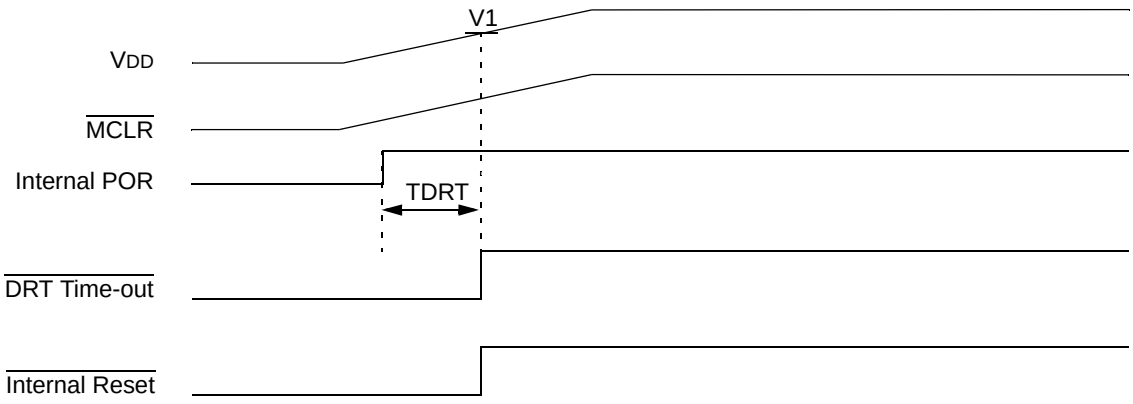


FIGURE 7-10: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD}): SLOW V_{DD} RISE TIME



Note: When V_{DD} rises slowly, the T_{DRT} time-out expires long before V_{DD} has reached its final value. In this example, the chip will reset properly if, and only if, V1 ≥ V_{DD} min.

7.7 Time-out Sequence, Power-down and Wake-up from Sleep Status Bits (TO, PD, GPWUF/RBWUF)

The $\overline{TO}$, $\overline{PD}$ and (GPWUF/RBWUF) bits in the STATUS register can be tested to determine if a Reset condition has been caused by a Power-up condition, a $\overline{MCLR}$ or Watchdog Timer (WDT) Reset.

TABLE 7-8: $\overline{TO}$/$\overline{PD}$/(GPWUF/RBWUF) STATUS AFTER RESET

GPWUF/ RBWUF	$\overline{TO}$	$\overline{PD}$	Reset Caused By
0	0	0	WDT wake-up from Sleep
0	0	u	WDT time-out (not from Sleep)
0	1	0	$\overline{MCLR}$ wake-up from Sleep
0	1	1	Power-up
0	u	u	$\overline{MCLR}$ not during Sleep
1	1	0	Wake-up from Sleep on pin change

Legend: u = unchanged

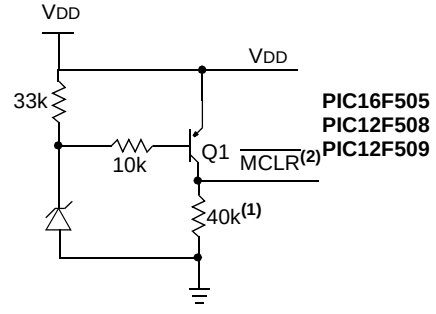
Note 1: The $\overline{TO}$, $\overline{PD}$ and GPWUF/RBWUF bits maintain their status (u) until a Reset occurs. A low-pulse on the $\overline{MCLR}$ input does not change the $\overline{TO}$, $\overline{PD}$ and GPWUF/RBWUF Status bits.

7.8 Reset on Brown-out

A brown-out is a condition where device power (V_{DD}) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

To reset PIC12F508/509/16F505 devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 7-12 and Figure 7-13.

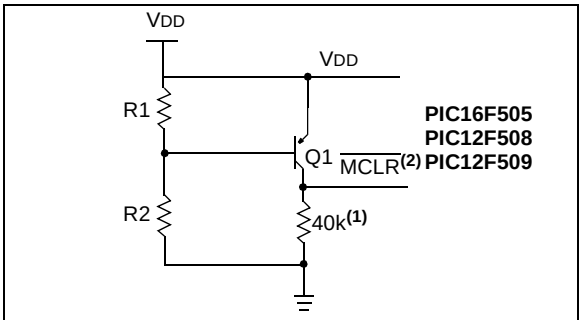
FIGURE 7-12: BROWN-OUT PROTECTION CIRCUIT 1



Note 1: This circuit will activate Reset when V_{DD} goes below Vz + 0.7V (where Vz = Zener voltage).

2: Pin must be confirmed as $\overline{MCLR}$.

FIGURE 7-13: BROWN-OUT PROTECTION CIRCUIT 2

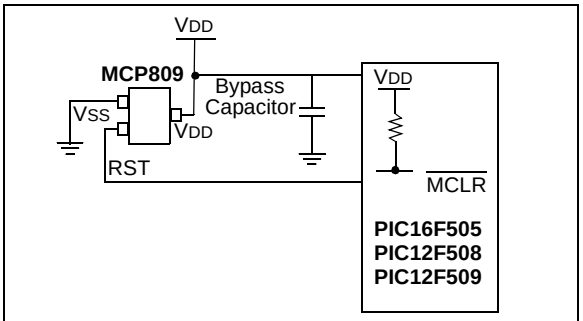


Note 1: This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when V_{DD} is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V$$

2: Pin must be confirmed as $\overline{MCLR}$.

FIGURE 7-14: BROWN-OUT PROTECTION CIRCUIT 3



Note: This brown-out protection circuit employs Microchip Technology's MCP809 micro-controller supervisor. There are 7 different trip point selections to accommodate 5V to 3V systems.

FIGURE 7-15: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION

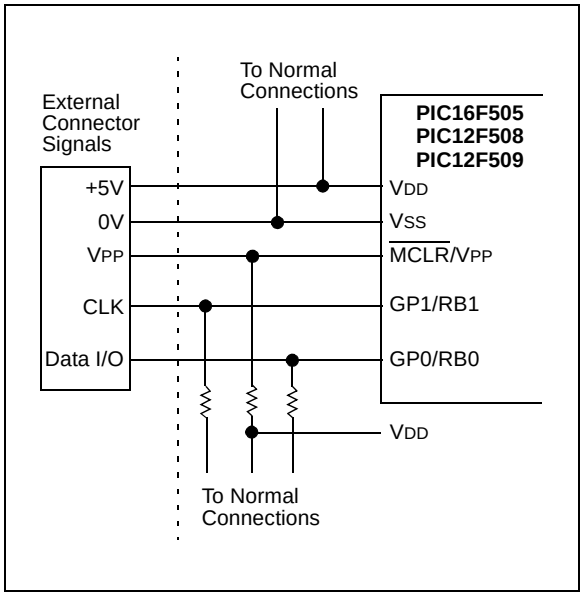


TABLE 8-2: INSTRUCTION SET SUMMARY

Mnemonic, Operands		Description	Cycles	12-Bit Opcode			Status Affected	Notes
				MSb		LSb		
ADDWF	f, d	Add W and f	1	0001	11df	ffff	C, DC, Z	**1, 2, 4**
ANDWF	f, d	AND W with f	1	0001	01df	ffff	Z	**2, 4**
CLRF	f	Clear f	1	0000	011f	ffff	Z	**4**
CLRW	—	Clear W	1	0000	0100	0000	Z	
COMF	f, d	Complement f	1	0010	01df	ffff	Z	
DECF	f, d	Decrement f	1	0000	11df	ffff	Z	**2, 4**
DECFSZ	f, d	Decrement f, Skip if 0	1**(2)**	0010	11df	ffff	None	**2, 4**
INCF	f, d	Increment f	1	0010	10df	ffff	Z	**2, 4**
INCFSZ	f, d	Increment f, Skip if 0	1**(2)**	0011	11df	ffff	None	**2, 4**
IORWF	f, d	Inclusive OR W with f	1	0001	00df	ffff	Z	**2, 4**
MOVF	f, d	Move f	1	0010	00df	ffff	Z	**2, 4**
MOVWF	f	Move W to f	1	0000	001f	ffff	None	**1, 4**
NOP	—	No Operation	1	0000	0000	0000	None	
RLF	f, d	Rotate left f through Carry	1	0011	01df	ffff	C	**2, 4**
RRF	f, d	Rotate right f through Carry	1	0011	00df	ffff	C	**2, 4**
SUBWF	f, d	Subtract W from f	1	0000	10df	ffff	C, DC, Z	**1, 2, 4**
SWAPF	f, d	Swap f	1	0011	10df	ffff	None	**2, 4**
XORWF	f, d	Exclusive OR W with f	1	0001	10df	ffff	Z	**2, 4**
BIT-ORIENTED FILE REGISTER OPERATIONS								
BCF	f, b	Bit Clear f	1	0100	bbbf	ffff	None	**2, 4**
BSF	f, b	Bit Set f	1	0101	bbbf	ffff	None	**2, 4**
BTFSC	f, b	Bit Test f, Skip if Clear	1**(2)**	0110	bbbf	ffff	None	
BTFSS	f, b	Bit Test f, Skip if Set	1**(2)**	0111	bbbf	ffff	None	
LITERAL AND CONTROL OPERATIONS								
ANDLW	k	AND literal with W	1	1110	kkkk	kkkk	Z	
CALL	k	Call Subroutine	2	1001	kkkk	kkkk	None	**1**
CLRWDT	—	Clear Watchdog Timer	1	0000	0000	0100	$\overline{TO}$, $\overline{PD}$	
GOTO	k	Unconditional branch	2	101k	kkkk	kkkk	None	
IORLW	k	Inclusive OR literal with W	1	1101	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	1100	kkkk	kkkk	None	
OPTION	—	Load OPTION register	1	0000	0000	0010	None	
RETLW	k	Return, place literal in W	2	1000	kkkk	kkkk	None	
SLEEP	—	Go into Standby mode	1	0000	0000	0011	$\overline{TO}$, $\overline{PD}$	
TRIS	f	Load TRIS register	1	0000	0000	0fff	None	**3**
XORLW	k	Exclusive OR literal to W	1	1111	kkkk	kkkk	Z	

Note 1: The 9th bit of the program counter will be forced to a '0' by any instruction that writes to the PC except for GOTO. See **Section 4.7 "Program Counter"**.

2: When an I/O register is modified as a function of itself (e.g. MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

3: The instruction TRIS f, where f = 6, causes the contents of the W register to be written to the tri-state latches of PORTB. A '1' forces the pin to a high-impedance state and disables the output buffers.

4: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared (if assigned to TMR0).

IORWF	Inclusive OR W with f
Syntax:	[*label*] IORWF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(W).OR. (f) → (dest)
Status Affected:	Z
Description:	Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

MOVF	Move f
Syntax:	[*label*] MOVF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(f) → (dest)
Status Affected:	Z
Description:	The contents of register 'f' are moved to destination 'd'. If 'd' is '0', destination is the W register. If 'd' is '1', the destination is file register 'f'. 'd' = 1 is useful as a test of a file register, since status flag Z is affected.

MOVLW	Move Literal to W
Syntax:	[*label*] MOVLW k
Operands:	$0 \le k \le 255$
Operation:	k → (W)
Status Affected:	None
Description:	The eight-bit literal 'k' is loaded into the W register. The "don't cares" will assembled as '0's.

MOVWF	Move W to f
Syntax:	[*label*] MOVWF f
Operands:	$0 \le f \le 31$
Operation:	(W) → (f)
Status Affected:	None
Description:	Move data from the W register to register 'f'.

NOP	No Operation
Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.

OPTION	Load OPTION Register
Syntax:	[*label*] OPTION
Operands:	None
Operation:	(W) → OPTION
Status Affected:	None
Description:	The content of the W register is loaded into the OPTION register.

FIGURE 10-1: PIC12F508/509/16F505 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C

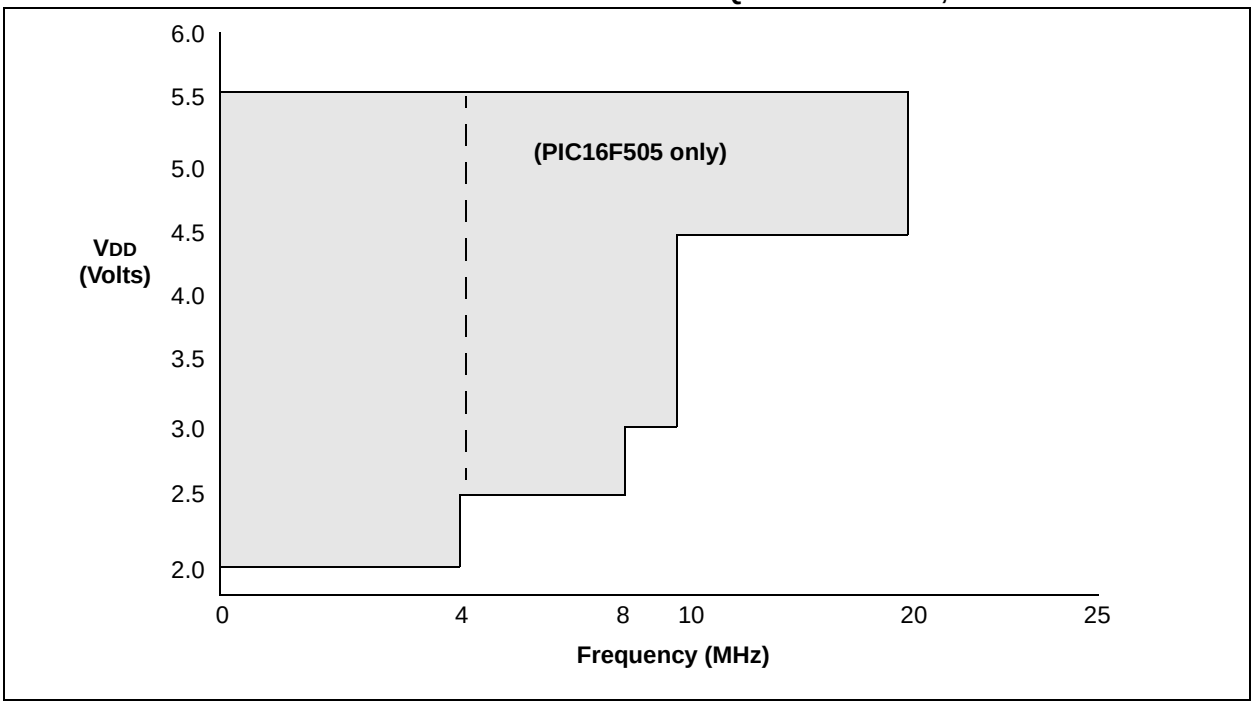
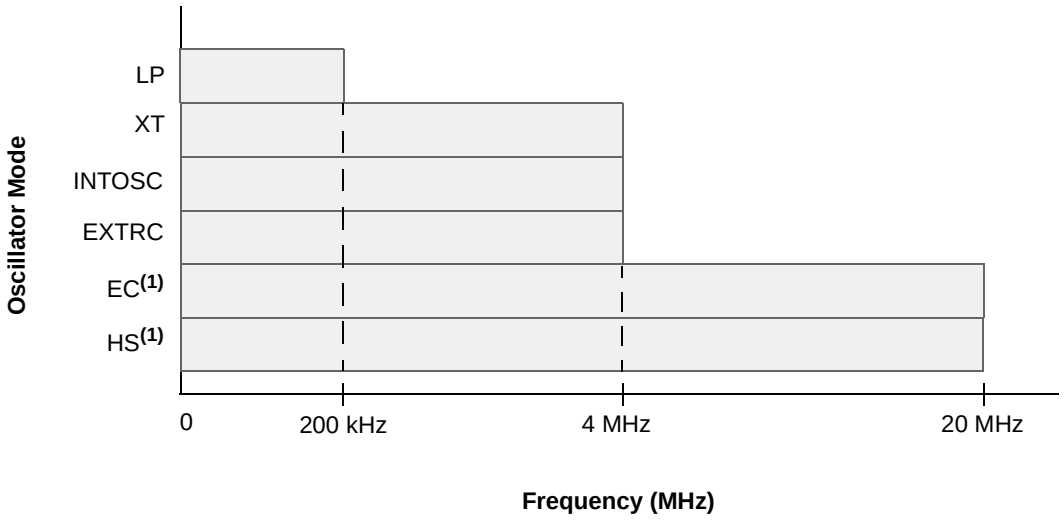


FIGURE 10-2: MAXIMUM OSCILLATOR FREQUENCY TABLE



Note 1: For PIC16F505 only.

TABLE 10-1: DC CHARACTERISTICS: PIC12F508/509/16F505 (Industrial, Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating temperature -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended) Operating voltage VDD range as described in DC specification				
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
		I/O ports:					
D030		with TTL buffer	Vss	—	0.8V	V	For all 4.5 ≤ VDD ≤ 5.5V
D030A			Vss	—	0.15 VDD	V	Otherwise
D031		with Schmitt Trigger buffer	Vss	—	0.15 VDD	V	
D032		$\overline{MCLR}$, T0CKI	Vss	—	0.15 VDD	V	
D033		OSC1 (in EXTRC)	Vss	—	0.15 VDD	V	**(Note1)**
D033		OSC1 (in HS)	Vss	—	0.3 VDD	V	**(Note1)**
D033		OSC1 (in XT and LP)	Vss	—	0.3	V	**(Note1)**
	VIH	**Input High Voltage**					
		I/O ports:		—			
D040		with TTL buffer	2.0	—	VDD	V	4.5 ≤ VDD ≤ 5.5V
D040A			0.25 VDD + 0.8	—	VDD	V	Otherwise
D041		with Schmitt Trigger buffer	0.85 VDD	—	VDD	V	For entire VDD range
D042		MCLR, T0CKI	0.85 VDD	—	VDD	V	
D043		OSC1 (in EXTRC)	0.85 VDD	—	VDD	V	**(Note1)**
D043		OSC1 (in HS)	0.7 VDD	—	VDD	V	**(Note1)**
D043		OSC1 (in XT and LP)	1.6	—	VDD	V	
D070	IPUR	**GPIO/PORTB weak pull-up current(4)**	50	250	400	µA	VDD = 5V, VPIN = VSS
	IIL	**Input Leakage Current(2), (3)**					
D060		I/O ports	—	—	± 1	µA	Vss ≤ VPIN ≤ VDD, Pin at high-impedance
D061		GP3/RB3/$\overline{MCLR}$I(5)	—	± 0.7	± 5	µA	Vss ≤ VPIN ≤ VDD
D063		OSC1	—	—	± 5	µA	Vss ≤ VPIN ≤ VDD, XT, HS and LP oscillator configuration
		Output Low Voltage					
D080		I/O ports/CLKOUT	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D080A			—	—	0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
D083		OSC2	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
D083A			—	—	0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C
		Output High Voltage					
D090		I/O ports/CLKOUT(3)	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D090A			VDD – 0.7	—	—	V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
D092		OSC2	VDD – 0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D092A			VDD – 0.7	—	—	V	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C
		Capacitive Loading Specs on Output Pins					
D100		OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101		All I/O pins and OSC2	—	—	50	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12F508/509/16F505 be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

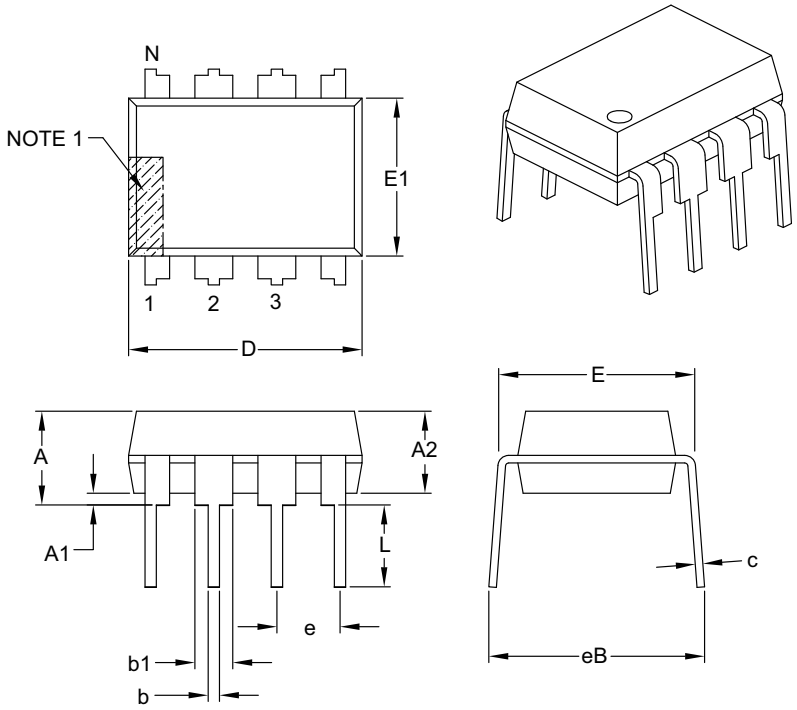
3: Negative current is defined as coming out of the pin.

4: The specification applies to all weak pull-up devices, including the weak pull-up on GP3/$\overline{MCLR}$. The current listed will be the same whether GP3/$\overline{MCLR}$ is configured as GP3 with a weak pull-up or enabled as $\overline{MCLR}$.

5: This specification applies when GP3/RB3/$\overline{MCLR}$ is configured as an input with pull-up disabled. The leakage current of the $\overline{MCLR}$ circuit is higher than the standard I/O logic.

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

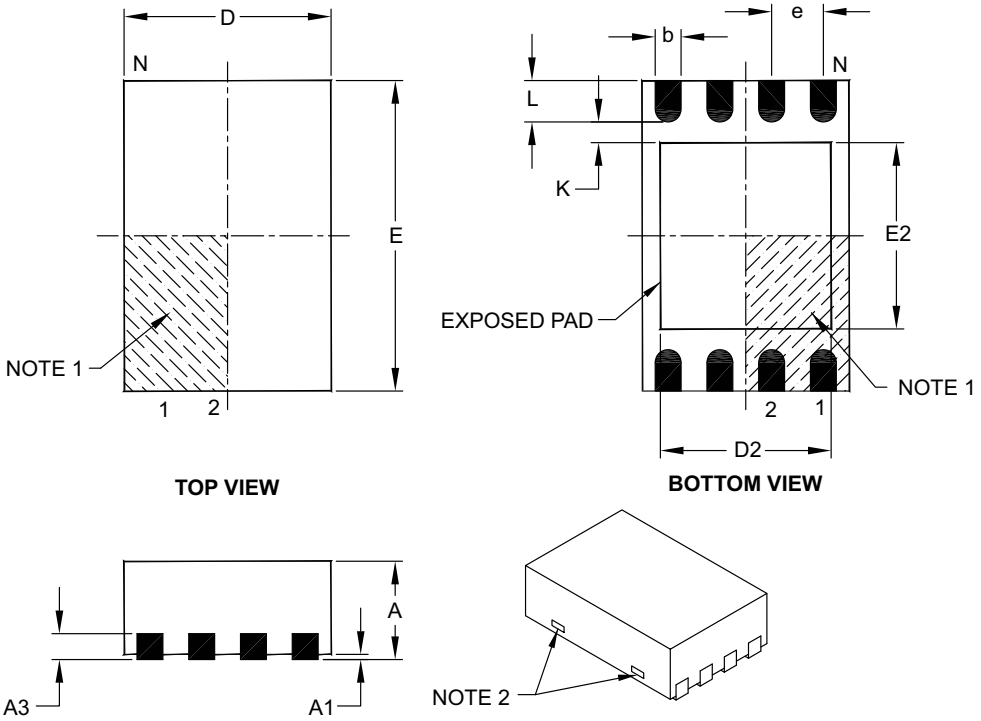
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.30	–	1.55
Exposed Pad Width	E2	1.50	–	1.75
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

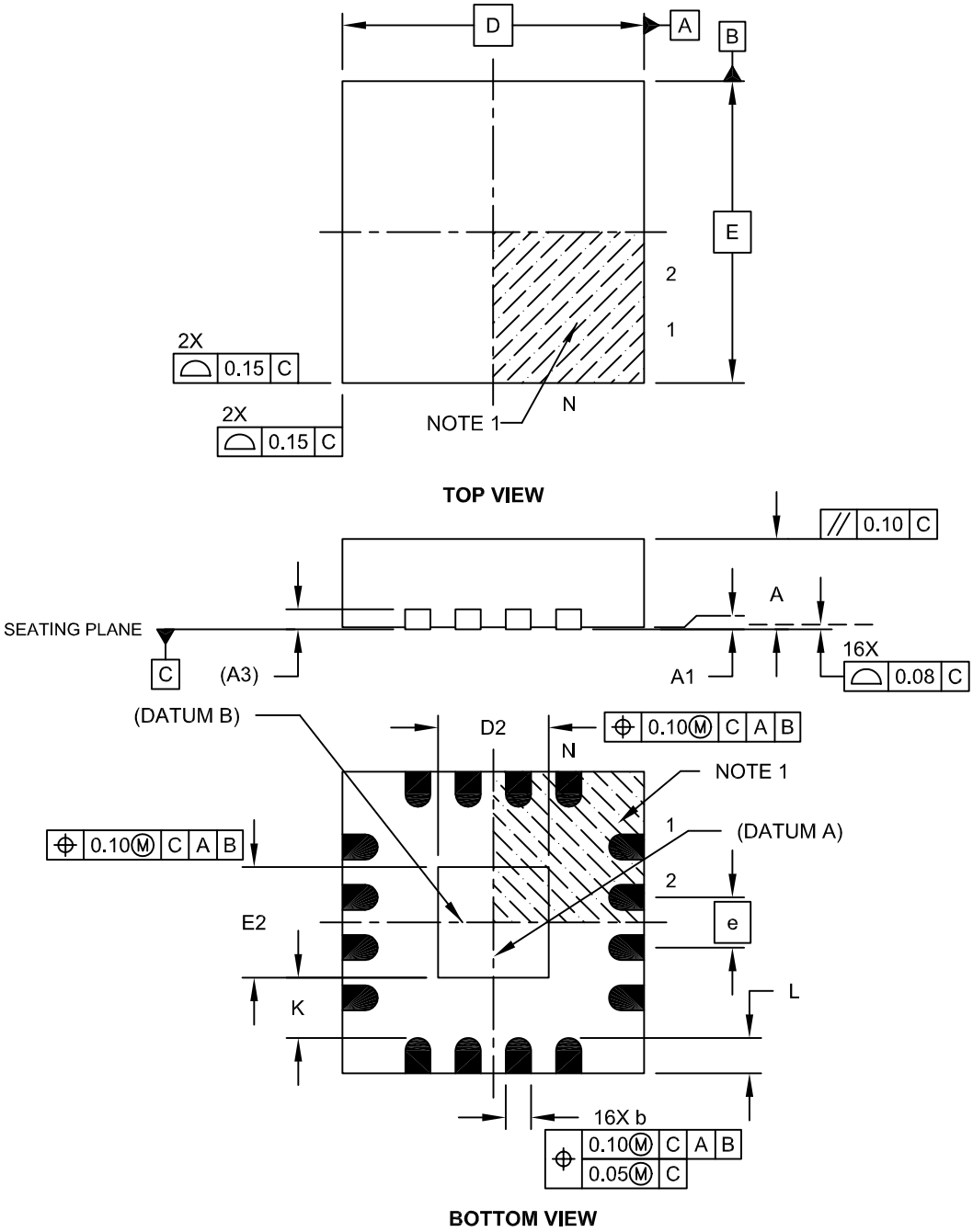
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123C

16-Lead Plastic Quad Flat, No Lead Package (MG) - 3x3x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-142A Sheet 1 of 2