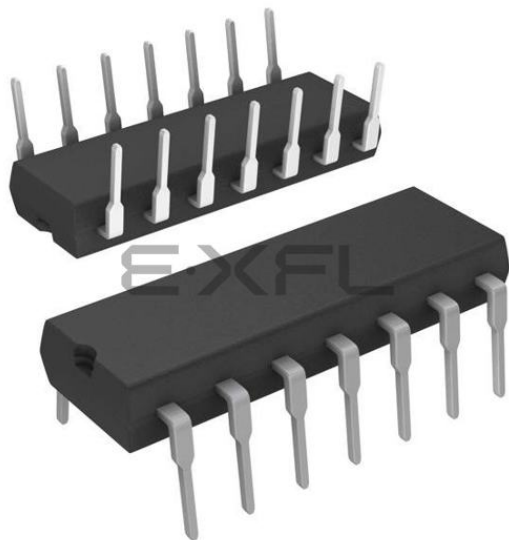




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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	11
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	14-DIP (0.300", 7.62mm)
Supplier Device Package	14-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f505-e-p



PIC12F508/509/16F505

8/14-Pin, 8-Bit Flash Microcontrollers

Devices Included In This Data Sheet:

- PIC12F508
- PIC12F509
- PIC16F505

High-Performance RISC CPU:

- Only 33 Single-Word Instructions to Learn
- All Single-Cycle Instructions Except for Program Branches, which are Two-Cycle
- 12-Bit Wide Instructions
- 2-Level Deep Hardware Stack
- Direct, Indirect and Relative Addressing modes for Data and Instructions
- 8-Bit Wide Data Path
- 8 Special Function Hardware Registers
- Operating Speed:
 - DC – 20 MHz clock input (PIC16F505 only)
 - DC – 200 ns instruction cycle (PIC16F505 only)
 - DC – 4 MHz clock input
 - DC – 1000 ns instruction cycle

Special Microcontroller Features:

- 4 MHz Precision Internal Oscillator:
 - Factory calibrated to $\pm 1\%$
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Debugging (ICD) Support
- Power-On Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) with Dedicated On-Chip RC Oscillator for Reliable Operation
- Programmable Code Protection
- Multiplexed MCLR Input Pin
- Internal Weak Pull-Ups on I/O Pins
- Power-Saving Sleep mode
- Wake-Up from Sleep on Pin Change
- Selectable Oscillator Options:
 - INTRC: 4 MHz precision Internal oscillator
 - EXTRC: External low-cost RC oscillator
 - XT: Standard crystal/resonator
 - HS: High-speed crystal/resonator (PIC16F505 only)
 - LP: Power-saving, low-frequency crystal
 - EC: High-speed external clock input (PIC16F505 only)

Low-Power Features/CMOS Technology:

- Operating Current:
 - $< 175 \mu\text{A}$ @ 2V, 4 MHz, typical
- Standby Current:
 - 100 nA @ 2V, typical
- Low-Power, High-Speed Flash Technology:
 - 100,000 Flash endurance
 - > 40 year retention
- Fully Static Design
- Wide Operating Voltage Range: 2.0V to 5.5V
- Wide Temperature Range:
 - Industrial: -40°C to $+85^{\circ}\text{C}$
 - Extended: -40°C to $+125^{\circ}\text{C}$

Peripheral Features (PIC12F508/509):

- 6 I/O Pins:
 - 5 I/O pins with individual direction control
 - 1 input only pin
 - High current sink/source for direct LED drive
 - Wake-on-change
 - Weak pull-ups
- 8-Bit Real-Time Clock/Counter (TMR0) with 8-Bit Programmable Prescaler

Peripheral Features (PIC16F505):

- 12 I/O Pins:
 - 11 I/O pins with individual direction control
 - 1 input only pin
 - High current sink/source for direct LED drive
 - Wake-on-change
 - Weak pull-ups
- 8-Bit Real-Time Clock/Counter (TMR0) with 8-Bit Programmable Prescaler

PIC12F508/509/16F505

1.0 GENERAL DESCRIPTION

The PIC12F508/509/16F505 devices from Microchip Technology are low-cost, high-performance, 8-bit, fully-static, Flash-based CMOS microcontrollers. They employ a RISC architecture with only 33 single-word/single-cycle instructions. All instructions are single cycle (200 μ s) except for program branches, which take two cycles. The PIC12F508/509/16F505 devices deliver performance an order of magnitude higher than their competitors in the same price category. The 12-bit wide instructions are highly symmetrical, resulting in a typical 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC12F508/509/16F505 products are equipped with special features that reduce system cost and power requirements. The Power-on Reset (POR) and Device Reset Timer (DRT) eliminate the need for external Reset circuitry. There are four oscillator configurations to choose from (six on the PIC16F505), including INTRC Internal Oscillator mode and the power-saving LP (Low-Power) Oscillator mode. Power-Saving Sleep mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The PIC12F508/509/16F505 devices are available in the cost-effective Flash programmable version, which is suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in Flash programmable microcontrollers, while benefiting from the Flash programmable flexibility.

The PIC12F508/509/16F505 products are supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a 'C' compiler, a low-cost development programmer and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

1.1 Applications

The PIC12F508/509/16F505 devices fit in applications ranging from personal care appliances and security systems to low-power remote transmitters/receivers. The Flash technology makes customizing application programs (transmitter codes, appliance settings, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make these microcontrollers perfect for applications with space limitations. Low cost, low power, high performance, ease-of-use and I/O flexibility make the PIC12F508/509/16F505 devices very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, logic and PLDs in larger systems and coprocessor applications).

TABLE 1-1: PIC12F508/509/16F505 DEVICES

		PIC12F508	PIC12F509	PIC16F505
Clock	Maximum Frequency of Operation (MHz)	4	4	20
Memory	Flash Program Memory (words)	512	1024	1024
	Data Memory (bytes)	25	41	72
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0
	Wake-up from Sleep on Pin Change	Yes	Yes	Yes
Features	I/O Pins	5	5	11
	Input Pins	1	1	1
	Internal Pull-ups	Yes	Yes	Yes
	In-Circuit Serial Programming	Yes	Yes	Yes
	Number of Instructions	33	33	33
	Packages	8-pin PDIP, SOIC, MSOP, DFN	8-pin PDIP, SOIC, MSOP, DFN	14-pin PDIP, SOIC, TSSOP

The PIC12F508/509/16F505 devices have Power-on Reset, selectable Watchdog Timer, selectable code-protect, high I/O current capability and precision internal oscillator.

The PIC12F508/509/16F505 devices use serial programming with data pin RB0/GP0 and clock pin RB1/GP1.

PIC12F508/509/16F505

3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the PC is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-3 and Example 3-1.

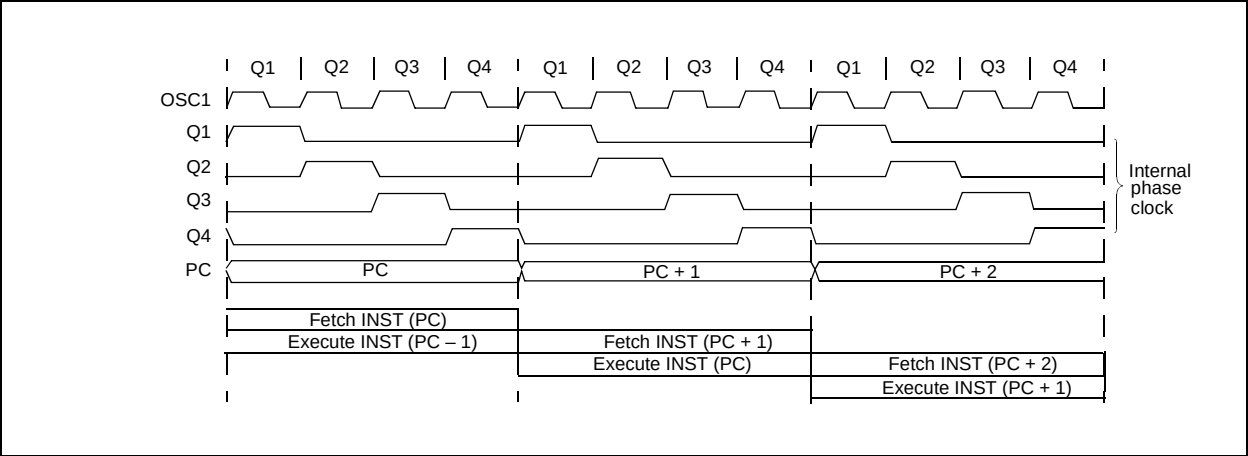
3.2 Instruction Flow/Pipelining

An instruction cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute take another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the PC to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 3-1).

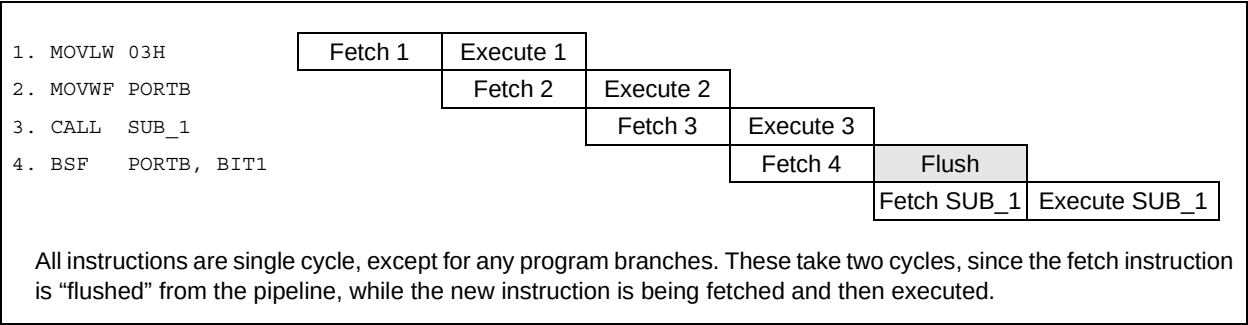
A fetch cycle begins with the PC incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-3: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



PIC12F508/509/16F505

REGISTER 4-2: STATUS REGISTER (ADDRESS: 03h) (PIC16F505)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
RBWUF	—	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7	RBWUF: PORTB Reset bit 1 = Reset due to wake-up from Sleep on pin change 0 = After power-up or other Reset
bit 6	Reserved: Do not use
bit 5	PA0: Program Page Preselect bits 1 = Page 1 (200h-3FFh) 0 = Page 0 (000h-1FFh) Each page is 512 bytes. Using the PA0 bit as a general purpose read/write bit in devices which do not use it for program page preselect is not recommended, since this may affect upward compatibility with future products.
bit 4	$\overline{TO}$: Time-Out bit 1 = After power-up, CLRWDT instruction, or SLEEP instruction 0 = A WDT time-out occurred
bit 3	$\overline{PD}$: Power-Down bit 1 = After power-up or by the CLRWDT instruction 0 = By execution of the SLEEP instruction
bit 2	Z: Zero bit 1 = The result of an arithmetic or logic operation is zero 0 = The result of an arithmetic or logic operation is not zero
bit 1	DC: Digit Carry/Borrow bit (for ADDWF and SUBWF instructions) <u>ADDWF:</u> 1 = A carry from the 4th low-order bit of the result occurred 0 = A carry from the 4th low-order bit of the result did not occur <u>SUBWF:</u> 1 = A borrow from the 4th low-order bit of the result did not occur 0 = A borrow from the 4th low-order bit of the result occurred
bit 0	C: Carry/Borrow bit (for ADDWF, SUBWF and RRF, RLF instructions) <u>ADDWF:</u> <u>SUBWF:</u> <u>RRF or RLF:</u> 1 = A carry occurred 1 = A borrow did not occur Load bit with LSb or MSb, respectively 0 = A carry did not occur 0 = A borrow occurred

4.7 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

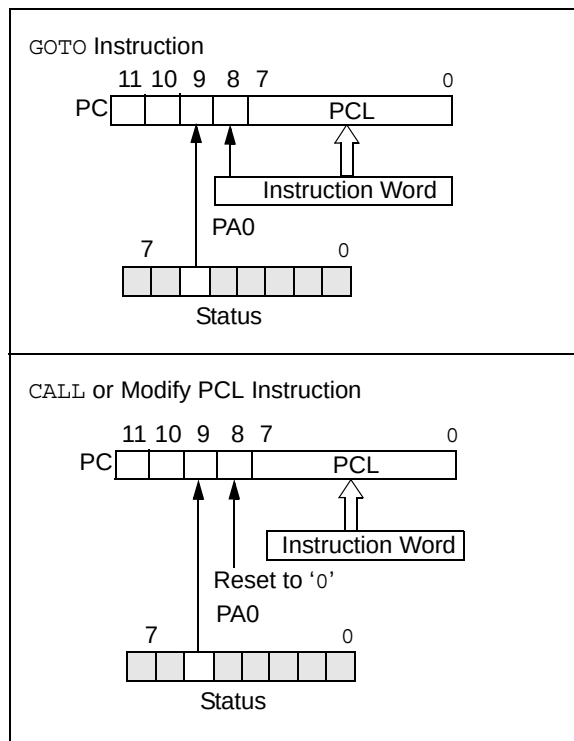
For a **GOTO** instruction, bits 8:0 of the PC are provided by the **GOTO** instruction word. The Program Counter (PCL) is mapped to PC<7:0>. Bit 5 of the STATUS register provides page information to bit 9 of the PC (Figure 4-6).

For a **CALL** instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-6).

Instructions where the PCL is the destination, or modify PCL instructions, include **MOVWF PC**, **ADDWF PC** and **BSF PC, 5**.

Note: Because PC<8> is cleared in the **CALL** instruction or any modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-6: LOADING OF PC BRANCH INSTRUCTIONS



4.7.1 EFFECTS OF RESET

The PC is set upon a Reset, which means that the PC addresses the last location in the last page (i.e., the oscillator calibration instruction). After executing **MOVLW XX**, the PC will roll over to location 00h and begin executing user code.

The STATUS register page preselect bits are cleared upon a Reset, which means that page 0 is pre-selected.

Therefore, upon a Reset, a **GOTO** instruction will automatically cause the program to jump to page 0 until the value of the page bits is altered.

4.8 Stack

The PIC12F508/509/16F505 devices have a 2-deep, 12-bit wide hardware PUSH/POP stack.

A **CALL** instruction will **PUSH** the current value of Stack 1 into Stack 2 and then **PUSH** the current PC value, incremented by one, into Stack Level 1. If more than two sequential **CALL**s are executed, only the most recent two return addresses are stored.

A **RETLW** instruction will **POP** the contents of Stack Level 1 into the PC and then copy Stack Level 2 contents into Stack Level 1. If more than two sequential **RETLW**s are executed, the stack will be filled with the address previously stored in Stack Level 2. Note that the W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

Note 1: There are no Status bits to indicate stack overflows or stack underflow conditions.

2: There are no instruction mnemonics called **PUSH** or **POP**. These are actions that occur from the execution of the **CALL** and **RETLW** instructions.

PIC12F508/509/16F505

4.9 Indirect Data Addressing: INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

4.9.1 INDIRECT ADDRESSING

- Register file 07 contains the value 10h
- Register file 08 contains the value 0Ah
- Load the value 07 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 08)
- A read of the INDF register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 4-1.

EXAMPLE 4-1: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```

        MOVLW 0x10    ;initialize pointer
        MOVWF FSR     ;to RAM
NEXT    CLRF  INDF    ;clear INDF
        ;register
        INCF  FSR,F   ;inc pointer
        BTFSC FSR,4   ;all done?
        GOTO  NEXT    ;NO, clear next
CONTINUE
        :             ;YES, continue
        :
    
```

The FSR is a 5-bit wide register. It is used in conjunction with the INDF register to indirectly address the data memory area.

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

PIC12F508 – Does not use banking. FSR <7:5> are unimplemented and read as '1's.

PIC12F509 – Uses FSR<5>. Selects between bank 0 and bank 1. FSR<7:6> are unimplemented, read as '1'.

PIC16F505 – Uses FSR<6:5>. Selects from bank 0 to bank 3. FSR<7> is unimplemented, read as '1'.

FIGURE 4-7: DIRECT/INDIRECT ADDRESSING (PIC12F508/509)

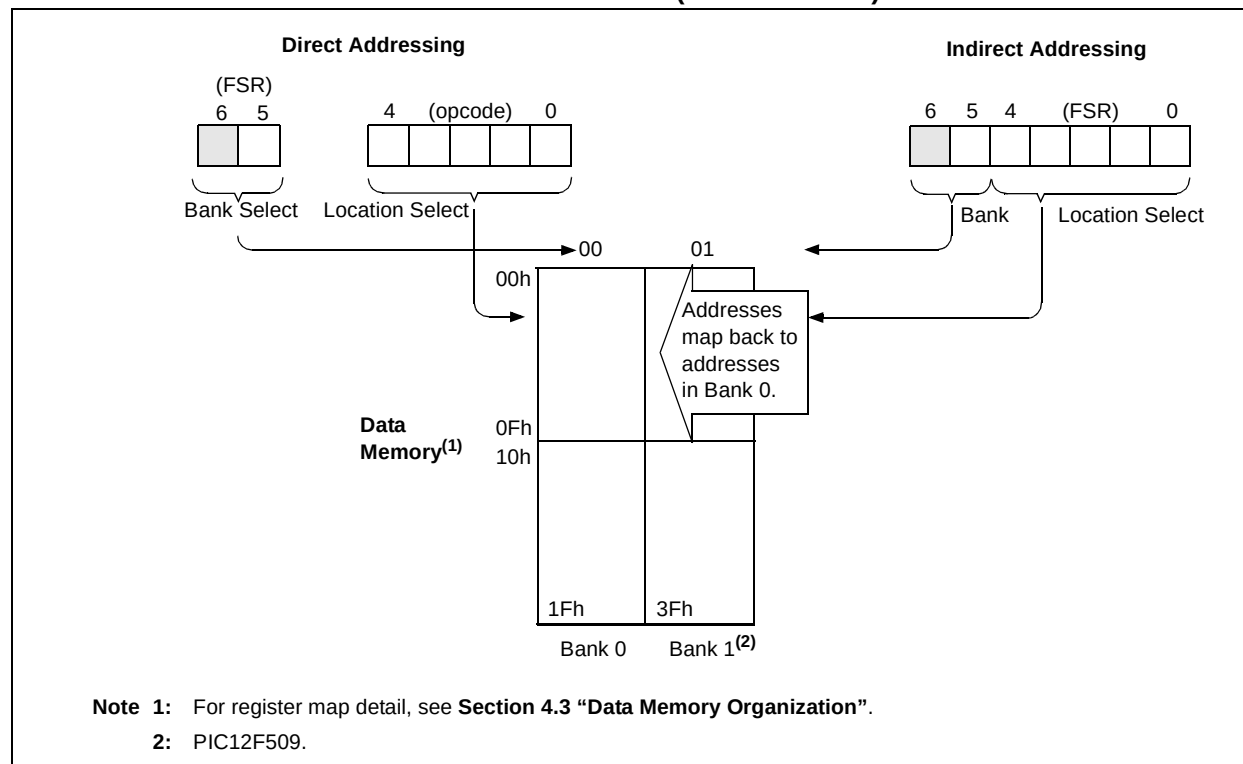
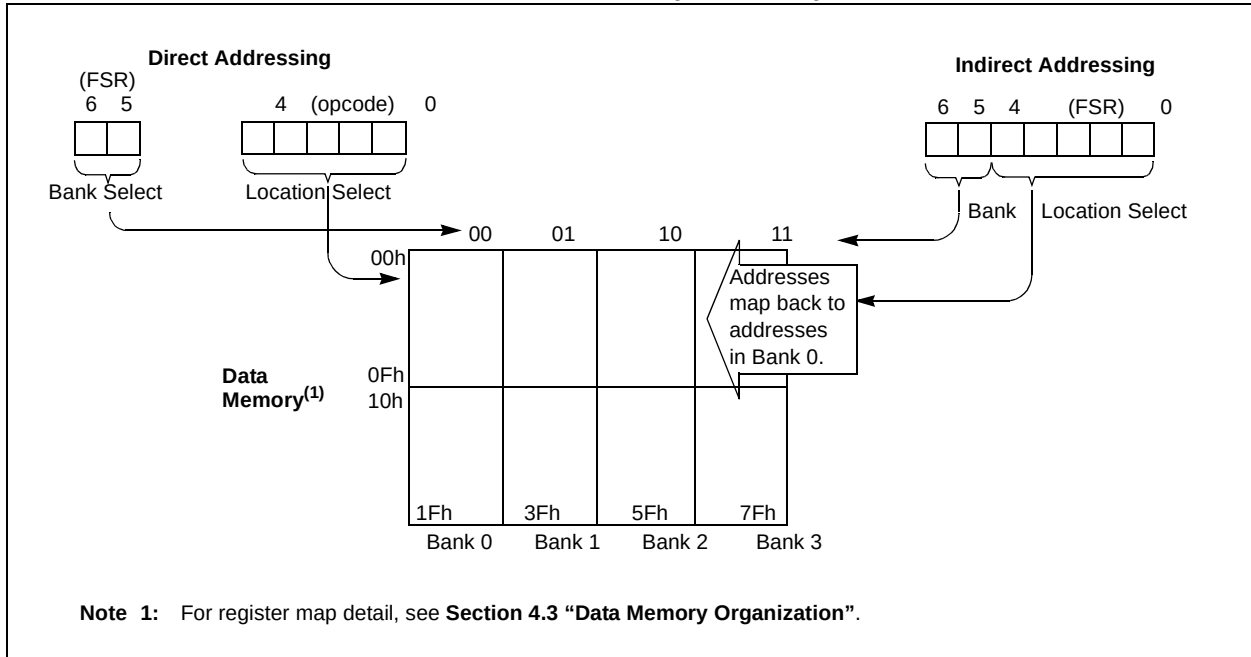


FIGURE 4-8: DIRECT/INDIRECT ADDRESSING (PIC16F505)



5.5 I/O Programming Considerations

5.5.1 BIDIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit 5 of PORTB/GPIO will cause all eight bits of PORTB/GPIO to be read into the CPU, bit 5 to be set and the PORTB/GPIO value to be written to the output latches. If another bit of PORTB/GPIO is used as a bidirectional I/O pin (say bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit 0 is switched into Output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential Read-Modify-Write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired OR", "wired AND"). The resulting high output currents may damage the chip.

EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT (e.g., PIC16F505)

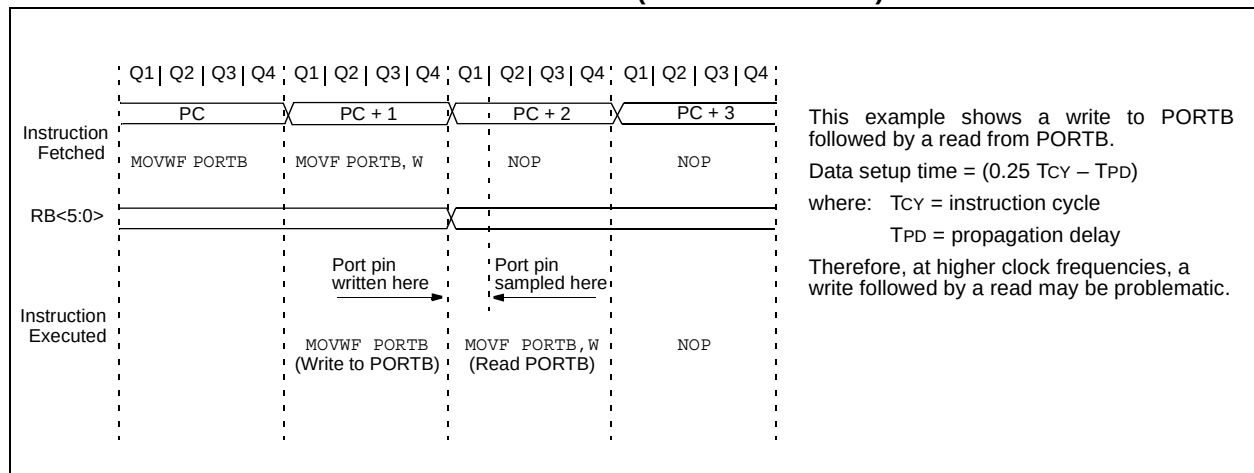
```
;Initial PORTB Settings
;PORTB<5:3> Inputs
;PORTB<2:0> Outputs
;
;          PORTB latch  PORTB pins
;          -----
BCF    PORTB, 5 ;--01 -ppp  --11 pppp
BCF    PORTB, 4 ;--10 -ppp  --11 pppp
MOVLW  007h;
TRIS   PORTB    ;--10 -ppp  --11 pppp
;
```

Note 1: The user may have expected the pin values to be '--00 pppp'. The 2nd BCF caused RB5 to be latched as the pin value (High).

5.5.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction causes that file to be read into the CPU. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 5-2: SUCCESSIVE I/O OPERATION (PIC16F505 Shown)



PIC12F508/509/16F505

NOTES:

PIC12F508/509/16F505

6.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module or as a postscaler for the Watchdog Timer (WDT), respectively (see **Section 7.6 “Watchdog Timer (WDT)”**). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet.

Note: The prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT and vice versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, x, etc.) will clear the prescaler. When assigned to WDT, a CLRWDW instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a Reset, the prescaler contains all '0's.

6.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed “on-the-fly” during program execution). To avoid an unintended device Reset, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0 → WDT)

```
CLRWDW          ;Clear WDT
CLRF    TMR0     ;Clear TMR0 & Prescaler
MOVLW  '00xx1111'b ;These 3 lines (5, 6, 7)
OPTION          ;are required only if
                ;desired
CLRWDW          ;PS<2:0> are 000 or 001
MOVLW  '00xx1xxx'b ;Set Postscaler to
OPTION          ;desired WDT rate
```

To change the prescaler from the WDT to the Timer0 module, use the sequence shown in Example 6-2. This sequence must be used even if the WDT is disabled. A CLRWDW instruction should be executed before switching the prescaler.

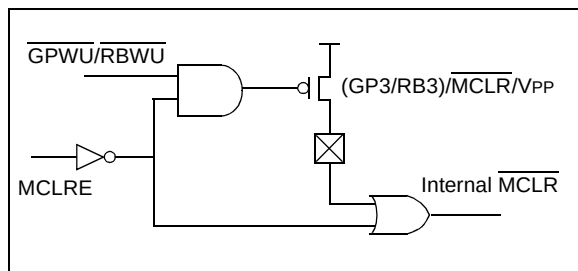
EXAMPLE 6-2: CHANGING PRESCALER (WDT → TIMER0)

```
CLRWDW          ;Clear WDT and
                ;prescaler
MOVLW  'xxxx0xxx' ;Select TMR0, new
                ;prescale value and
                ;clock source
OPTION
```

7.3.1 $\overline{\text{MCLR}}$ ENABLE

This Configuration bit, when unprogrammed (left in the '1' state), enables the external MCLR function. When programmed, the MCLR function is tied to the internal VDD and the pin is assigned to be an input only. See Figure 7-6.

FIGURE 7-6: $\overline{\text{MCLR}}$ SELECT



7.4 Power-on Reset (POR)

The PIC12F508/509/16F505 devices incorporate an on-chip Power-on Reset (POR) circuitry, which provides an internal chip Reset for most power-up situations.

The on-chip POR circuit holds the chip in Reset until VDD has reached a high enough level for proper operation. To take advantage of the internal POR, program the (GP3/RB3)/MCLR/VPP pin as MCLR and tie through a resistor to VDD, or program the pin as (GP3/RB3). An internal weak pull-up resistor is implemented using a transistor (refer to Table 10-2 for the pull-up resistor ranges). This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified. See **Section 10.0 "Electrical Characteristics"** for details.

When the devices start normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the devices must be held in Reset until the operating parameters are met.

A simplified block diagram of the on-chip Power-on Reset circuit is shown in Figure 7-7.

The Power-on Reset circuit and the Device Reset Timer (see **Section 7.5 "Device Reset Timer (DRT)"**) circuit are closely related. On power-up, the Reset latch is set and the DRT is reset. The DRT timer begins counting once it detects $\overline{\text{MCLR}}$ to be high. After the time-out period, which is typically 18 ms, it will reset the Reset latch and thus end the on-chip Reset signal.

A power-up example where $\overline{\text{MCLR}}$ is held low is shown in Figure 7-8. VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of Reset TdRT msec after MCLR goes high.

In Figure 7-9, the on-chip Power-on Reset feature is being used (MCLR and VDD are tied together or the pin is programmed to be (GP3/RB3)). The VDD is stable before the start-up timer times out and there is no problem in getting a proper Reset. However, Figure 7-10 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses that MCLR is high and when MCLR and VDD actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip may not function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 7-9).

Note: When the devices start normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to Application Notes AN522 "Power-Up Considerations" (DS00522) and AN607 "Power-up Trouble Shooting" (DS00607).

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7.7 Time-out Sequence, Power-down and Wake-up from Sleep Status Bits ($\overline{TO}$, $\overline{PD}$, GPWUF/RBWUF)

The $\overline{TO}$, $\overline{PD}$ and (GPWUF/RBWUF) bits in the STATUS register can be tested to determine if a Reset condition has been caused by a Power-up condition, a MCLR or Watchdog Timer (WDT) Reset.

TABLE 7-8: $\overline{TO}/\overline{PD}/(GPWUF/RBWUF)$ STATUS AFTER RESET

GPWUF/ RBWUF	$\overline{TO}$	$\overline{PD}$	Reset Caused By
0	0	0	WDT wake-up from Sleep
0	0	u	WDT time-out (not from Sleep)
0	1	0	MCLR wake-up from Sleep
0	1	1	Power-up
0	u	u	MCLR not during Sleep
1	1	0	Wake-up from Sleep on pin change

Legend: u = unchanged

Note 1: The $\overline{TO}$, $\overline{PD}$ and GPWUF/RBWUF bits maintain their status (u) until a Reset occurs. A low-pulse on the MCLR input does not change the $\overline{TO}$, $\overline{PD}$ and GPWUF/RBWUF Status bits.

7.8 Reset on Brown-out

A brown-out is a condition where device power (V_{DD}) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

To reset PIC12F508/509/16F505 devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 7-12 and Figure 7-13.

FIGURE 7-12: BROWN-OUT PROTECTION CIRCUIT 1

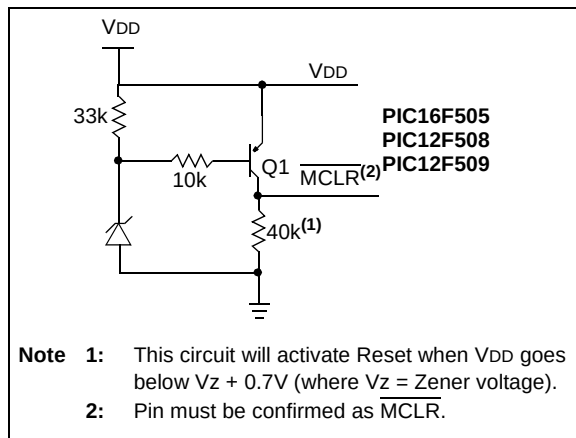


FIGURE 7-13: BROWN-OUT PROTECTION CIRCUIT 2

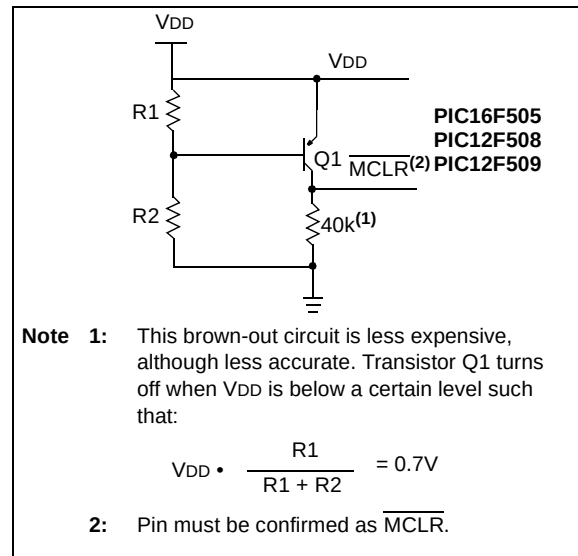
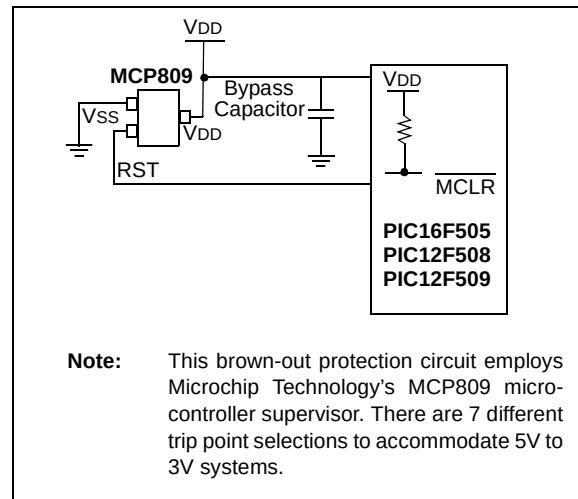
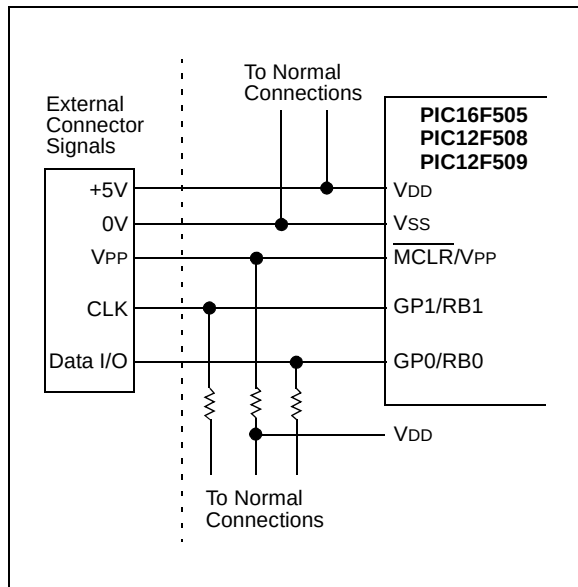


FIGURE 7-14: BROWN-OUT PROTECTION CIRCUIT 3



PIC12F508/509/16F505

FIGURE 7-15: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



PIC12F508/509/16F505

TABLE 8-2: INSTRUCTION SET SUMMARY

Mnemonic, Operands		Description	Cycles	12-Bit Opcode			Status Affected	Notes
				MSb	LSb			
ADDWF	f, d	Add W and f	1	0001	11df	ffff	C, DC, Z	1, 2, 4
ANDWF	f, d	AND W with f	1	0001	01df	ffff	Z	2, 4
CLRF	f	Clear f	1	0000	011f	ffff	Z	4
CLRW	—	Clear W	1	0000	0100	0000	Z	
COMF	f, d	Complement f	1	0010	01df	ffff	Z	
DECF	f, d	Decrement f	1	0000	11df	ffff	Z	2, 4
DECFSZ	f, d	Decrement f, Skip if 0	1 ⁽²⁾	0010	11df	ffff	None	2, 4
INCF	f, d	Increment f	1	0010	10df	ffff	Z	2, 4
INCFSZ	f, d	Increment f, Skip if 0	1 ⁽²⁾	0011	11df	ffff	None	2, 4
IORWF	f, d	Inclusive OR W with f	1	0001	00df	ffff	Z	2, 4
MOVF	f, d	Move f	1	0010	00df	ffff	Z	2, 4
MOVWF	f	Move W to f	1	0000	001f	ffff	None	1, 4
NOP	—	No Operation	1	0000	0000	0000	None	
RLF	f, d	Rotate left f through Carry	1	0011	01df	ffff	C	2, 4
RRF	f, d	Rotate right f through Carry	1	0011	00df	ffff	C	2, 4
SUBWF	f, d	Subtract W from f	1	0000	10df	ffff	C, DC, Z	1, 2, 4
SWAPF	f, d	Swap f	1	0011	10df	ffff	None	2, 4
XORWF	f, d	Exclusive OR W with f	1	0001	10df	ffff	Z	2, 4
BIT-ORIENTED FILE REGISTER OPERATIONS								
BCF	f, b	Bit Clear f	1	0100	bbbf	ffff	None	2, 4
BSF	f, b	Bit Set f	1	0101	bbbf	ffff	None	2, 4
BTFSC	f, b	Bit Test f, Skip if Clear	1 ⁽²⁾	0110	bbbf	ffff	None	
BTFSS	f, b	Bit Test f, Skip if Set	1 ⁽²⁾	0111	bbbf	ffff	None	
LITERAL AND CONTROL OPERATIONS								
ANDLW	k	AND literal with W	1	1110	kkkk	kkkk	Z	1
CALL	k	Call Subroutine	2	1001	kkkk	kkkk	None	
CLRWDT	—	Clear Watchdog Timer	1	0000	0000	0100	TO, PD	
GOTO	k	Unconditional branch	2	101k	kkkk	kkkk	None	
IORLW	k	Inclusive OR literal with W	1	1101	kkkk	kkkk	Z	3
MOVLW	k	Move literal to W	1	1100	kkkk	kkkk	None	
OPTION	—	Load OPTION register	1	0000	0000	0010	None	
RETLW	k	Return, place literal in W	2	1000	kkkk	kkkk	None	
SLEEP	—	Go into Standby mode	1	0000	0000	0011	TO, PD	
TRIS	f	Load TRIS register	1	0000	0000	0fff	None	
XORLW	k	Exclusive OR literal to W	1	1111	kkkk	kkkk	Z	

Note 1: The 9th bit of the program counter will be forced to a '0' by any instruction that writes to the PC except for GOTO. See **Section 4.7 "Program Counter"**.

- When an I/O register is modified as a function of itself (e.g. MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- The instruction TRIS f, where f = 6, causes the contents of the W register to be written to the tri-state latches of PORTB. A '1' forces the pin to a high-impedance state and disables the output buffers.
- If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared (if assigned to TMR0).

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IORWF **Inclusive OR W with f**

Syntax: [*label*] IORWF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: (W).OR. (f) $\rightarrow$ (dest)

Status Affected: Z

Description: Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

MOVWF **Move W to f**

Syntax: [*label*] MOVWF f

Operands: $0 \leq f \leq 31$

Operation: (W) $\rightarrow$ (f)

Status Affected: None

Description: Move data from the W register to register 'f'.

MOVF **Move f**

Syntax: [*label*] MOVF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

Operation: (f) $\rightarrow$ (dest)

Status Affected: Z

Description: The contents of register 'f' are moved to destination 'd'. If 'd' is '0', destination is the W register. If 'd' is '1', the destination is file register 'f'. 'd' = 1 is useful as a test of a file register, since status flag Z is affected.

NOP **No Operation**

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

Description: No operation.

MOVLW **Move Literal to W**

Syntax: [*label*] MOVLW k

Operands: $0 \leq k \leq 255$

Operation: $k \rightarrow$ (W)

Status Affected: None

Description: The eight-bit literal 'k' is loaded into the W register. The "don't cares" will assembled as '0's.

OPTION **Load OPTION Register**

Syntax: [*label*] OPTION

Operands: None

Operation: (W) $\rightarrow$ OPTION

Status Affected: None

Description: The content of the W register is loaded into the OPTION register.

9.11 PICSTART Plus Development Programmer

The PICSTART Plus Development Programmer is an easy-to-use, low-cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus Development Programmer supports most PIC devices in DIP packages up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus Development Programmer is CE compliant.

9.12 PICKit 2 Development Programmer

The PICKit™ 2 Development Programmer is a low-cost programmer and selected Flash device debugger with an easy-to-use interface for programming many of Microchip's baseline, mid-range and PIC18F families of Flash memory microcontrollers. The PICKit 2 Starter Kit includes a prototyping development board, twelve sequential lessons, software and HI-TECH's PICC™ Lite C compiler, and is designed to help get up to speed quickly using PIC® microcontrollers. The kit provides everything needed to program, evaluate and develop applications using Microchip's powerful, mid-range Flash memory family of microcontrollers.

9.13 Demonstration, Development and Evaluation Boards

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

10.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings^(†)

Ambient temperature under bias	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on V _{DD} with respect to V _{SS}	0 to +6.5V
Voltage on $\overline{\text{MCLR}}$ with respect to V _{SS}	0 to +13.5V
Voltage on all other pins with respect to V _{SS}	-0.3V to (V _{DD} + 0.3V)
Total power dissipation ⁽¹⁾	800 mW
Max. current out of V _{SS} pin	200 mA
Max. current into V _{DD} pin	150 mA
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DD})	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD})	±20 mA
Max. output current sunk by any I/O pin	25 mA
Max. output current sourced by any I/O pin	25 mA
Max. output current sourced by I/O port	75 mA
Max. output current sunk by I/O port	75 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

[†]NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

10.3 Timing Parameter Symbolology and Load Conditions – PIC12F508/509/16F505

The timing parameter symbols have been created following one of the following formats:

- 1. TppS2ppS
- 2. TppS

T	
F Frequency	T Time

Lowercase subscripts (pp) and their meanings:

pp		
2	to	mc $\overline{\text{MCLR}}$
ck	CLKOUT	osc Oscillator
cy	Cycle time	os OSC1
drt	Device Reset Timer	t0 T0CKI
io	I/O port	wdt Watchdog Timer

Uppercase letters and their meanings:

S		
F	Fall	P Period
H	High	R Rise
I	Invalid (high-impedance)	V Valid
L	Low	Z High-impedance

FIGURE 10-3: LOAD CONDITIONS – PIC12F508/509/16F505

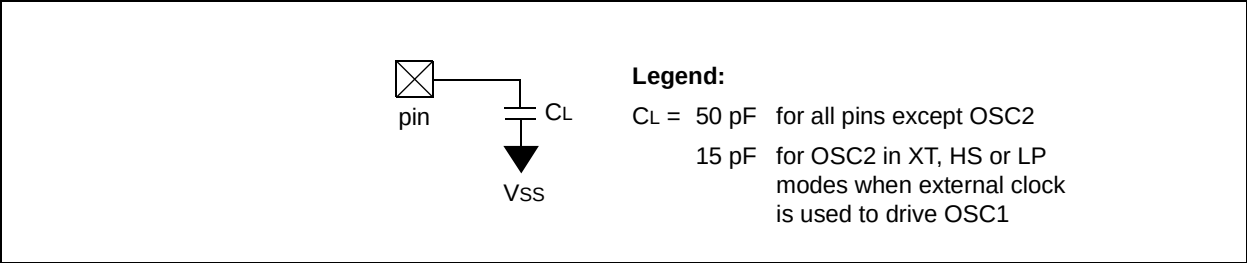


FIGURE 10-4: EXTERNAL CLOCK TIMING – PIC12F508/509/16F505

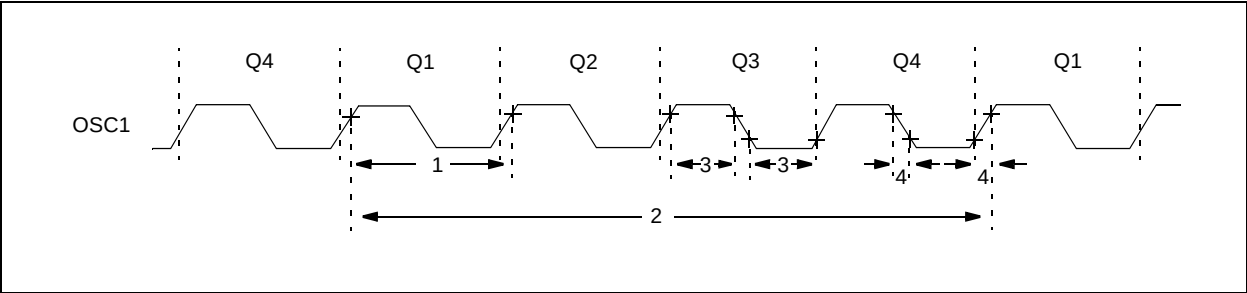


FIGURE 11-12: TTL INPUT THRESHOLD V_{IN} vs. V_{DD}

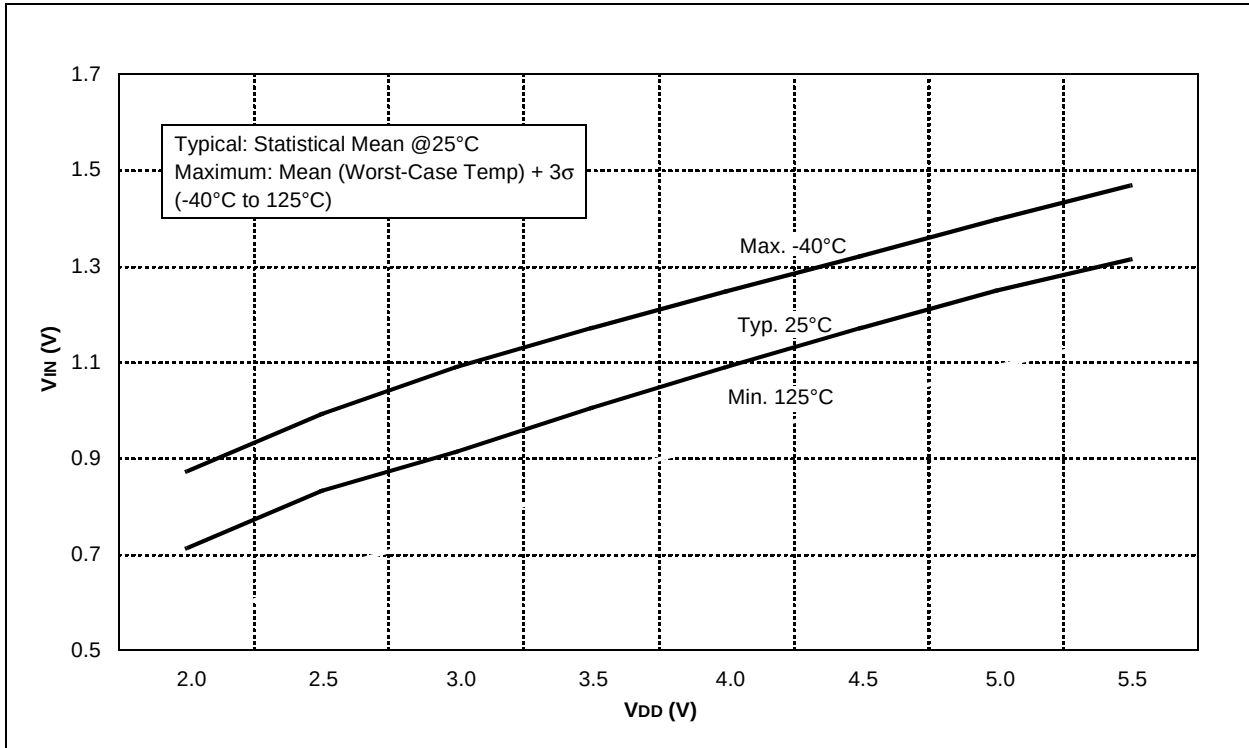
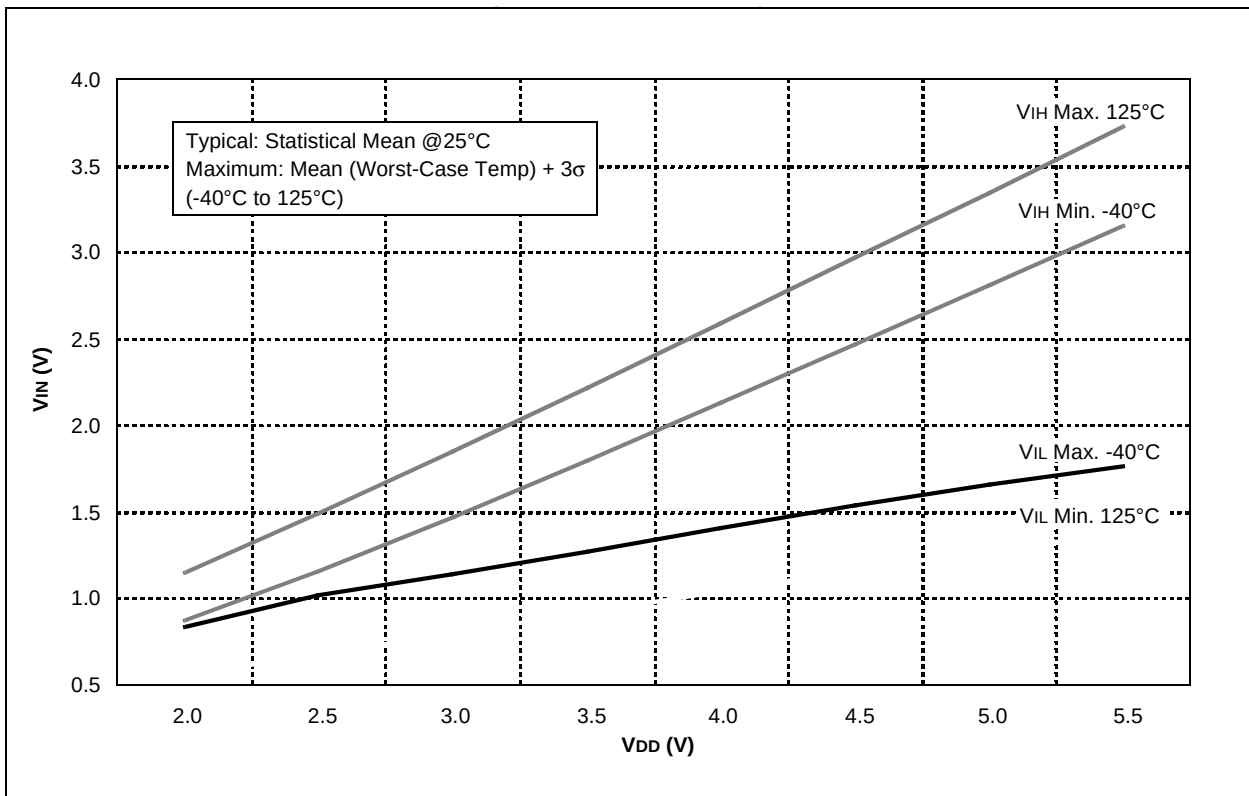


FIGURE 11-13: SCHMITT TRIGGER INPUT THRESHOLD V_{IN} vs. V_{DD}



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W

Wake-up from Sleep 55

Watchdog Timer (WDT) 41, 52

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Z

Zero bit 11