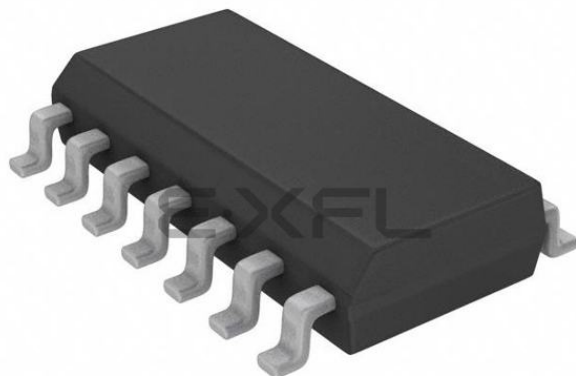




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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	11
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package	14-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f505t-e-sl

PIC12F508/509/16F505

Table of Contents

1.0	General Description	7
2.0	PIC12F508/509/16F505 Device Varieties	9
3.0	Architectural Overview	11
4.0	Memory Organization	17
5.0	I/O Port	31
6.0	Timer0 Module and TMR0 Register	35
7.0	Special Features Of The CPU	41
8.0	Instruction Set Summary	57
9.0	Development Support	65
10.0	Electrical Characteristics	69
11.0	DC and AC Characteristics Graphs and Charts	81
12.0	Packaging Information	91
	Index	105
	The Microchip Web Site	107
	Customer Change Notification Service	107
	Customer Support	107
	Reader Response	108
	Product Identification System	109

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PIC12F508/509/16F505

NOTES:

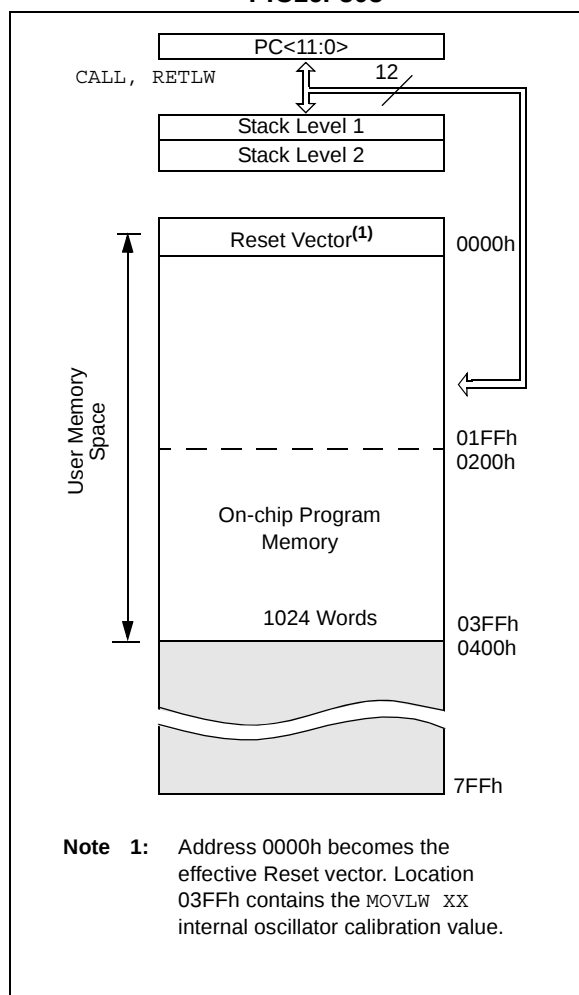
PIC12F508/509/16F505

4.2 Program Memory Organization For The PIC16F505

The PIC16F505 device has a 11-bit Program Counter (PC) capable of addressing a 2K x 12 program memory space.

The 1K x 12 (0000h-03FFh) for the PIC16F505 are physically implemented. Refer to Figure 4-2. Accessing a location above this boundary will cause a wrap-around within the first 1K x 12 space. The effective Reset vector is at 0000h (see Figure 4-2). Location 03FFh contains the internal oscillator calibration value. This value should never be overwritten.

FIGURE 4-2: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F505



4.3 Data Memory Organization

Data memory is composed of registers or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: Special Function Registers (SFR) and General Purpose Registers (GPR).

The Special Function Registers include the TMR0 register, the Program Counter (PCL), the STATUS register, the I/O registers (ports) and the File Select Register (FSR). In addition, Special Function Registers are used to control the I/O port configuration and prescaler options.

The General Purpose Registers are used for data and control information under command of the instructions.

For the PIC12F508/509, the register file is composed of 7 Special Function Registers, 9 General Purpose Registers and 16 or 32 General Purpose Registers accessed by banking (see Figure 4-3 and Figure 4-4).

For the PIC16F505, the register file is composed of 8 Special Function Registers, 8 General Purpose Registers and 64 General Purpose Registers accessed by banking (Figure 4-5).

4.3.1 GENERAL PURPOSE REGISTER FILE

The General Purpose Register file is accessed, either directly or indirectly, through the File Select Register (FSR). See **Section 4.9 "Indirect Data Addressing: INDF and FSR Registers"**.

PIC12F508/509/16F505

4.4 STATUS Register

This register contains the arithmetic status of the ALU, the Reset status and the page preselect bit.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS`, will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where u = unchanged).

Therefore, it is recommended that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS register. These instructions do not affect the Z, DC or C bits from the STATUS register. For other instructions which do affect Status bits, see **Section 8.0 “Instruction Set Summary”**.

REGISTER 4-1: STATUS REGISTER (ADDRESS: 03h) (PIC12F508/509)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
GPWUF	—	PA0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

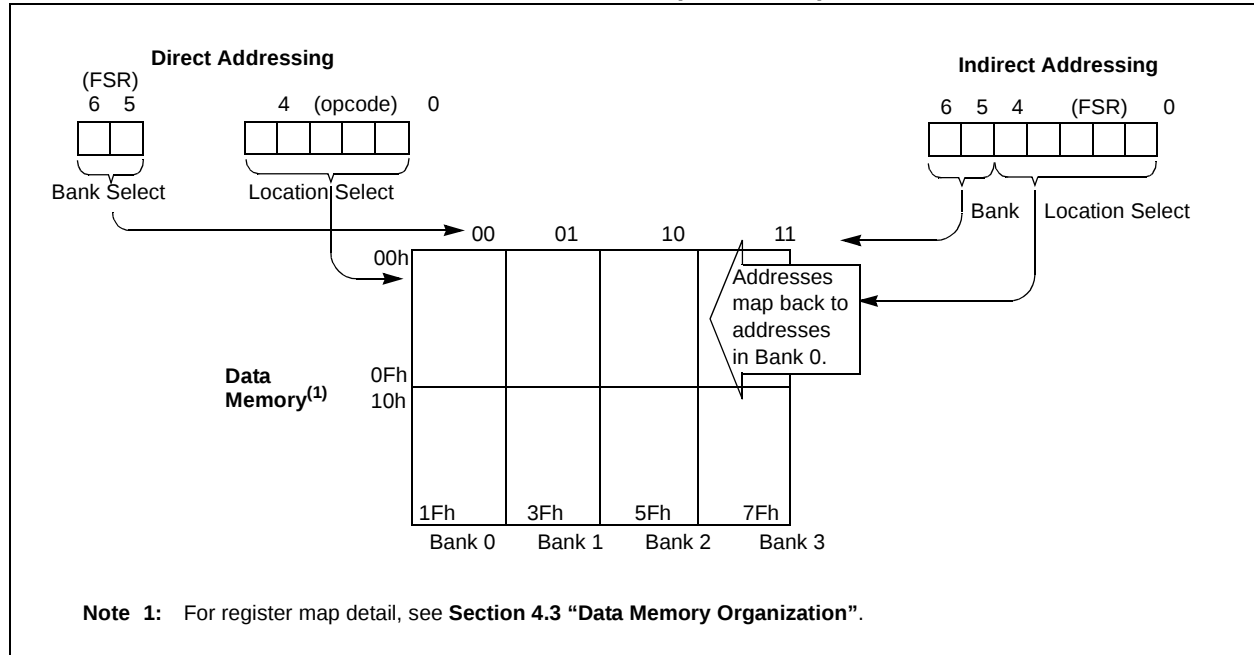
'0' = Bit is cleared

x = Bit is unknown

bit 7	GPWUF: GPIO Reset bit 1 = Reset due to wake-up from Sleep on pin change 0 = After power-up or other Reset
bit 6	Reserved: Do not use
bit 5	PA0: Program Page Preselect bits ⁽¹⁾ 1 = Page 1 (200h-3FFh) 0 = Page 0 (000h-1FFh) Each page is 512 bytes. Using the PA0 bit as a general purpose read/write bit in devices which do not use it for program page preselect is not recommended, since this may affect upward compatibility with future products.
bit 4	$\overline{\text{TO}}$: Time-Out bit 1 = After power-up, <code>CLRWDT</code> instruction, or <code>SLEEP</code> instruction 0 = A WDT time-out occurred
bit 3	$\overline{\text{PD}}$: Power-Down bit 1 = After power-up or by the <code>CLRWDT</code> instruction 0 = By execution of the <code>SLEEP</code> instruction
bit 2	Z: Zero bit 1 = The result of an arithmetic or logic operation is zero 0 = The result of an arithmetic or logic operation is not zero
bit 1	DC: Digit Carry/Borrow bit (for <code>ADDWF</code> and <code>SUBWF</code> instructions) <u>ADDWF:</u> 1 = A carry from the 4th low-order bit of the result occurred 0 = A carry from the 4th low-order bit of the result did not occur <u>SUBWF:</u> 1 = A borrow from the 4th low-order bit of the result did not occur 0 = A borrow from the 4th low-order bit of the result occurred
bit 0	C: Carry/Borrow bit (for <code>ADDWF</code> , <code>SUBWF</code> and <code>RRF</code> , <code>RLF</code> instructions) <u>ADDWF:</u> 1 = A carry occurred 0 = A carry did not occur <u>SUBWF:</u> 1 = A borrow did not occur 0 = A borrow occurred <u>RRF_OR_RLF:</u> Load bit with LSb or MSb, respectively

Note 1: This bit is used on the PIC12F509. For code compatibility do not use this bit on the PIC12F508.

FIGURE 4-8: DIRECT/INDIRECT ADDRESSING (PIC16F505)



PIC12F508/509/16F505

FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

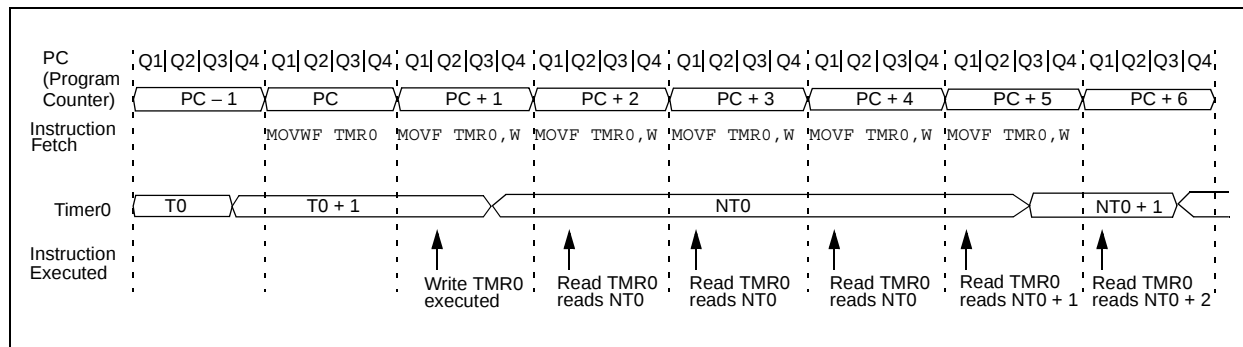


TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
01h	TMR0	Timer0 – 8-bit Real-Time Clock/Counter								xxxx xxxx	uuuu uuuu
N/A	OPTION ⁽¹⁾	GPWU	GPPU	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
N/A	OPTION ⁽²⁾	RBWU	RBPW	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
N/A	TRISGPIO ^{(1), (3)}	—	—	I/O Control Register						--11 1111	--11 1111
N/A	TRISC ^{(2), (3)}	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--11 1111	--11 1111

Legend: Shaded cells are not used by Timer0. – = unimplemented, x = unknown, u = unchanged.

Note 1: PIC12F508/509 only.

Note 2: PIC16F505 only.

Note 3: The TRIS of the T0CKI pin is overridden when T0CS = 1.

PIC12F508/509/16F505

6.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module or as a postscaler for the Watchdog Timer (WDT), respectively (see **Section 7.6 “Watchdog Timer (WDT)”**). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet.

Note: The prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT and vice versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, x, etc.) will clear the prescaler. When assigned to WDT, a CLRWDW instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a Reset, the prescaler contains all '0's.

6.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed “on-the-fly” during program execution). To avoid an unintended device Reset, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0 → WDT)

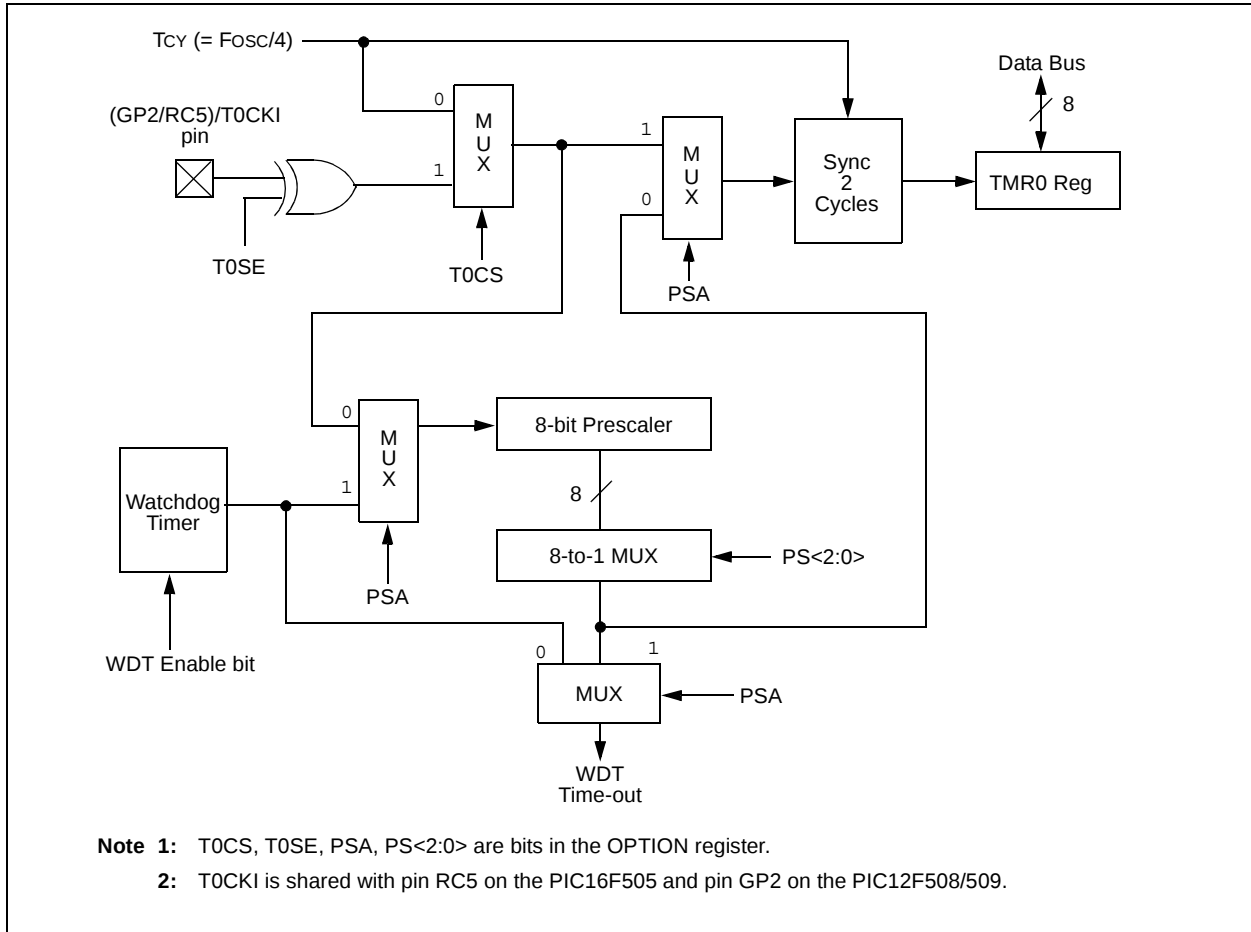
```
CLRWDW          ;Clear WDT
CLRF    TMR0     ;Clear TMR0 & Prescaler
MOVLW    '00xx1111'b ;These 3 lines (5, 6, 7)
OPTION          ;are required only if
                ;desired
CLRWDW          ;PS<2:0> are 000 or 001
MOVLW    '00xx1xxx'b ;Set Postscaler to
OPTION          ;desired WDT rate
```

To change the prescaler from the WDT to the Timer0 module, use the sequence shown in Example 6-2. This sequence must be used even if the WDT is disabled. A CLRWDW instruction should be executed before switching the prescaler.

EXAMPLE 6-2: CHANGING PRESCALER (WDT → TIMER0)

```
CLRWDW          ;Clear WDT and
                ;prescaler
MOVLW    'xxxx0xxx' ;Select TMR0, new
                ;prescale value and
                ;clock source
OPTION
```

FIGURE 6-5: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER^{(1), (2)}



7.9 Power-down Mode (Sleep)

A device may be powered down (Sleep) and later powered up (wake-up from Sleep).

7.9.1 SLEEP

The Power-Down mode is entered by executing a `SLEEP` instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{TO}$ bit (`STATUS<4>`) is set, the $\overline{PD}$ bit (`STATUS<3>`) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the `SLEEP` instruction was executed (driving high, driving low or high-impedance).

Note: A Reset generated by a WDT time-out does not drive the $\overline{MCLR}$ pin low.

For lowest current consumption while powered down, the $\overline{TOCKI}$ input should be at V_{DD} or V_{SS} and the (GP3/RB3)/ $\overline{MCLR}/V_{PP}$ pin must be at a logic high level if $\overline{MCLR}$ is enabled.

7.9.2 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:

1. An external Reset input on (GP3/RB3)/ $\overline{MCLR}/V_{PP}$ pin, when configured as $\overline{MCLR}$.
2. A Watchdog Timer time-out Reset (if WDT was enabled).
3. A change on input pin GP0/RB0, GP1/RB1, GP3/RB3 or RB4 when wake-up on change is enabled.

These events cause a device Reset. The $\overline{TO}$, $\overline{PD}$ and GPWUF/RBWUF bits can be used to determine the cause of device Reset. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up). The $\overline{PD}$ bit, which is set on power-up, is cleared when `SLEEP` is invoked. The GPWUF/RBWUF bit indicates a change in state while in Sleep at pins GP0/RB0, GP1/RB1, GP3/RB3 or RB4 (since the last file or bit operation on GP/RB port).

Note: **Caution:** Right before entering Sleep, read the input pins. When in Sleep, wake-up occurs when the values at the pins change from the state they were in at the last reading. If a wake-up on change occurs and the pins are not read before re-entering Sleep, a wake-up will occur immediately even if no pins change while in Sleep mode.

The WDT is cleared when the device wakes from Sleep, regardless of the wake-up source.

7.10 Program Verification/Code Protection

If the code protection bit has not been programmed, the on-chip program memory can be read out for verification purposes.

The first 64 locations and the last location (OSCCAL) can be read, regardless of the code protection bit setting.

The last memory location can be read regardless of the code protection bit setting on the PIC12F508/509/16F505 devices.

7.11 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during Program/Verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '0's.

7.12 In-Circuit Serial Programming™

The PIC12F508/509/16F505 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware, or a custom firmware, to be programmed.

The devices are placed into a Program/Verify mode by holding the GP1/RB1 and GP0/RB0 pins low while raising the $\overline{MCLR}$ (V_{PP}) pin from V_{IL} to V_{IH} (see programming specification). GP1/RB1 becomes the programming clock and GP0/RB0 becomes the programming data. Both GP1/RB1 and GP0/RB0 are Schmitt Trigger inputs in this mode.

After Reset, a 6-bit command is then supplied to the device. Depending on the command, 14 bits of program data are then supplied to or from the device, depending if the command was a Load or a Read. For complete details of serial programming, please refer to the PIC12F508/509/16F505 Programming Specifications.

A typical In-Circuit Serial Programming connection is shown in Figure 7-15.

ADDWF Add W and f

Syntax: [*label*] ADDWF f,d
 Operands: $0 \leq f \leq 31$
 $d \in [0,1]$
 Operation: $(W) + (f) \rightarrow (\text{dest})$
 Status Affected: C, DC, Z
 Description: Add the contents of the W register and register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

BCF Bit Clear f

Syntax: [*label*] BCF f,b
 Operands: $0 \leq f \leq 31$
 $0 \leq b \leq 7$
 Operation: $0 \rightarrow (f)$
 Status Affected: None
 Description: Bit 'b' in register 'f' is cleared.

ANDLW AND literal with W

Syntax: [*label*] ANDLW k
 Operands: $0 \leq k \leq 255$
 Operation: $(W).AND. (k) \rightarrow (W)$
 Status Affected: Z
 Description: The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

BSF Bit Set f

Syntax: [*label*] BSF f,b
 Operands: $0 \leq f \leq 31$
 $0 \leq b \leq 7$
 Operation: $1 \rightarrow (f)$
 Status Affected: None
 Description: Bit 'b' in register 'f' is set.

ANDWF AND W with f

Syntax: [*label*] ANDWF f,d
 Operands: $0 \leq f \leq 31$
 $d \in [0,1]$
 Operation: $(W).AND. (f) \rightarrow (\text{dest})$
 Status Affected: Z
 Description: The contents of the W register are AND'ed with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

BTFSC Bit Test f, Skip if Clear

Syntax: [*label*] BTFSC f,b
 Operands: $0 \leq f \leq 31$
 $0 \leq b \leq 7$
 Operation: skip if $(f) = 0$
 Status Affected: None
 Description: If bit 'b' in register 'f' is '0', then the next instruction is skipped.
 If bit 'b' is '0', then the next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead, making this a two-cycle instruction.

DECF	Decrement f
Syntax:	[<i>label</i>] DECF f,d
Operands:	$0 \leq f \leq 31$ $d \in [0,1]$
Operation:	$(f) - 1 \rightarrow (\text{dest})$
Status Affected:	Z
Description:	Decrement register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

INCF	Increment f
Syntax:	[<i>label</i>] INCF f,d
Operands:	$0 \leq f \leq 31$ $d \in [0,1]$
Operation:	$(f) + 1 \rightarrow (\text{dest})$
Status Affected:	Z
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

DECFSZ	Decrement f, Skip if 0
Syntax:	[<i>label</i>] DECFSZ f,d
Operands:	$0 \leq f \leq 31$ $d \in [0,1]$
Operation:	$(f) - 1 \rightarrow d$; skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '0', the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction.

INCFSZ	Increment f, Skip if 0
Syntax:	[<i>label</i>] INCFSZ f,d
Operands:	$0 \leq f \leq 31$ $d \in [0,1]$
Operation:	$(f) + 1 \rightarrow (\text{dest})$, skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '0', then the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction.

GOTO	Unconditional Branch
Syntax:	[<i>label</i>] GOTO k
Operands:	$0 \leq k \leq 511$
Operation:	$k \rightarrow \text{PC}<8:0>$; $\text{STATUS}<6:5> \rightarrow \text{PC}<10:9>$
Status Affected:	None
Description:	GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS<6:5>. GOTO is a two-cycle instruction.

IORLW	Inclusive OR literal with W
Syntax:	[<i>label</i>] IORLW k
Operands:	$0 \leq k \leq 255$
Operation:	$(W) .\text{OR.} (k) \rightarrow (W)$
Status Affected:	Z
Description:	The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.

9.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
 - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
 - MPASM™ Assembler
 - MPLAB C18 and MPLAB C30 C Compilers
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
 - MPLAB ASM30 Assembler/Linker/Library
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB ICE 2000 In-Circuit Emulator
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debugger
 - MPLAB ICD 2
- Device Programmers
 - PICSTART® Plus Development Programmer
 - MPLAB PM3 Device Programmer
 - PICKit™ 2 Development Programmer
- Low-Cost Demonstration and Development Boards and Evaluation Kits

9.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
 - Simulator
 - Programmer (sold separately)
 - Emulator (sold separately)
 - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Visual device initializer for easy register initialization
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as HI-TECH Software C Compilers and IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
 - Source files (assembly or C)
 - Mixed assembly and C
 - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

PIC12F508/509/16F505

TABLE 10-5: TIMING REQUIREMENTS – PIC12F508/509/16F505

AC CHARACTERISTICS		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) Operating Voltage V_{DD} range is described in Section 10.1 "Power-on Reset (POR)"				
Param No.	Sym.	Characteristic	Min.	Typ ⁽¹⁾	Max.	Units
17	TosH2ioV	OSC1 $\uparrow$ (Q1 cycle) to Port Out Valid ^{(2), (3)}	—	—	100*	ns
18	TosH2ioI	OSC1 $\uparrow$ (Q2 cycle) to Port Input Invalid (I/O in hold time) ⁽²⁾	50	—	—	ns
19	TioV2osH	Port Input Valid to OSC1 $\uparrow$ (I/O in setup time)	20	—	—	ns
20	TioR	Port Output Rise Time ⁽³⁾	—	10	25**	ns
21	TioF	Port Output Fall Time ⁽³⁾	—	10	25**	ns

* These parameters are characterized but not tested.

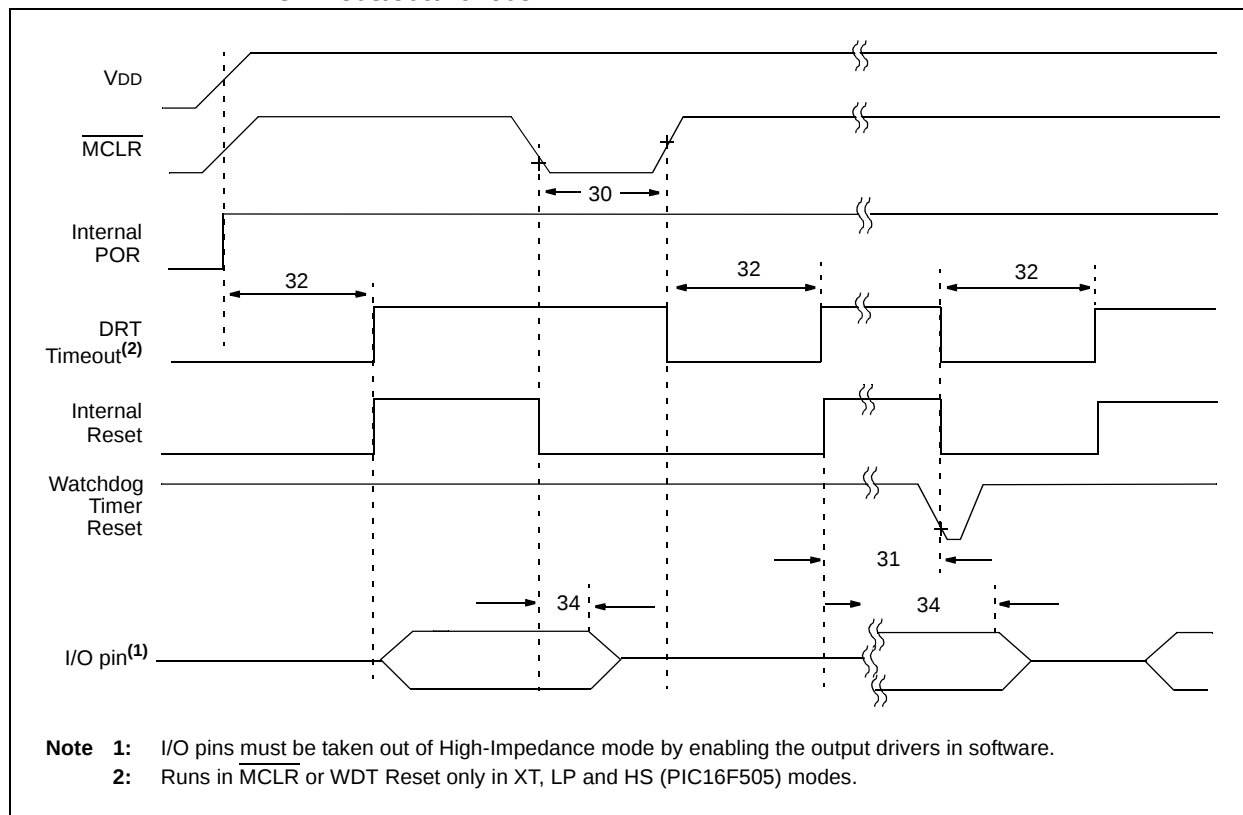
** These parameters are design targets and are not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in EXTRC mode.

3: See Figure 10-3 for loading conditions.

FIGURE 10-6: RESET, WATCHDOG TIMER AND DEVICE RESET TIMER TIMING – PIC12F508/509/16F505



PIC12F508/509/16F505

FIGURE 10-7: TIMER0 CLOCK TIMINGS – PIC12F508/509/16F505

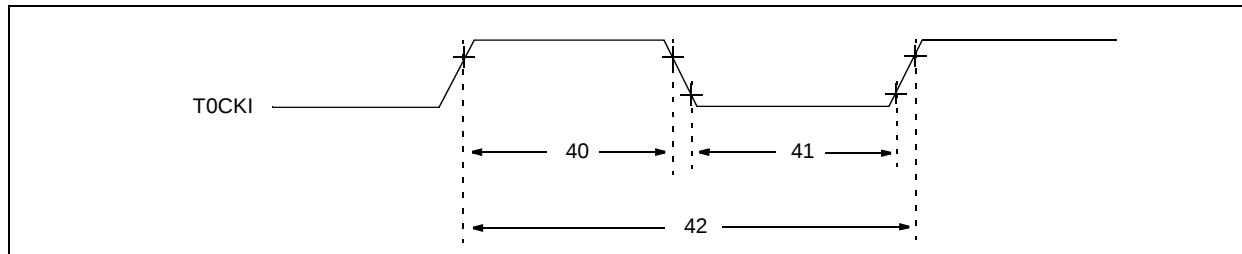


TABLE 10-7: TIMER0 CLOCK REQUIREMENTS – PIC12F508/509/16F505

AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) Operating Voltage V_{DD} range is described in Section 10.1 "Power-on Reset (POR)"					
Param No.	Sym.	Characteristic		Min.	Typ ⁽¹⁾	Max.	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	$0.5 T_{CY} + 20^*$	—	—	ns	
			With Prescaler	10^*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	$0.5 T_{CY} + 20^*$	—	—	ns	
			With Prescaler	10^*	—	—	ns	
42	Tt0P	T0CKI Period		$20 \text{ or } T_{CY} + 40^* N$	—	—	ns	Whichever is greater. $N = \text{Prescale Value}$ (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC12F508/509/16F505

FIGURE 11-6: MAXIMUM WDT I_{PD} vs. V_{DD} OVER TEMPERATURE

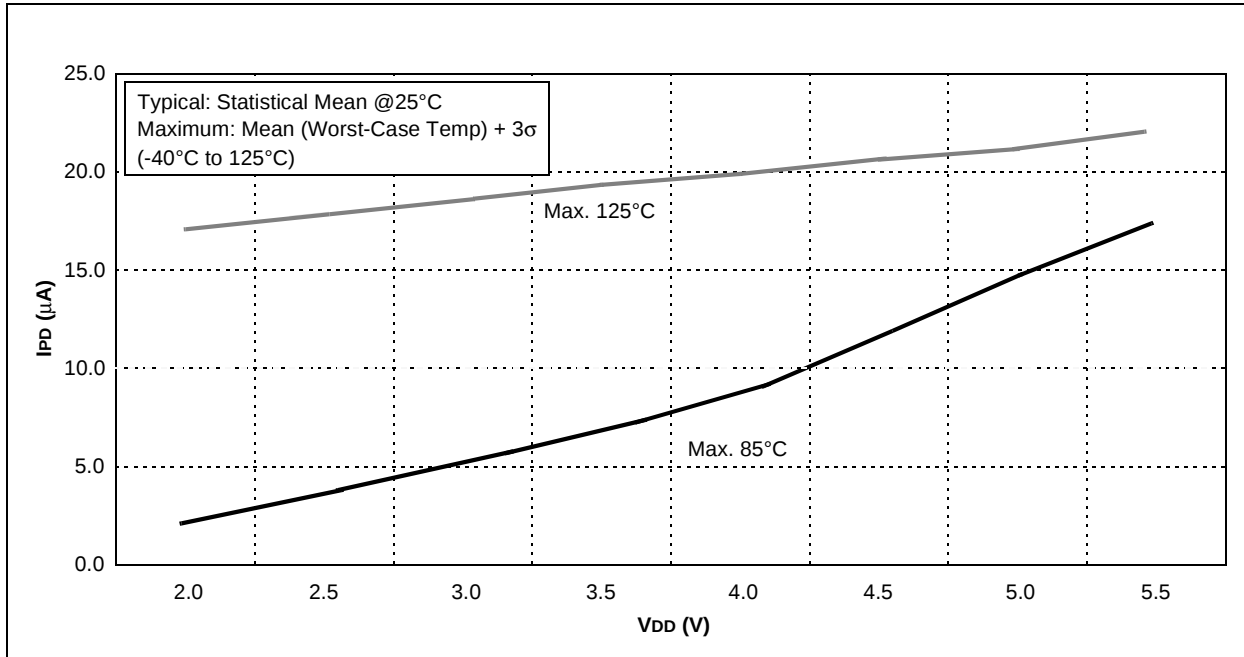


FIGURE 11-7: WDT TIME-OUT or DEVICE RESET TIMER vs. V_{DD} OVER TEMPERATURE (NO WDT PRESCALER)⁽¹⁾

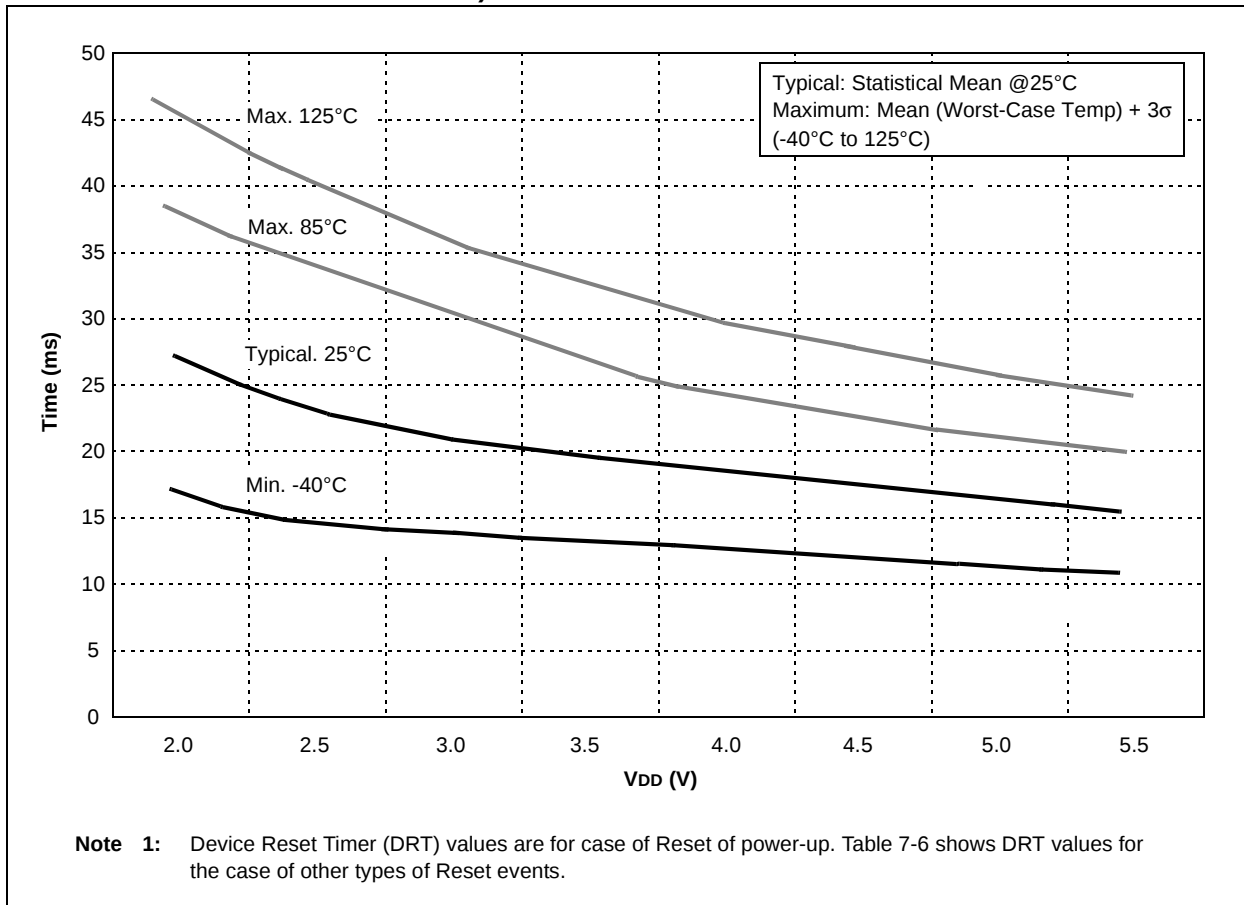


FIGURE 11-12: TTL INPUT THRESHOLD V_{IN} vs. V_{DD}

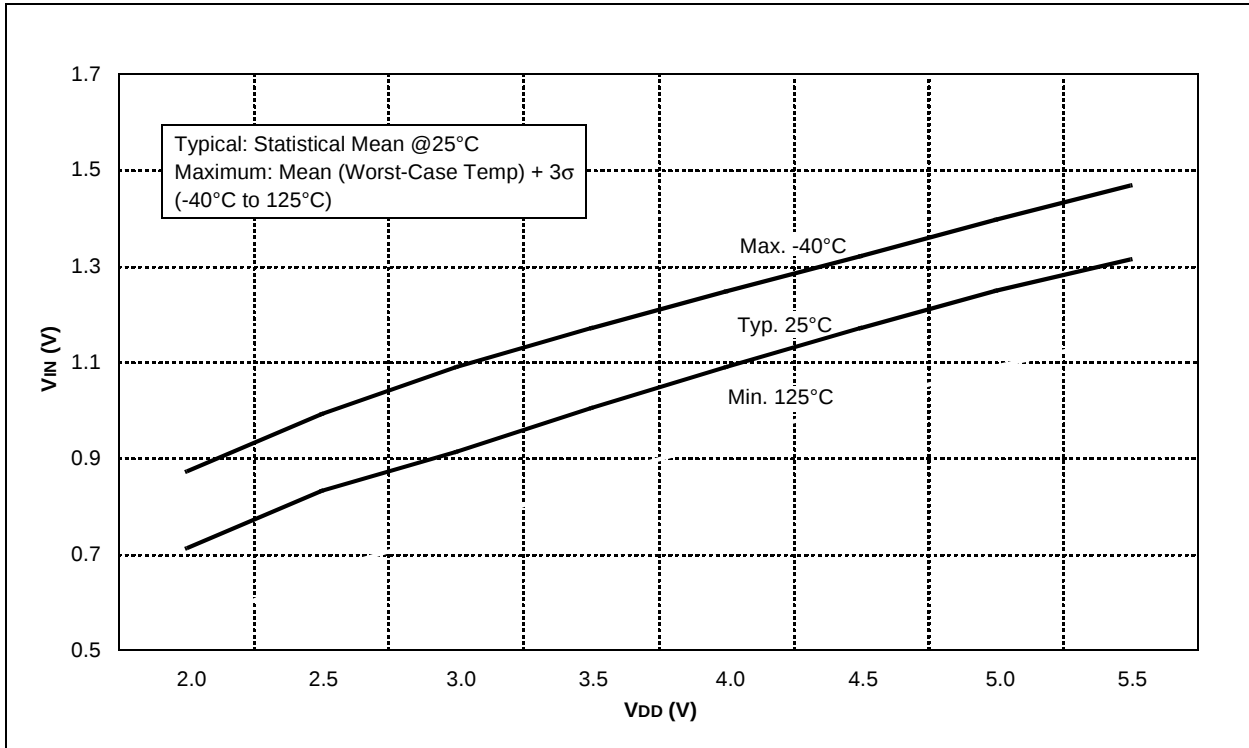
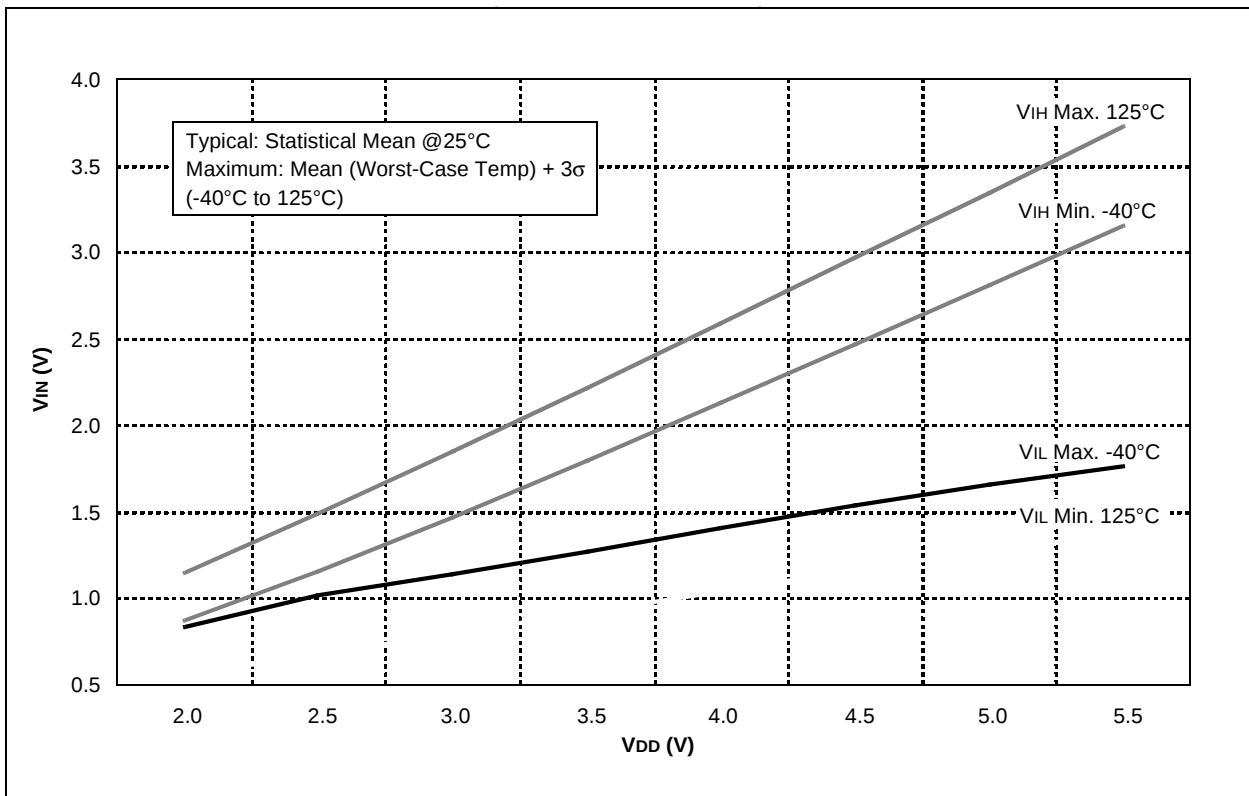


FIGURE 11-13: SCHMITT TRIGGER INPUT THRESHOLD V_{IN} vs. V_{DD}



PIC12F508/509/16F505

FIGURE 11-14: TYPICAL INTOSC FREQUENCY CHANGE vs VDD (25°C)

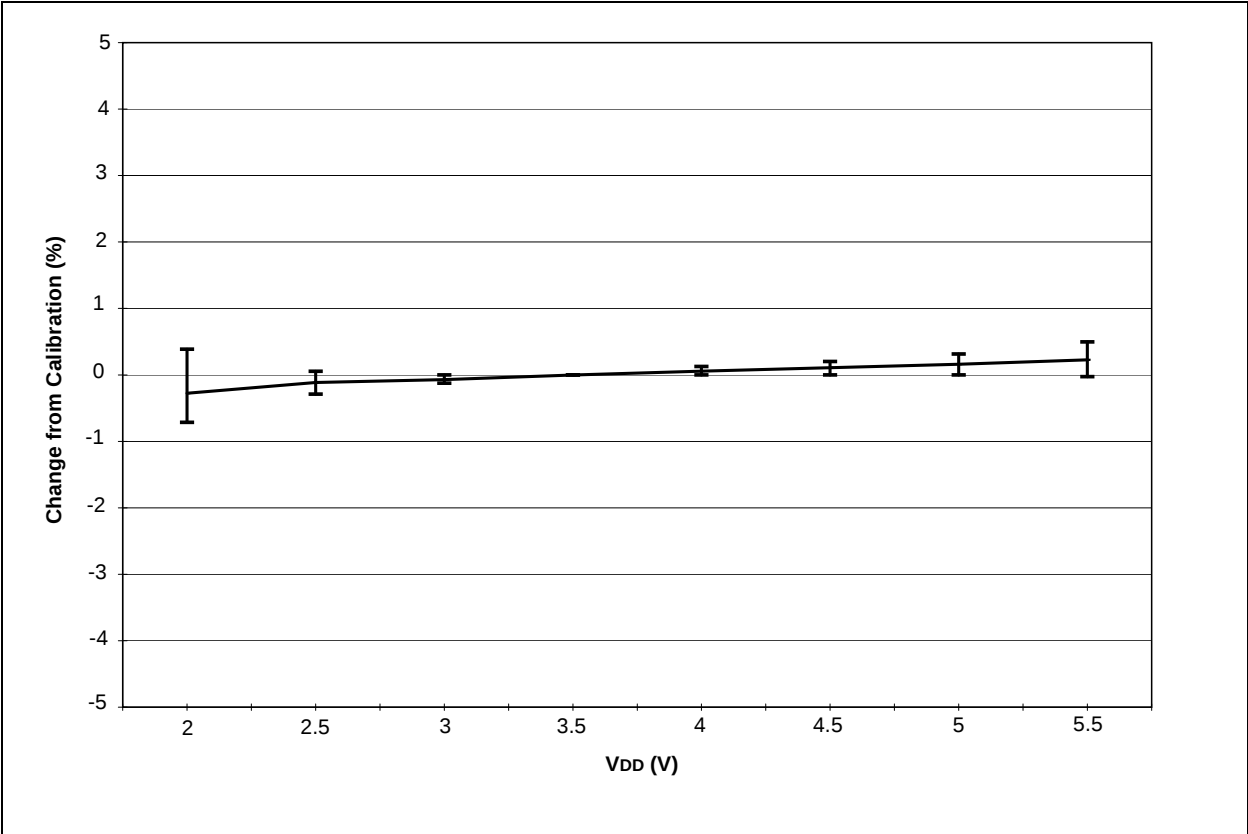
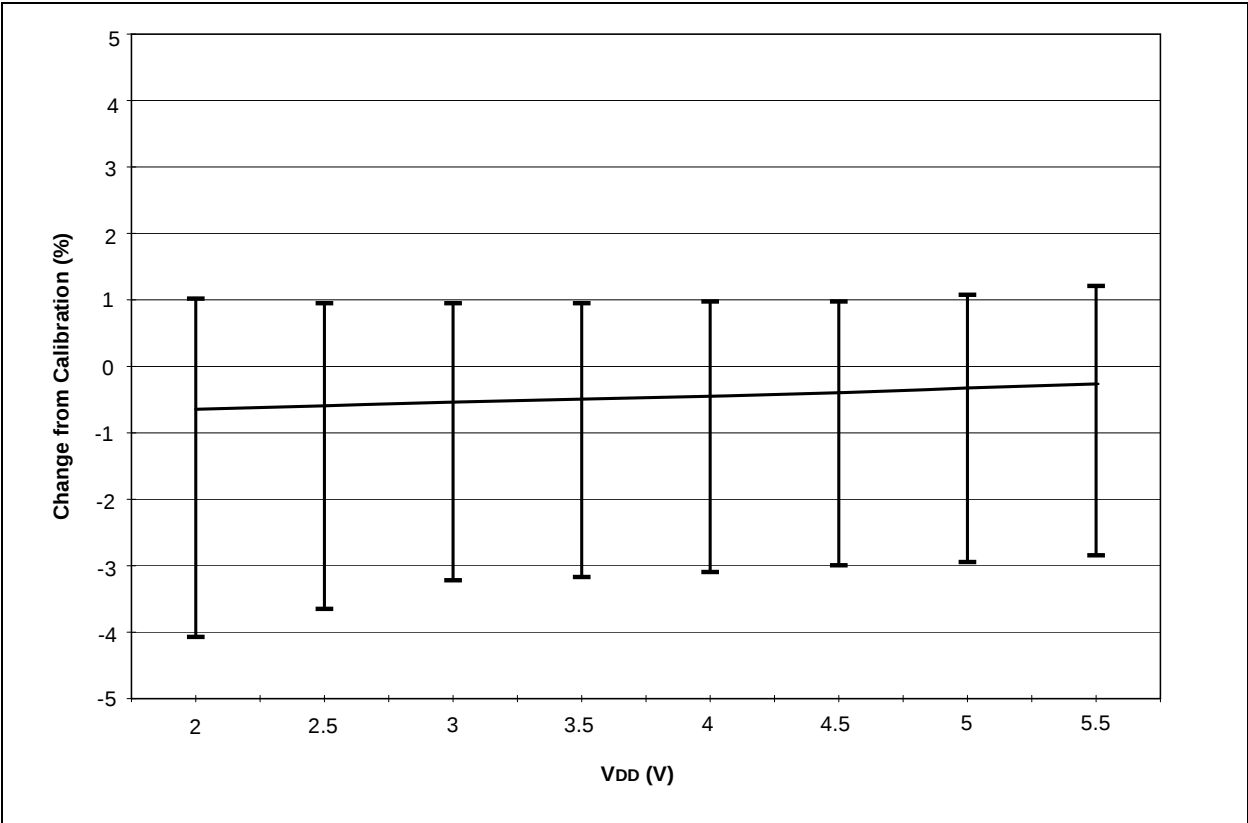
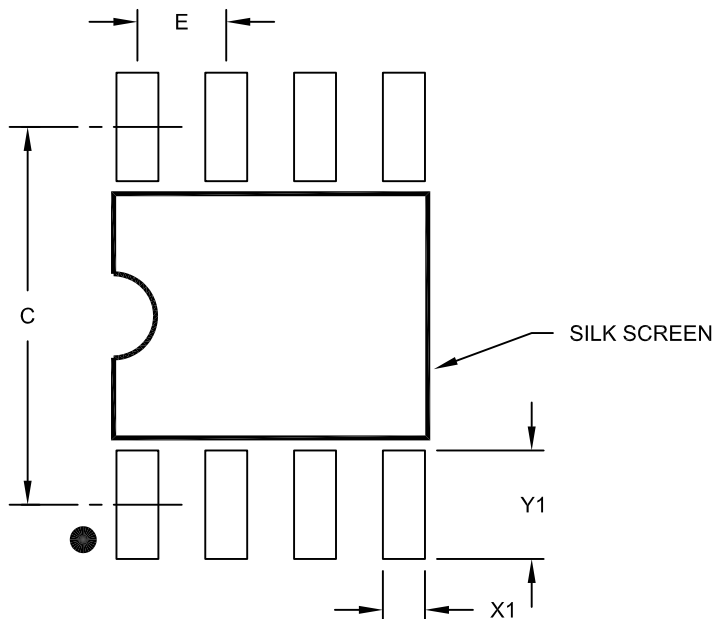


FIGURE 11-15: TYPICAL INTOSC FREQUENCY CHANGE vs VDD (-40°C)



8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

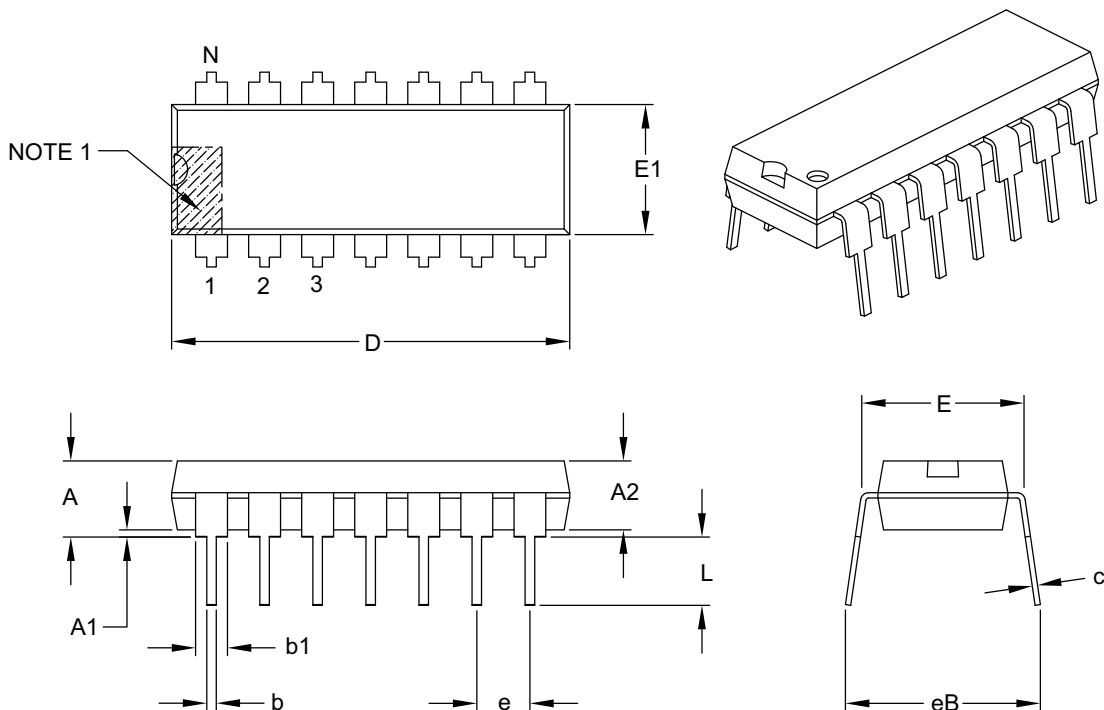
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

PIC12F508/509/16F505

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

