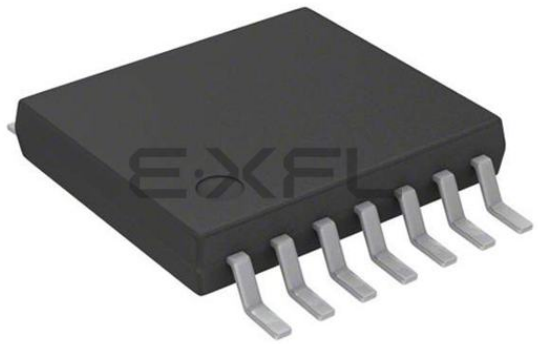

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	11
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	72 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f505t-i-st

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC12F508/509/16F505 devices can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC12F508/509/16F505 devices use a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architectures where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide, making it possible to have all single-word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle (200 ns @ 20 MHz, 1 µs @ 4 MHz) except for program branches.

Table 3-1 below lists program memory (Flash) and data memory (RAM) for the PIC12F508/509/16F505 devices.

TABLE 3-1: PIC12F508/509/16F505 MEMORY

Device	Memory	
	Program	Data
PIC12F508	512 x 12	25 x 8
PIC12F509	1024 x 12	41 x 8
PIC16F505	1024 x 12	72 x 8

The PIC12F508/509/16F505 devices can directly or indirectly address its register files and data memory. All Special Function Registers (SFR), including the PC, are mapped in the data memory. The PIC12F508/509/16F505 devices have a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation, on any register, using any addressing mode. This symmetrical nature and lack of “special optimal situations” make programming with the PIC12F508/509/16F505 devices simple, yet efficient. In addition, the learning curve is reduced significantly.

The PIC12F508/509/16F505 devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two’s complement in nature. In two-operand instructions, one operand is typically the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC) and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the `SUBWF` and `ADDWF` instructions for examples.

Simplified block diagrams are shown in Figure 3-1 and Figure 3-2, with the corresponding pin described in Table 3-2 and Table 3-3.

TABLE 3-2: PIC12F508/509 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
GP0/ICSPDAT	GP0	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	ICSPDAT	ST	CMOS	In-Circuit Serial Programming™ data pin.
GP1/ICSPCLK	GP1	TTL	CMOS	Bidirectional I/O pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	ICSPCLK	ST	CMOS	In-Circuit Serial Programming clock pin.
GP2/T0CKI	GP2	TTL	CMOS	Bidirectional I/O pin.
	T0CKI	ST	—	Clock input to TMR0.
GP3/$\overline{\text{MCLR}}$/V_{PP}	GP3	TTL	—	Input pin. Can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	$\overline{\text{MCLR}}$	ST	—	Master Clear (Reset). When configured as $\overline{\text{MCLR}}$, this pin is an active-low Reset to the device. Voltage on $\overline{\text{MCLR}}$/V_{PP} must not exceed V_{DD} during normal device operation or the device will enter Programming mode. Weak pull-up always on if configured as $\overline{\text{MCLR}}$.
	V_{PP}	HV	—	Programming voltage input.
GP4/OSC2	GP4	TTL	CMOS	Bidirectional I/O pin.
	OSC2	—	XTAL	Oscillator crystal output. Connections to crystal or resonator in Crystal Oscillator mode (XT and LP modes only, GPIO in other modes).
GP5/OSC1/CLKIN	GP5	TTL	CMOS	Bidirectional I/O pin.
	OSC1	XTAL	—	Oscillator crystal input.
	CLKIN	ST	—	External clock source input.
V_{DD}	V_{DD}	—	P	Positive supply for logic and I/O pins.
V_{SS}	V_{SS}	—	P	Ground reference for logic and I/O pins.

Legend: I = Input, O = Output, I/O = Input/Output, P = Power, — = Not used, TTL = TTL input, ST = Schmitt Trigger input, HV = High Voltage

4.3.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions to control the operation of the device (Table 4-1).

The Special Function Registers can be classified into two sets. The Special Function Registers associated with the “core” functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

TABLE 4-1: SPECIAL FUNCTION REGISTER (SFR) SUMMARY (PIC12F508/509)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset(2)	Page #
00h	INDF	Uses Contents of FSR to Address Data Memory (not a physical register)								xxxx xxxx	28
01h	TMR0	8-bit Real-Time Clock/Counter								xxxx xxxx	35
02h(1)	PCL	Low-order 8 bits of PC								1111 1111	27
03h	STATUS	GPWUF	—	PA0(5)	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0-01 1xxx(3)	22
04h	FSR	Indirect Data Memory Address Pointer								111x xxxx	28
04h(4)	FSR	Indirect Data Memory Address Pointer								110x xxxx	28
05h	OSCCAL	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	1111 111-	26
06h	GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	31
N/A	TRISGPIO	—	—	I/O Control Register						--11 1111	31
N/A	OPTION	$\overline{GPWU}$	$\overline{GPPU}$	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	24

Legend: – = unimplemented, read as ‘0’, x = unknown, u = unchanged, q = value depends on condition.

Note 1: The upper byte of the Program Counter is not directly accessible. See **Section 4.7 “Program Counter”** for an explanation of how to access these bits.

2: Other (non Power-up) Resets include external Reset through $\overline{MCLR}$, Watchdog Timer and wake-up on pin change Reset.

3: If Reset was due to wake-up on pin change, then bit 7 = 1. All other Resets will cause bit 7 = 0.

4: PIC12F509 only.

5: This bit is used on the PIC12F509. For code compatibility do not use this bit on the PIC12F508.

4.5 OPTION Register

The OPTION register is a 8-bit wide, write-only register, which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the OPTION instruction, the contents of the W register will be transferred to the OPTION register. A Reset sets the OPTION<7:0> bits.

Note: If TRIS bit is set to '0', the wake-up on change and pull-up functions are disabled for that pin (i.e., note that TRIS overrides Option control of $\overline{GPPU}$/RBPU and $\overline{GPWU}$/RBWU).

Note: If the T0CS bit is set to '1', it will override the TRIS function on the T0CKI pin.

REGISTER 4-3: OPTION REGISTER (PIC12F508/509)

W-1	W-1	W-1	W-1	W-1	W-1	W-1	W-1
$\overline{GPWU}$	$\overline{GPPU}$	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{GPWU}$:** Enable Wake-up on Pin Change bit (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 6 **$\overline{GPPU}$**: Enable Weak Pull-ups bit (GP0, GP1, GP3)
1 = Disabled
0 = Enabled

bit 5 **T0CS**: Timer0 Clock Source Select bit
1 = Transition on T0CKI pin (overrides TRIS on the T0CKI pin)
0 = Transition on internal instruction cycle clock, FOSC/4

bit 4 **T0SE**: Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on the T0CKI pin
0 = Increment on low-to-high transition on the T0CKI pin

bit 3 **PSA**: Prescaler Assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

Bit Value	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

4.9 Indirect Data Addressing: INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

4.9.1 INDIRECT ADDRESSING

- Register file 07 contains the value 10h
- Register file 08 contains the value 0Ah
- Load the value 07 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 08)
- A read of the INDR register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 4-1.

EXAMPLE 4-1: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```
        MOVLW   0x10    ;initialize pointer
        MOVWF   FSR     ;to RAM
NEXT    CLRF    INDF    ;clear INDF
                        ;register
        INCF    FSR,F   ;inc pointer
        BTFSC   FSR,4   ;all done?
        GOTO    NEXT    ;NO, clear next
CONTINUE
            :           ;YES, continue
            :
```

The FSR is a 5-bit wide register. It is used in conjunction with the INDF register to indirectly address the data memory area.

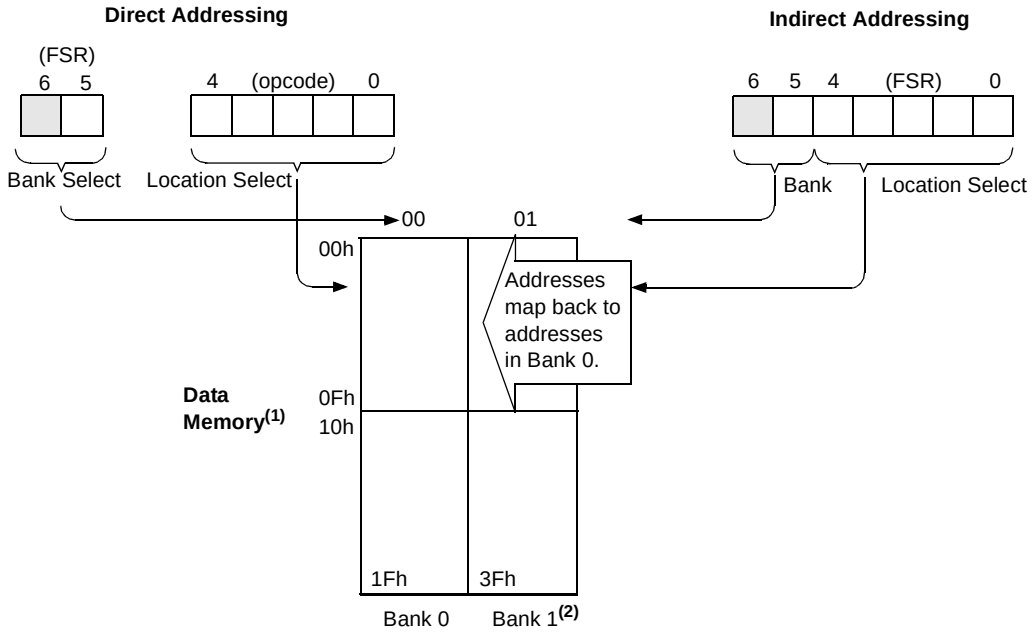
The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

PIC12F508 – Does not use banking. FSR <7:5> are unimplemented and read as '1's.

PIC12F509 – Uses FSR<5>. Selects between bank 0 and bank 1. FSR<7:6> are unimplemented, read as '1'.

PIC16F505 – Uses FSR<6:5>. Selects from bank 0 to bank 3. FSR<7> is unimplemented, read as '1'.

FIGURE 4-7: DIRECT/INDIRECT ADDRESSING (PIC12F508/509)



Note 1: For register map detail, see **Section 4.3 "Data Memory Organization"**.

2: PIC12F509.

FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

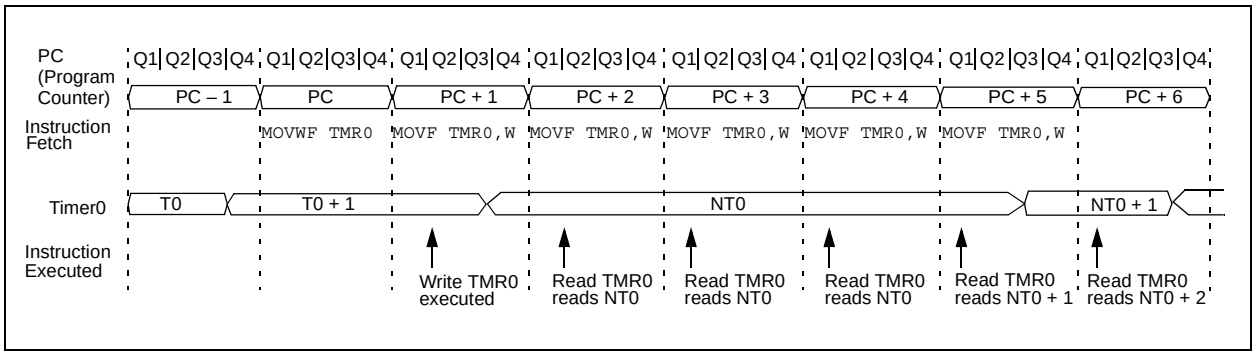


TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets
01h	TMR0	Timer0 – 8-bit Real-Time Clock/Counter								xxxx xxxx	uuuu uuuu
N/A	OPTION(1)	$\overline{\text{GPWU}}$	$\overline{\text{GPPU}}$	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
N/A	OPTION(2)	$\overline{\text{RBWU}}$	$\overline{\text{RBPU}}$	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
N/A	TRISGPIO(1), (3)	—	—	I/O Control Register						--11 1111	--11 1111
N/A	TRISC(2), (3)	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--11 1111	--11 1111

Legend: Shaded cells are not used by Timer0. – = unimplemented, x = unknown, u = unchanged.

Note 1: PIC12F508/509 only.

2: PIC16F505 only.

3: The TRIS of the T0CKI pin is overridden when T0CS = 1.

6.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module or as a postscaler for the Watchdog Timer (WDT), respectively (see **Section 7.6 "Watchdog Timer (WDT)"**). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet.

Note:	The prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT and vice versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1, x`, etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a Reset, the prescaler contains all '0's.

6.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on-the-fly" during program execution). To avoid an unintended device Reset, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0 → WDT)

```
CLRWDT              ;Clear WDT
CLRF   TMR0         ;Clear TMR0 & Prescaler
MOVLW  '00xx1111'b  ;These 3 lines (5, 6, 7)
OPTION              ;are required only if
                    ;desired
CLRWDT              ;PS<2:0> are 000 or 001
MOVLW  '00xx1xxx'b  ;Set Postscaler to
OPTION              ;desired WDT rate
```

To change the prescaler from the WDT to the Timer0 module, use the sequence shown in Example 6-2. This sequence must be used even if the WDT is disabled. A `CLRWDT` instruction should be executed before switching the prescaler.

EXAMPLE 6-2: CHANGING PRESCALER (WDT → TIMER0)

```
CLRWDT              ;Clear WDT and
                    ;prescaler
MOVLW  'xxxx0xxx'   ;Select TMR0, new
                    ;prescale value and
                    ;clock source
OPTION
```

REGISTER 7-1: CONFIGURATION WORD FOR PIC12F508/509(1)

—	—	—	—	—	—	—	MCLRE	$\overline{CP}$	WDTE	FOSC1	FOSC0
bit 11											bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 11-5 **Unimplemented**: Read as '0'

bit 4 **MCLRE:** GP3/$\overline{MCLR}$ Pin Function Select bit
1 = GP3/$\overline{MCLR}$ pin function is $\overline{MCLR}$
0 = GP3/$\overline{MCLR}$ pin function is digital input, $\overline{MCLR}$ internally tied to V_{DD}

bit 3 **$\overline{CP}$:** Code Protection bit
1 = Code protection off
0 = Code protection on

bit 2 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0 **FOSC<1:0>:** Oscillator Selection bits
11 = EXTRC = external RC oscillator
10 = INTRC = internal RC oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: Refer to the "*PIC12F508/509 Memory Programming Specifications*" (DS41227) to determine how to access the Configuration Word. The Configuration Word is not user addressable during device operation.

TABLE 7-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR – PIC12F508/509/16F505(2)

Osc Type	Resonator Freq.	Cap. Range C1	Cap. Range C2
LP	32 kHz(1)	15 pF	15 pF
XT	200 kHz 1 MHz 4 MHz	47-68 pF 15 pF 15 pF	47-68 pF 15 pF 15 pF
HS(3)	20 MHz	15-47 pF	15-47 pF

Note 1: For V_{DD} > 4.5V, C1 = C2 ≈ 30 pF is recommended.

2: These values are for design guidance only. Rs may be required to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

3: PIC16F505 only.

7.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator or a simple oscillator circuit with TTL gates can be used as an external crystal oscillator circuit. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with parallel resonance, or one with series resonance.

Figure 7-3 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometers bias the 74AS04 in the linear region. This circuit could be used for external oscillator designs.

FIGURE 7-3: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

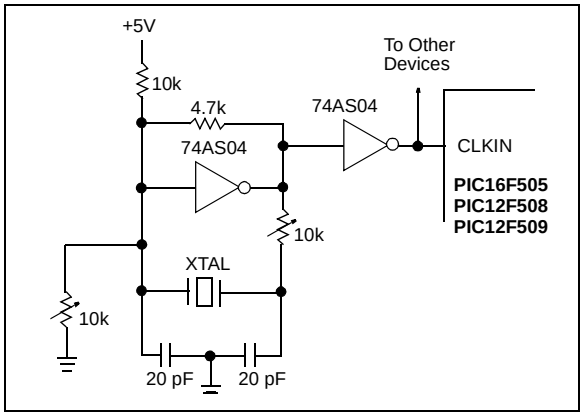
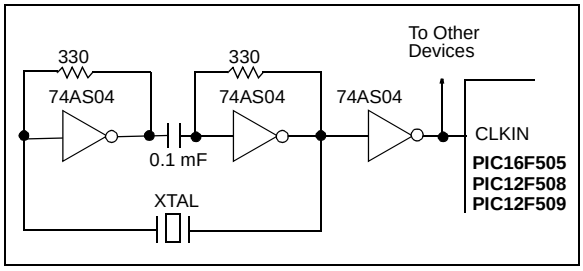


Figure 7-4 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 7-4: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



7.2.4 EXTERNAL RC OSCILLATOR

For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (R_{EXT}) and capacitor (C_{EXT}) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit-to-unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low C_{EXT} values. The user also needs to take into account variation due to tolerance of external R and C components used.

Figure 7-5 shows how the R/C combination is connected to the PIC12F508/509/16F505 devices. For R_{EXT} values below 3.0 kΩ, the oscillator operation may become unstable, or stop completely. For very high R_{EXT} values (e.g., 1 MΩ), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping R_{EXT} between 5.0 kΩ and 100 kΩ.

7.9 Power-down Mode (Sleep)

A device may be powered down (Sleep) and later powered up (wake-up from Sleep).

7.9.1 SLEEP

The Power-Down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{TO}$ bit (STATUS<4>) is set, the $\overline{PD}$ bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low or high-impedance).

Note:	A Reset generated by a WDT time-out does not drive the $\overline{MCLR}$ pin low.

For lowest current consumption while powered down, the T0CKI input should be at V_{DD} or V_{SS} and the (GP3/RB3)/$\overline{MCLR}$/V_{PP} pin must be at a logic high level if $\overline{MCLR}$ is enabled.

7.9.2 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:

1. An external Reset input on (GP3/RB3)/$\overline{MCLR}$/V_{PP} pin, when configured as $\overline{MCLR}$.
2. A Watchdog Timer time-out Reset (if WDT was enabled).
3. A change on input pin GP0/RB0, GP1/RB1, GP3/RB3 or RB4 when wake-up on change is enabled.

These events cause a device Reset. The $\overline{TO}$, $\overline{PD}$ and GPWUF/RBWUF bits can be used to determine the cause of device Reset. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up). The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked. The GPWUF/RBWUF bit indicates a change in state while in Sleep at pins GP0/RB0, GP1/RB1, GP3/RB3 or RB4 (since the last file or bit operation on GP/RB port).

Note:	**Caution:** Right before entering Sleep, read the input pins. When in Sleep, wake-up occurs when the values at the pins change from the state they were in at the last reading. If a wake-up on change occurs and the pins are not read before re-entering Sleep, a wake-up will occur immediately even if no pins change while in Sleep mode.

The WDT is cleared when the device wakes from Sleep, regardless of the wake-up source.

7.10 Program Verification/Code Protection

If the code protection bit has not been programmed, the on-chip program memory can be read out for verification purposes.

The first 64 locations and the last location (OSCCAL) can be read, regardless of the code protection bit setting.

The last memory location can be read regardless of the code protection bit setting on the PIC12F508/509/16F505 devices.

7.11 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during Program/Verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '0's.

7.12 In-Circuit Serial Programming™

The PIC12F508/509/16F505 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware, or a custom firmware, to be programmed.

The devices are placed into a Program/Verify mode by holding the GP1/RB1 and GP0/RB0 pins low while raising the $\overline{MCLR}$ (V_{PP}) pin from V_{IL} to V_{IHH} (see programming specification). GP1/RB1 becomes the programming clock and GP0/RB0 becomes the programming data. Both GP1/RB1 and GP0/RB0 are Schmitt Trigger inputs in this mode.

After Reset, a 6-bit command is then supplied to the device. Depending on the command, 14 bits of program data are then supplied to or from the device, depending if the command was a Load or a Read. For complete details of serial programming, please refer to the PIC12F508/509/16F505 Programming Specifications.

A typical In-Circuit Serial Programming connection is shown in Figure 7-15.

BTFSS	Bit Test f, Skip if Set
Syntax:	[*label*] BTFSS f,b
Operands:	0 ≤ f ≤ 31 0 ≤ b < 7
Operation:	skip if (f<b>) = 1
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', then the next instruction is skipped. If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a two-cycle instruction.

CALL	Subroutine Call
Syntax:	[*label*] CALL k
Operands:	0 ≤ k ≤ 255
Operation:	(PC) + 1→ Top-of-Stack; k → PC<7:0>; (STATUS<6:5>) → PC<10:9>; 0 → PC<8>
Status Affected:	None
Description:	Subroutine call. First, return address (PC + 1) is PUSHed onto the stack. The eight-bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two-cycle instruction.

CLRF	Clear f
Syntax:	[*label*] CLRF f
Operands:	0 ≤ f ≤ 31
Operation:	00h → (f); 1 → Z
Status Affected:	Z
Description:	The contents of register 'f' are cleared and the Z bit is set.

CLRW	Clear W
Syntax:	[*label*] CLRW
Operands:	None
Operation:	00h → (W); 1 → Z
Status Affected:	Z
Description:	The W register is cleared. Zero bit (Z) is set.

CLRWDT	Clear Watchdog Timer
Syntax:	[*label*] CLRWDT
Operands:	None
Operation:	00h → WDT; 0 → WDT prescaler (if assigned); 1 → $\overline{TO}$; 1 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

COMF	Complement f
Syntax:	[*label*] COMF f,d
Operands:	0 ≤ f ≤ 31 d ∈ [0,1]
Operation:	($\bar{f}$) → (dest)
Status Affected:	Z
Description:	The contents of register 'f' are complemented. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

9.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C18 and MPLAB C30 C Compilers
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB ASM30 Assembler/Linker/Library
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD 2
- Device Programmers
  - PICSTART® Plus Development Programmer
  - MPLAB PM3 Device Programmer
  - PICkit™ 2 Development Programmer
- Low-Cost Demonstration and Development Boards and Evaluation Kits

9.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Visual device initializer for easy register initialization
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as HI-TECH Software C Compilers and IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (assembly or C)
  - Mixed assembly and C
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

10.2 DC Characteristics: PIC12F508/509/16F505 (Extended)

DC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ TA ≤ +125°C (extended)				
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ(1)**	**Max.**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	2.0		5.5	V	See Figure 10-1
D002	VDR	**RAM Data Retention Voltage(2)**	—	1.5*	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	Vss	—	V	See **Section 7.4 "Power-on Reset (POR)"** for details
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See **Section 7.4 "Power-on Reset (POR)"** for details
D010	IDD	**Supply Current(3,4)**	— —	175 0.625	275 1.1	µA mA	FOSC = 4 MHz, VDD = 2.0V FOSC = 4 MHz, VDD = 5.0V
			— —	500 1.5	650 2.2	µA mA	FOSC = 10 MHz, VDD = 3.0V FOSC = 20 MHz, VDD = 5.0V (PIC16F515 only)
			— —	11 38	26 110	µA µA	FOSC = 32 kHz, VDD = 2.0V FOSC = 32 kHz, VDD = 5.0V
D020	IPD	**Power-down Current(5)**	— —	0.1 0.35	9.0 15.0	µA µA	VDD = 2.0V VDD = 5.0V
D022	IWDT	**WDT Current(5)**	— —	1.0 7.0	18 22	µA µA	VDD = 2.0V VDD = 5.0V

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

4: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VSS, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

5: For standby current measurements, the conditions are the same as IDD, except that the device is in Sleep mode. If a module current is listed, the current is for that specific module enabled and the device in Sleep.

TABLE 10-2: PULL-UP RESISTOR RANGES – PIC12F508/509/16F505

VDD (Volts)	Temperature (°C)	Min.	Typ.	Max.
GP0(RBO)/GP1(RB1)				
2.0	–40	73K	105K	186K
	25	73K	113K	187K
	85	82K	123K	190K
	125	86K	132k	190K
5.5	–40	15K	21K	33K
	25	15K	22K	34K
	85	19K	26k	35K
	125	23K	29K	35K
GP3(RB3)				
2.0	–40	63K	81K	96K
	25	77K	93K	116K
	85	82K	96k	116K
	125	86K	100K	119K
5.5	–40	16K	20k	22K
	25	16K	21K	23K
	85	24K	25k	28K
	125	26K	27K	29K

* These parameters are characterized but not tested.

11.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where s is a standard deviation, over each temperature range.

FIGURE 11-1: IDD vs. VDD at FOSC = 4 MHz

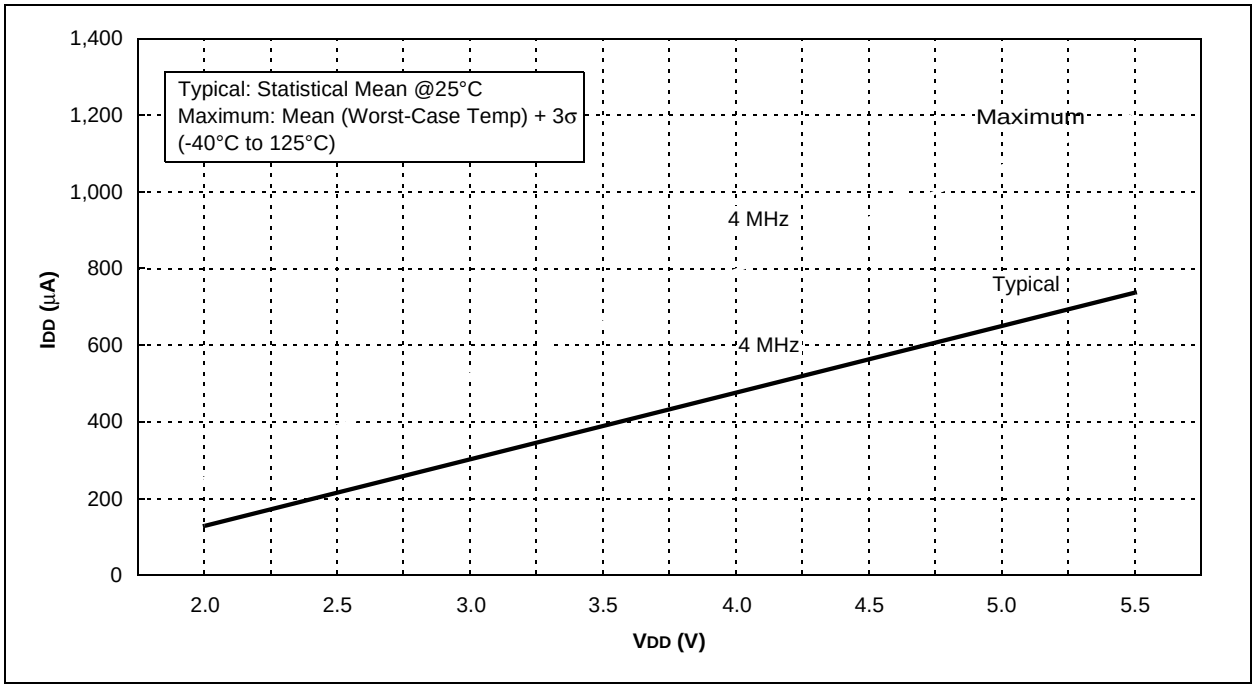


FIGURE 11-10: VOH vs. IOH OVER TEMPERATURE (VDD = 3.0V)

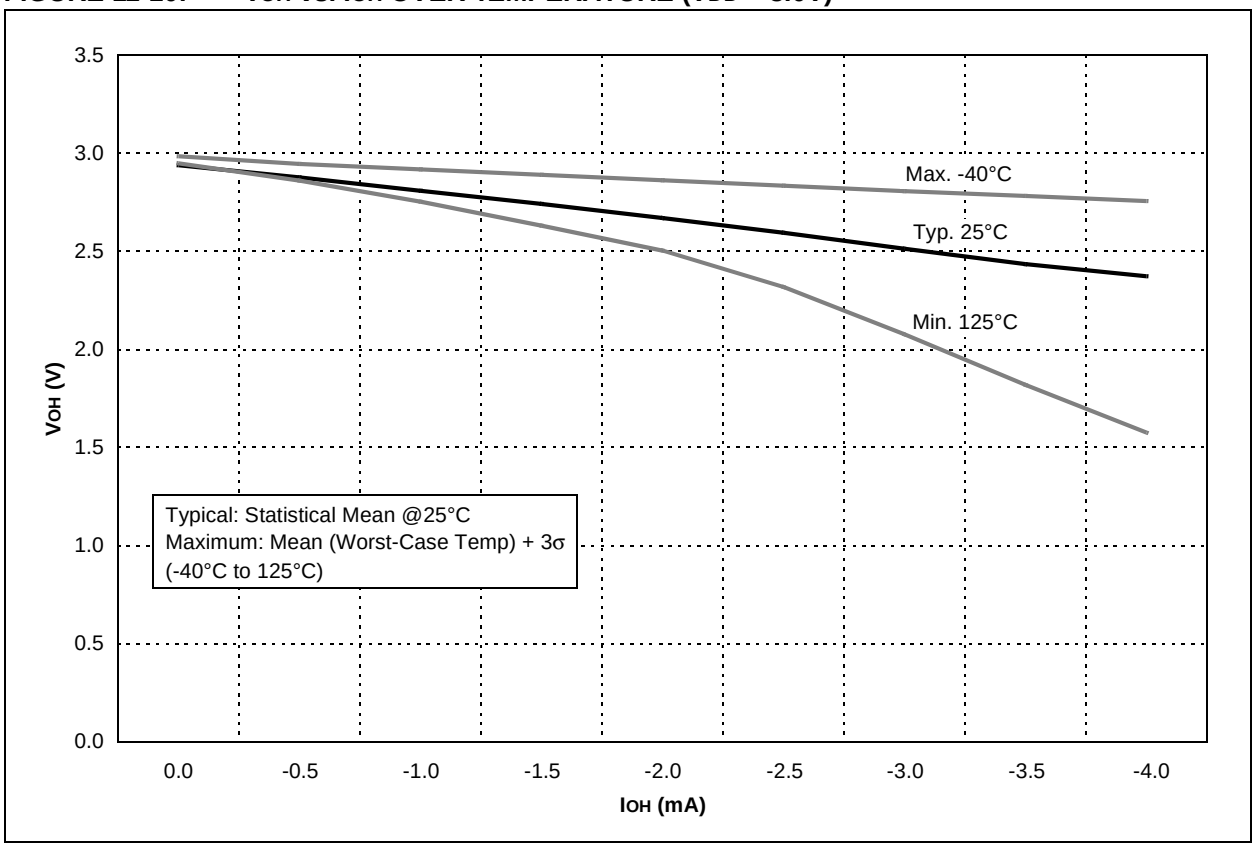
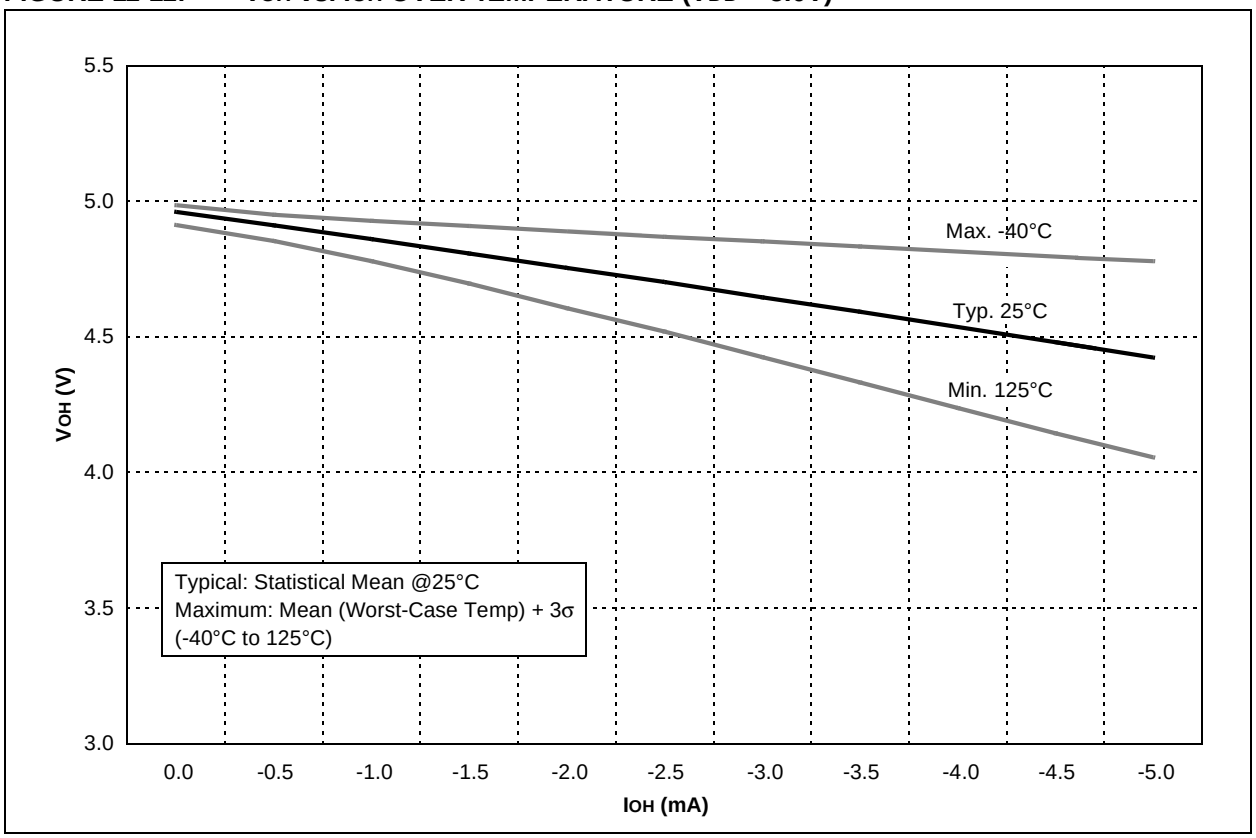


FIGURE 11-11: VOH vs. IOH OVER TEMPERATURE (VDD = 5.0V)



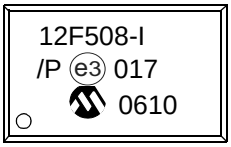
NOTES:

12.0 PACKAGING INFORMATION

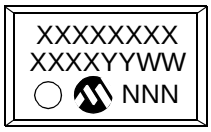
12.1 Package Marking Information

8-Lead PDIP

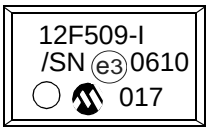
Example



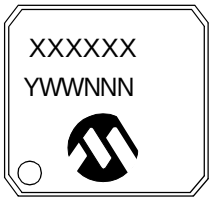
8-Lead SOIC (3.90 mm)



Example

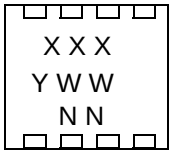


8-Lead MSOP

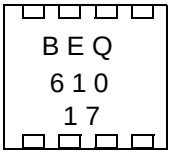


Example

8-Lead 2x3 DFN*



Example



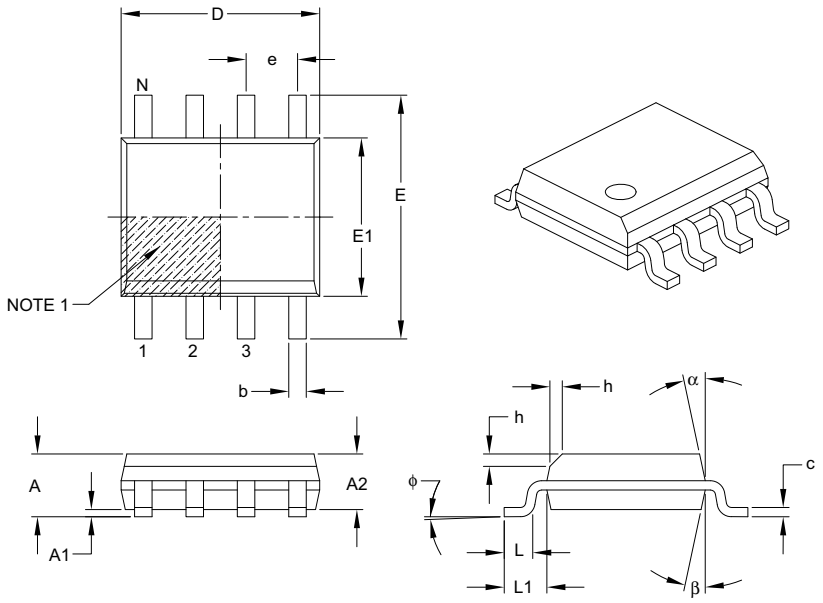
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard PIC® device marking consists of Microchip part number, year code, week code, and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device:	PIC16F505 PIC12F508 PIC12F509 PIC16F505T(1) PIC12F508T(2) PIC12F509T(2)	
Temperature Range:	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)	
Package:	MC = 8L DFN 2x3 (DUAL Flatpack No-Leads)(3, 4) MS = Micro-Small Outline Package (MSOP)(3, 4) P = Plastic (PDIP)(4) SL = 14L Small Outline, 3.90 mm (SOIC)(4) SN = 8L Small Outline, 3.90 mm Narrow (SOIC)(4) ST = Thin Shrink Small Outline (TSSOP)(4) MG = 16L QFN (3x3x0.9)(5)	
Pattern:	Special Requirements	

Note: Tape and Reel available for only the following packages: SOIC, MSOP and TSSOP.

Examples:

a) PIC12F508-E/P 301 = Extended Temp., PDIP package, QTP pattern #301

b) PIC12F508-I/SN = Industrial Temp., SOIC package

c) PIC12F508T-E/P = Extended Temp., PDIP package, Tape and Reel

Note 1: T = in tape and reel SOIC, TSSOP and QFN packages only

2: T = in tape and reel SOIC and MSOP packages only.

3: PIC12F508/PIC12F509 only.

4: Pb-free.

5: PIC16F505 only.