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## What is "Embedded - Microcontrollers"?

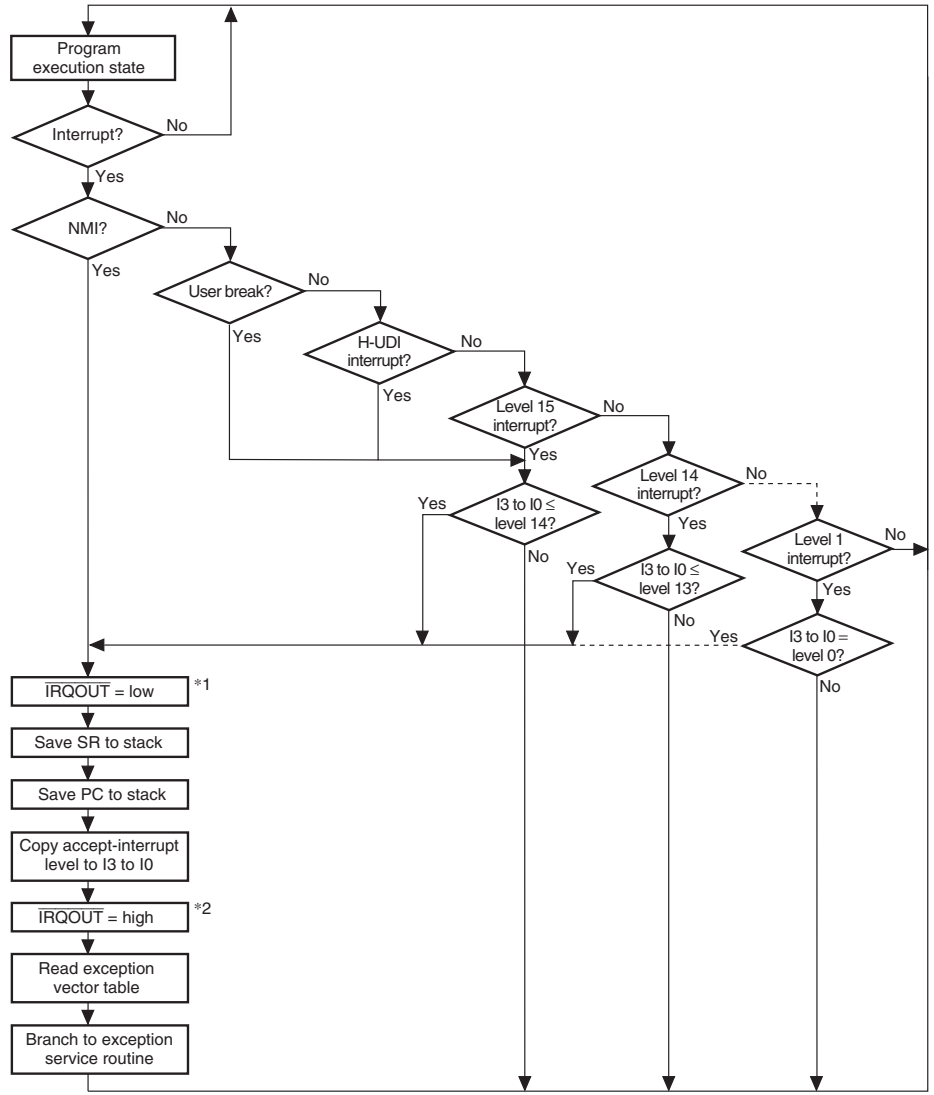
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | SH-2 |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | EBI/EMI, I²C, SCI |
| Peripherals | DMA, POR, PWM, WDT |
| Number of I/O | 74 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 75°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 112-BQFP |
| Supplier Device Package | 112-QFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/hd6417144f50v |

**Section 11 Multi-Function Timer Pulse Unit (MTU)**

the IRQ status register (ISR). Interrupts held pending due to edge detection are cleared by a power-on reset or a manual reset.




Notes: I3 to I0 are Interrupt mask bits of status register (SR) in the CPU

1. $\overline{\text{IRQOUT}}$ is the same signal as interrupt request signal to the CPU (see figure 6.1). Therefore, $\overline{\text{IRQOUT}}$ is output when the request priority level is higher than the level in bits I3–I0 of SR.
2. When the accepted interrupt is sensed by edge, a high level is output from the IRQOUT pin at the moment when the CPU starts interrupt exception processing instead of instruction execution (namely, before saving SR to stack). However, if the interrupt controller accepts an interrupt with a higher priority than the interrupt just to be accepted and has output an interrupt request to the CPU, the $\overline{\text{IRQOUT}}$ pin holds low level.

**Figure 6.3 Interrupt Sequence Flowchart**

## 9.4 Address Map

Figure 9.2 shows the address format used by this LSI.

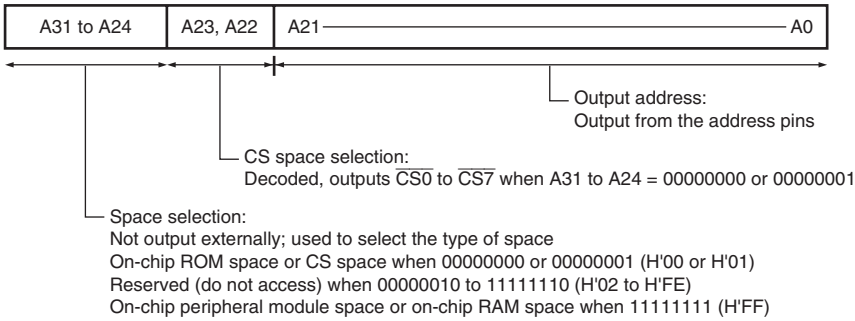



**Figure 9.2 Address Format**

This chip uses 32-bit addresses:

- Bits A31 to A24 are used to select the type of space and are not output externally.
- Bits A23 and A22 are decoded and output as chip select signals ($\overline{CS0}$ to $\overline{CS7}$) for the corresponding areas when bits A31 to A24 are 00000000 or 00000001.
- Bits A21 to A0 are output externally.

Table 9.2 shows the address map.

## 9.9 Memory Connection Example

Since A21 to A18 function as input ports at power-on reset, take the procedure such as pulling down as required.

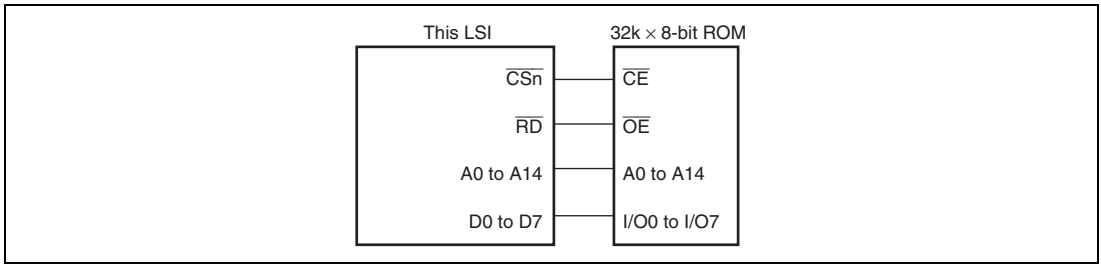



**Figure 9.10 Example of 8-bit Data Bus Width ROM Connection**

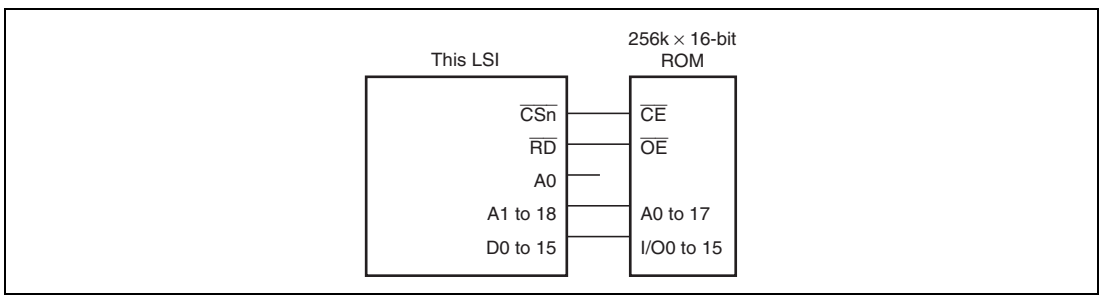



**Figure 9.11 Example of 16-bit Data Bus Width ROM Connection**

### 11.6.2 Interrupt Signal Timing

**TGF Flag Setting Timing in Case of Compare Match:** Figure 11.64 shows the timing for setting of the TGF flag in TSR on compare match, and TGI interrupt request signal timing.

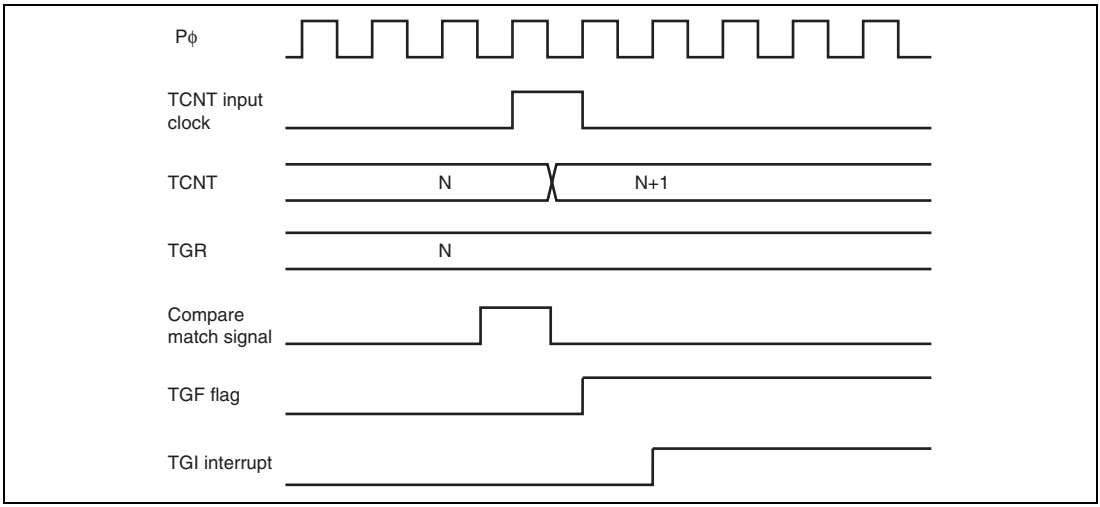



**Figure 11.64 TGI Interrupt Timing (Compare Match)**

**TGF Flag Setting Timing in Case of Input Capture:** Figure 11.65 shows the timing for setting of the TGF flag in TSR on input capture, and TGI interrupt request signal timing.

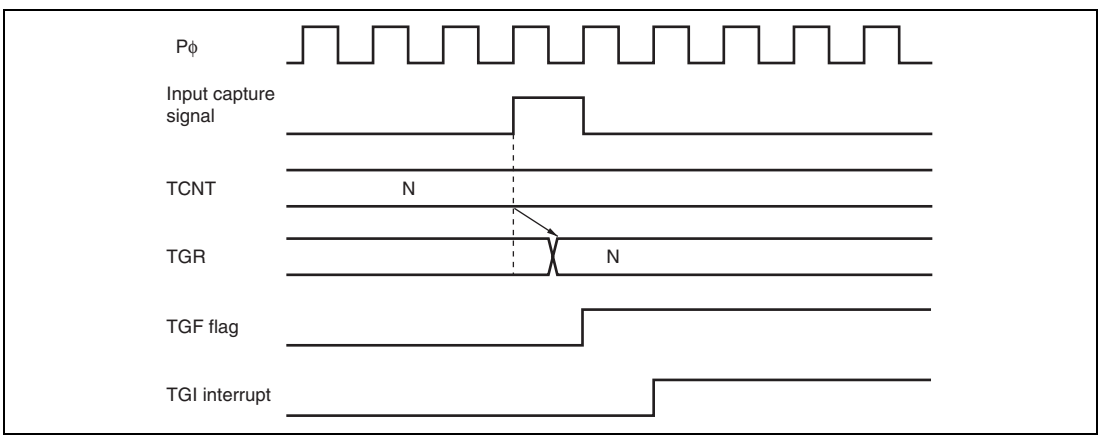



**Figure 11.65 TGI Interrupt Timing (Input Capture)**

### 11.7.10 Contention between Buffer Register Write and Input Capture

If an input capture signal is generated in the T2 state of a buffer register write cycle, the buffer operation takes precedence and the write to the buffer register is not performed.

Figure 11.78 shows the timing in this case.

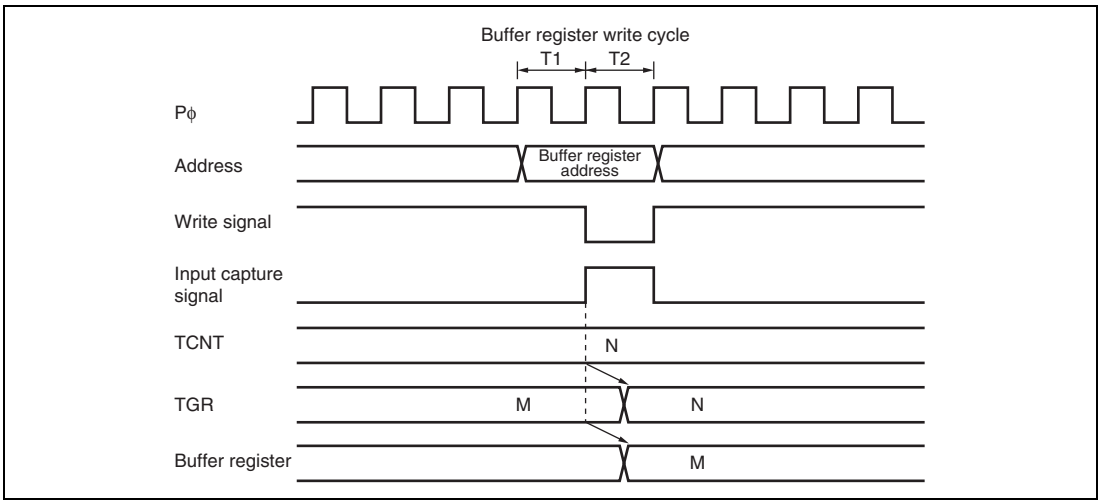



**Figure 11.78 Contention between Buffer Register Write and Input Capture**

### 11.7.11 TCNT2 Write and Overflow/Underflow Contention in Cascade Connection

With timer counters TCNT1 and TCNT2 in a cascade connection, when a contention occurs during TCNT_1 count (during a TCNT_2 overflow/underflow) in the $T_2$ state of the TCNT_2 write cycle, the write to TCNT_2 is conducted, and the TCNT_1 count signal is disabled. At this point, if there is match with TGRA_1 and the TCNT_1 value, a compare signal is issued. Furthermore, when the TCNT_1 count clock is selected as the input capture source of channel 0, TGRA_0 to D_0 carry out the input capture operation. In addition, when the compare match/input capture is selected as the input capture source of TGRB_1, TGRB_1 carries out input capture operation. The timing is shown in figure 11.79.

For cascade connections, be sure to synchronize settings for channels 1 and 2 when setting TCNT clearing.

**Operation when Error Occurs during Reset-Synchronous PWM Mode Operation, and Operation is Restarted in Complementary PWM Mode:** Figure 11.112 shows an explanatory diagram of the case where an error occurs in reset-synchronous PWM mode and operation is restarted in complementary PWM mode after re-setting.

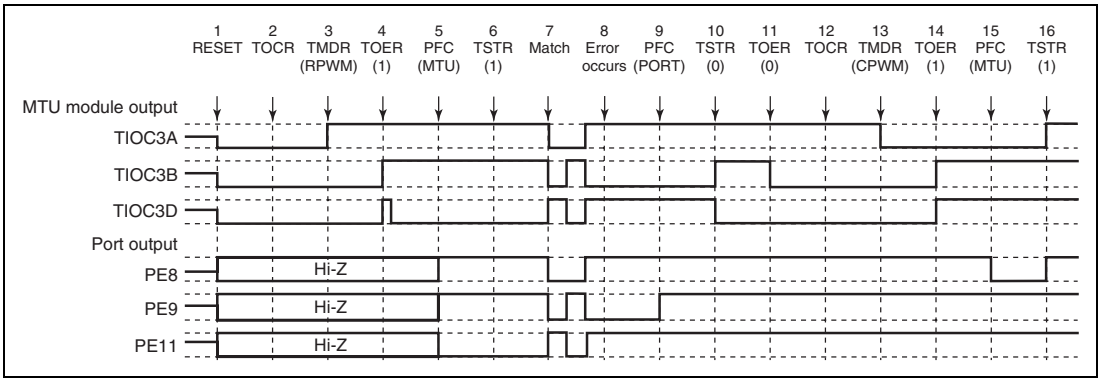



**Figure 11.112 Error Occurrence in Reset-Synchronous PWM Mode, Recovery in Complementary PWM Mode**

1 to 10 are the same as in figure 11.110.

11. Disable channel 3 and 4 output with TOER.
12. Select the complementary PWM output level and cyclic output enabling/disabling with TOCR.
13. Set complementary PWM. (The MTU cyclic output pin goes low.)
14. Enable channel 3 and 4 output with TOER.
15. Set MTU output with the PFC.
16. Operation is restarted by TSTR.

| Bit | Bit Name | Initial value | R/W | Description |
|---|---|---|---|---|
| 8 | OIE | 0 | R/W | Output Short Interrupt Enable<br>This bit makes interrupt requests when the OSF bit of the OCSR is set.<br>00: Interrupt requests disabled<br>01: Interrupt request enabled |
| 7 to 0 | — | All 0 | R | Reserved<br>These bits are always read as 0. The write value should always be 0. |

Note: * Only 0 can be written to write the flag.

### 11.9.4 Operation

**Input Level Detection Operation:**

If the input conditions set by the ICSR1 occur on any of the $\overline{\text{POE}}$ pins, all high-current pins become high-impedance state. Note however, that these high-current pins become high-impedance state only when general input/output function or MTU function is selected in these pins.

1. Falling Edge Detection

   When a change from high to low level is input to the $\overline{\text{POE}}$ pins.

2. Low-Level Detection

   Figure 11.115 shows the low-level detection operation. Sixteen continuous low levels are sampled with the sampling clock established by the ICSR1. If even one high level is detected during this interval, the low level is not accepted.

   Sampling starts when detecting the falling edge of the $\overline{\text{POE}}$ pin. Thereby, negate the $\overline{\text{POE}}$ pin when using $\overline{\text{POE}}$ function after sampling.

   Furthermore, the timing when the large-current pins enter the high-impedance state from the sampling clock is the same in both falling-edge detection and in low-level detection.

### 12.3.3 Reset Control/Status Register (RSTCSR)

RSTCSR is an 8-bit readable/writable register that controls the generation of the internal reset signal when TCNT overflows, and selects the type of internal reset signal.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | WOVF | 0 | R/(W)* | Watchdog Timer Overflow Flag<br>This bit is set when TCNT overflows in watchdog timer mode. This bit cannot be set in interval timer mode.<br>[Setting condition]<br>• Set when TCNT overflows in watchdog timer mode<br>[Clearing condition]<br>• Cleared by reading WOVF, and then writing 0 to WOVF |
| 6 | RSTE | 0 | R/W | Reset Enable<br>Specifies whether or not an internal reset signal is generated in the chip if TCNT overflows in watchdog timer mode.<br>0: Internal reset signal is not generated even if TCNT overflows<br>(Though this LSI is not reset, TCNT and TCSR in WDT are reset)<br>1: Internal reset signal is generated if TCNT overflows |
| 5 | RSTS | 0 | R/W | Reset Select<br>Selects the type of internal reset generated if TCNT overflows in watchdog timer mode.<br>0: Power-on reset<br>1: Manual reset |
| 4 to 0 | — | All 1 | R | Reserved<br>These bits are always read as 1. The write value should always be 1. |

Note: * Only 0 can be written for flag clearing.

### 12.6.3 Changing CKS2 to CKS0 Bit Values

If the values of bits CKS2 to CKS0 in the timer control/status register (TCSR) are rewritten while the WDT is running, the count may not increment correctly. Always stop the watchdog timer (by clearing the TME bit to 0) before changing the values of bits CKS2 to CKS0.

### 12.6.4 Changing between Watchdog Timer and Interval Timer Modes

To prevent incorrect operation, always stop the watchdog timer (by clearing the TME bit to 0) before switching between interval timer mode and watchdog timer mode.

### 12.6.5 System Reset by $\overline{\text{WDTOVF}}$ Signal

If a $\overline{\text{WDTOVF}}$ output signal is input to the $\overline{\text{RES}}$ pin, the chip cannot initialize correctly.

Avoid inputting the $\overline{\text{WDTOVF}}$ signal to the $\overline{\text{RES}}$ pin directly. To reset the entire system with the $\overline{\text{WDTOVF}}$ signal, use the circuit shown in figure 12.9.

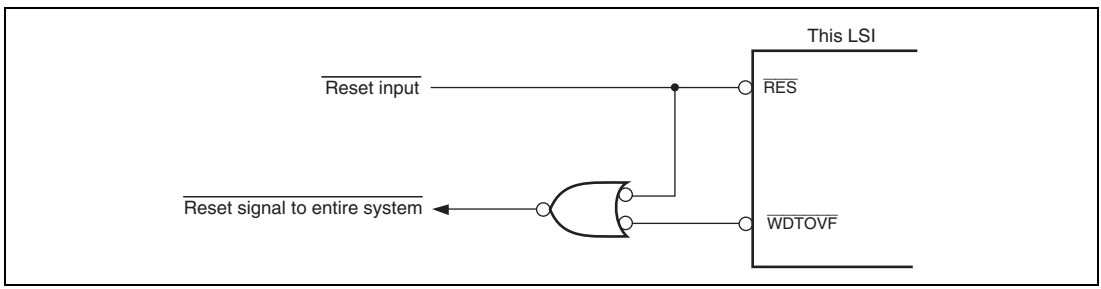



**Figure 12.9 Example of System Reset Circuit Using $\overline{\text{WDTOVF}}$ Signal**

### 12.6.6 Internal Reset in Watchdog Timer Mode

If the RSTE bit is cleared to 0 in watchdog timer mode, the chip will not be reset internally when a TCNT overflow occurs, but TCNT and TCSR in the WDT will be reset.

Table 13.11 shows the states of the SSR status flags and receive data handling when a receive error is detected. If a receive error is detected, the RDRF flag retains its state before receiving data. Reception cannot be resumed while a receive error flag is set to 1. Accordingly, clear the OER, FER, PER, and RDRF bits to 0 before resuming reception. Figure 13.9 shows a sample flow chart for serial data reception.

**Table 13.11 SSR Status Flags and Receive Data Handling**

| SSR Status Flag | | | | | |
|---|---|---|---|---|---|
| **RDRF*** | **OER** | **FER** | **PER** | **Receive Data** | **Receive Error Type** |
| 1 | 1 | 0 | 0 | Lost | Overrun error |
| 0 | 0 | 1 | 0 | Transferred to RDR | Framing error |
| 0 | 0 | 0 | 1 | Transferred to RDR | Parity error |
| 1 | 1 | 1 | 0 | Lost | Overrun error + framing error |
| 1 | 1 | 0 | 1 | Lost | Overrun error + parity error |
| 0 | 0 | 1 | 1 | Transferred to RDR | Framing error + parity error |
| 1 | 1 | 1 | 1 | Lost | Overrun error + framing error + parity error |

Note: * The RDRF flag retains its state before data reception.

# Section 14 I²C Bus Interface (IIC) Option

The I²C bus interface is an optional feature. When using this optional feature, pay attention to the following point:

- A “W” is added to the product-type name of a mask-ROM product which includes an optional feature.

This LSI incorporates a single-channel I²C bus interface. The I²C bus interface conforms to the Philips I²C bus (Inter-IC bus) interface system and provides a subset of the functions. Note, however, that the configuration of the registers that control the I²C bus differs on some points from that of Phillips’.

Data transfer is carried out by the data line (SDA0) and clock line (SCL0). This makes the interface efficient in terms of the use of area for connectors and printed circuits.

### 14.4.7 Timing for Setting IRIC and the Control of SCL

The timing with which the interrupt-request flag (IRIC) is set varies according to the settings of the WAIT bit in ICMR, FS bit in SAR, and the FSX bit in SARX. When the ICDRE and ICDRF flags are set to 1, the level on SCL is automatically set low in synchronization with the internal clock after the transfer of one frame of data. Figures 14.25 to 14.27 show the timing with which IRIC is set and the control of SCL.

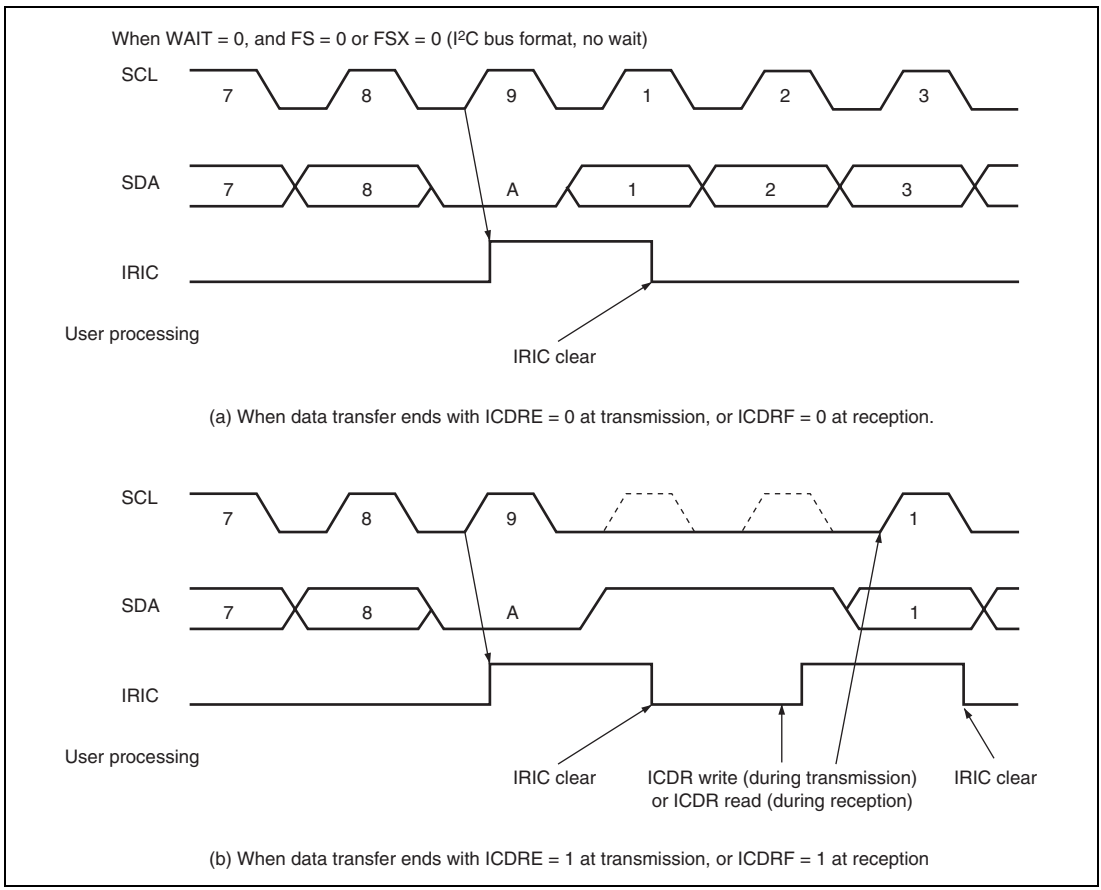



**Figure 14.25 IRIC Flag Set Timing and the Control of SCL (1)**

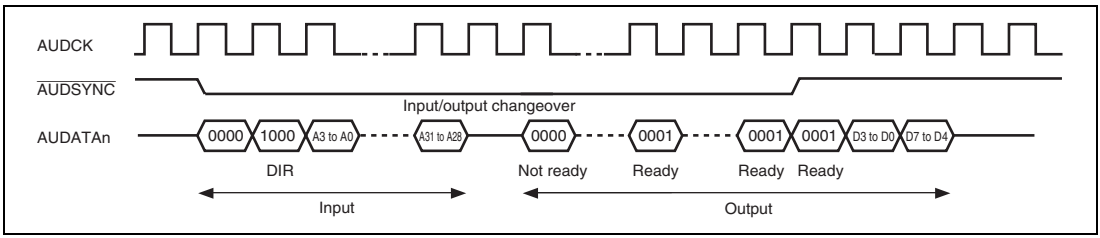



**Figure 23.5 Example of Read Operation (Byte Read)**

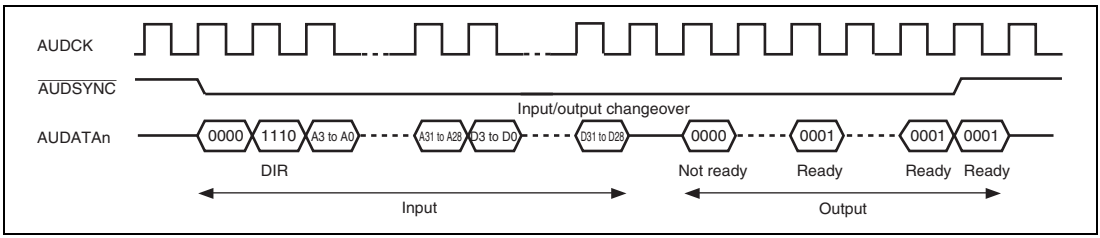



**Figure 23.6 Example of Write Operation (Longword Write)**

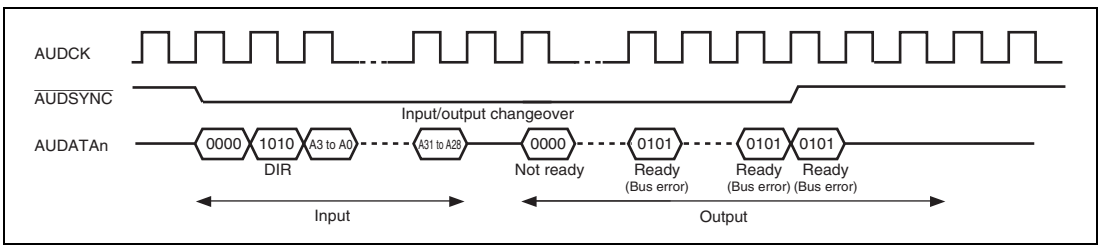



**Figure 23.7 Example of Error Occurrence (Longword Read)**

| Register abbreviation | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Module |
|---|---|---|---|---|---|---|---|---|---|
| TCR_3 | CCLR2 | CCLR1 | CCLR0 | CKEG1 | CKEG0 | TPSC2 | TPSC1 | TPSC0 | MTU |
| TCR_4 | CCLR2 | CCLR1 | CCLR0 | CKEG1 | CKEG0 | TPSC2 | TPSC1 | TPSC0 | (Channels 3, 4) |
| TMDR_3 | — | — | BFB | BFA | MD3 | MD2 | MD1 | MD0 | |
| TMDR_4 | — | — | BFB | BFA | MD3 | MD2 | MD1 | MD0 | |
| TIORH_3 | IOB3 | IOB2 | IOB1 | IOB0 | IOA3 | IOA2 | IOA1 | IOA0 | |
| TIORL_3 | IOD3 | IOD2 | IOD1 | IOD0 | IOC3 | IOC2 | IOC1 | IOC0 | |
| TIORH_4 | IOB3 | IOB2 | IOB1 | IOB0 | IOA3 | IOA2 | IOA1 | IOA0 | |
| TIORL_4 | IOD3 | IOD2 | IOD1 | IOD0 | IOC3 | IOC2 | IOC1 | IOC0 | |
| TIER_3 | TTGE | — | — | TCIEV | TGIED | TGIEC | TGIEB | TGIEA | |
| TIER_4 | TTGE | — | — | TCIEV | TGIED | TGIEC | TGIEB | TGIEA | |
| TOER | — | — | OE4D | OE4C | OE3D | OE4B | OE4A | OE3B | |
| TOCR | — | PSYE | — | — | — | — | OLSN | OLSP | |
| TGCR | — | BDC | N | P | FB | WF | VF | UF | |
| TCNT_3 | | | | | | | | | |
| TCNT_4 | | | | | | | | | |
| TCDR | | | | | | | | | |
| TDDR | | | | | | | | | |
| TGRA_3 | | | | | | | | | |
| TGRB_3 | | | | | | | | | |
| TGRA_4 | | | | | | | | | |
| TGRB_4 | | | | | | | | | |
| TCNTS | | | | | | | | | |
| TCBR | | | | | | | | | |

### 26.3.9 Serial Communication Interface (SCI) Timing

Table 26.11 shows serial communication interface timing.

**Table 26.11 Serial Communication Interface Timing**

Conditions: $V_{CC}$ = $PLLV_{CC}$ =3.3 V ± 0.3 V, $AV_{CC}$ = 3.3 V ± 0.3 V, $AV_{CC}$ = $V_{CC}$ ± 0.3 V, $AV_{ref}$ = 3.0 V to $AV_{CC}$ , $V_{SS}$ = $PLLV_{SS}$ = $AV_{SS}$ = 0 V, $T_a$ = –20°C to +75°C (regular specifications), $T_a$ = –40°C to +85°C (wide-range specifications), When programming or erasing flash memory, $T_a$ = –20°C to +75°C.

| Item | | Symbol | Min. | Max. | Unit | Figure |
|---|---|---|---|---|---|---|
| Input clock cycle (asynchronous) | | $t_{scyc}$ | 4 | — | $t_{pcyc}$ | Figure 26.19 |
| Input clock cycle (clock sync) | | $t_{scyc}$ | 6 | — | $t_{pcyc}$ | |
| Input clock pulse width | | $t_{sckw}$ | 0.4 | 0.6 | $t_{scyc}$ | |
| Input clock rise time | | $t_{sckr}$ | — | 1.5 | $t_{pcyc}$ | |
| Input clock fall time | | $t_{sckf}$ | — | 1.5 | $t_{pcyc}$ | |
| Transmit data delay time | asynchronous | $t_{TxD}$ | — | 100 | ns | Figure 26.20 |
| Received data setup time | | $t_{RxS}$ | 100 | — | ns | |
| Received data hold time | | $t_{RxH}$ | 100 | — | ns | |
| Transmit data delay time | clock sync | $t_{TxD}$ | — | $t_{pcyc}$ + 43 | ns | |
| Received data setup time | (When SCK input) | $t_{RxS}$ | $t_{pcyc}$ + 25 | — | ns | |
| Received data hold time | | $t_{RxH}$ | $t_{pcyc}$ + 25 | — | ns | |
| Transmit data delay time | clock sync | $t_{TxD}$ | — | 65 | ns | |
| Received data setup time | (When SCK output) | $t_{RxS}$ | 0.5 $t_{pcyc}$ + 50 | — | ns | |
| Received data hold time | | $t_{RxH}$ | 1.5 $t_{pcyc}$ | — | ns | |

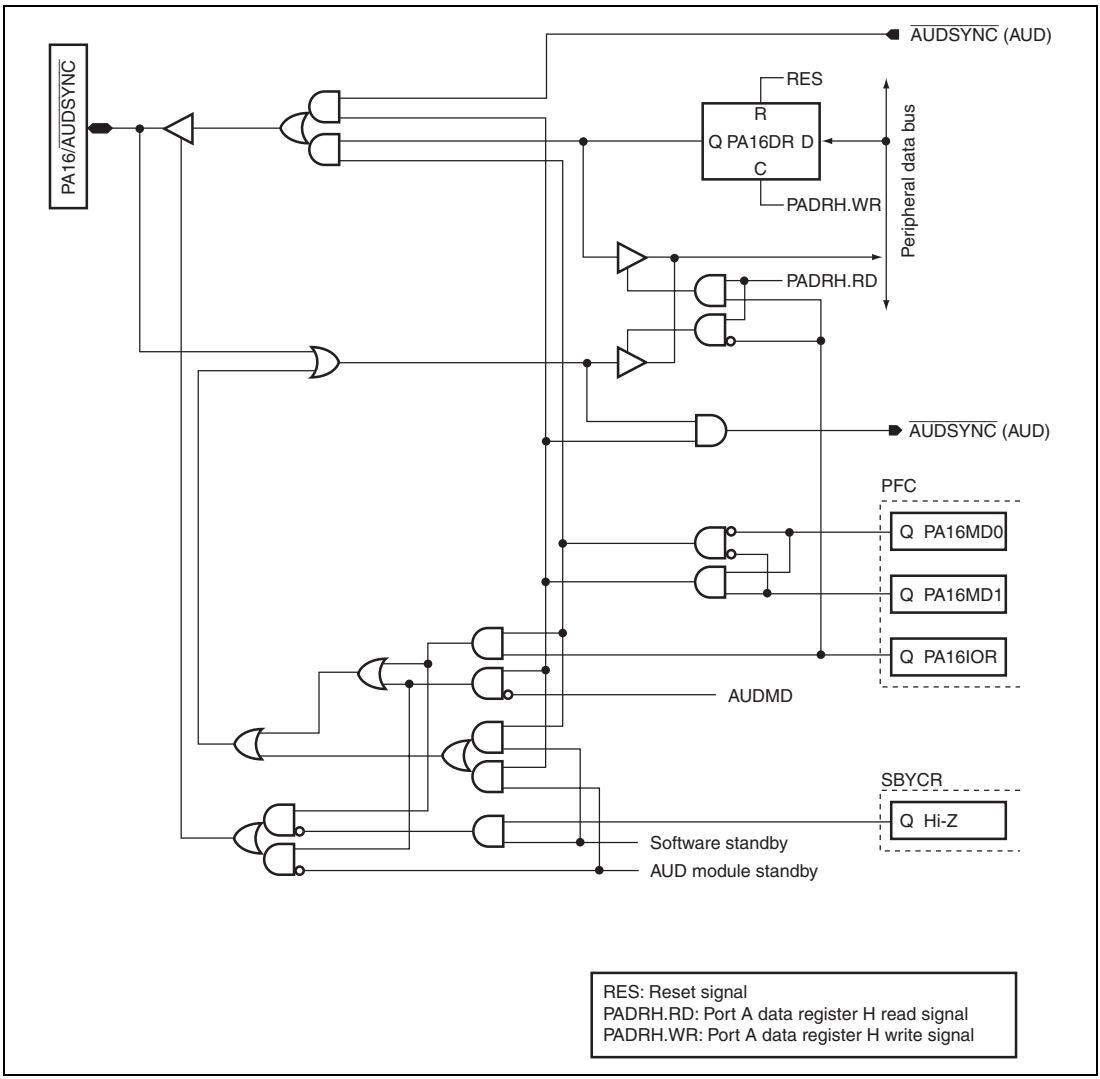
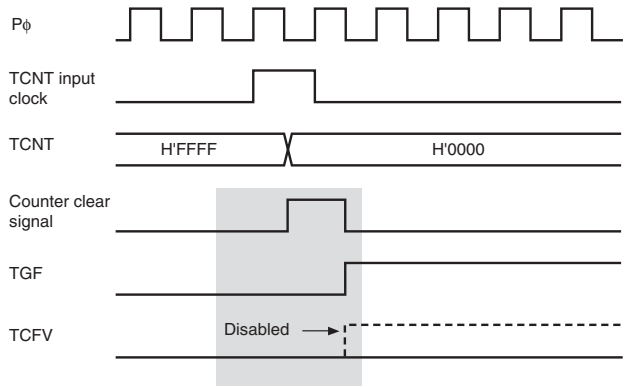
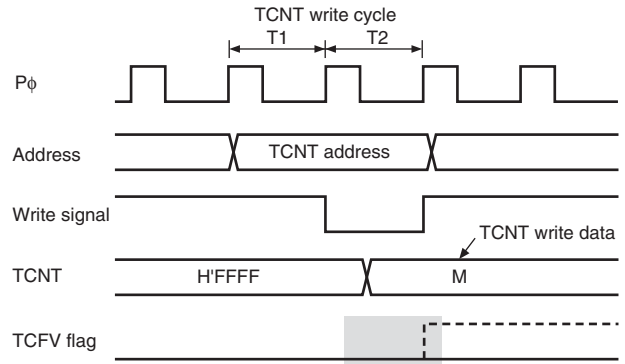



**Figure D.8 PA16/$\overline{\text{AUDSYNC}}$**

| | Symbol in Figure D.8 | | Available Products | | | |
|---|---|---|---|---|---|---|
| | | | SH7144 | | SH7145 | |
| Pins | PA16 | $\overline{\text{AUDSYNC}}$ | F-ZTAT version | Masked ROM version/ ROM less version | F-ZTAT version | Masked ROM version/ ROM less version |
| PA16/AUDSYNC | PA16 | $\overline{\text{AUDSYNC}}$ (AUD) | — | — | √ | — |

| Item | Page | Revision (See Manual for Details) |
|---|---|---|
| 11.7.16 Contention between Overflow/Underflow and Counter Clearing<br>Figure 11.83 Contention between Overflow and Counter Clearing | 333 | Figure amended<br>  |
| 11.7.17 Contention between TCNT Write and Overflow/Underflow<br>Figure 11.84 Contention between TCNT Write and Overflow | 334 | Figure amended<br>  |
| 11.7.22 Note on Buffer Operation Setting | 335 | Newly added |
| 12.1 Features | 379 | Description replaced |
| 13.4.4 SCI Initialization (Asynchronous Mode)<br>Figure 13.5 Sample SCI Initialization Flowchart | 430 | Figure replaced |