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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	98
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd6417145f50v

Global Base Register (GBR): Indicates the base address of the indirect GBR addressing mode. The indirect GBR addressing mode is used in data transfer for on-chip peripheral modules register areas and in logic operations.

Vector Base Register (VBR): Indicates the base address of the exception processing vector area.

2.2.3 System Registers

System registers consist of four 32-bit registers: high and low multiply and accumulate registers (MACH and MACL), the procedure register (PR), and the program counter (PC).

Multiply-and-Accumulate Registers (MAC): Registers to store the results of multiply-and-accumulate operations.

Procedure Register (PR): Registers to store the return address from a subroutine procedure.

Program Counter (PC): Registers to indicate the sum of current instruction addresses and four, that is, the address of the second instruction after the current instruction.

2.2.4 Initial Values of Registers

Table 2.1 lists the values of the registers after reset.

Table 2.1 Initial Values of Registers

Classification	Register	Initial Value
General registers	R0 to R14	Undefined
	R15 (SP)	Value of the stack pointer in the vector address table
Control registers	SR	Bits I3 to I0 are 1111 (H'F), reserved bits are 0, and other bits are undefined
	GBR	Undefined
	VBR	H'00000000
System registers	MACH, MACL, PR	Undefined
	PC	Value of the program counter in the vector address table

Bit	Bit Name	Initial Value	R/W	Description
3	RW1	0	R/W	Read/Write Select 1 and 0
2	RW0	0	R/W	These bits select whether to break on read and/or write cycles 00: No user break interrupt occurs 01: Break on read cycles 10: Break on write cycles 11: Break on both read and write cycles
1	SZ1	0	R/W	Operand Size Select 1 and 0*
0	SZ0	0	R/W	These bits select operand size as a break condition. 00: Operand size is not a break condition 01: Break on byte access 10: Break on word access 11: Break on longword access

Note: * When breaking on an instruction fetch, clear the SZ0 bit to 0. All instructions are considered to be accessed in word-size (even when there are instructions in on-chip memory and two instruction fetches are performed simultaneously in one bus cycle).
Operand size is word for instructions or determined by the operand size specified for the CPU/DTC, DMAC data access. It is not determined by the bus width of the space being accessed.

7.2.4 User Break Control Register (UBCR)

The user break control register (UBCR) is a 16-bit readable/writable register that enables or disables user break interrupts.

Bit	Bit Name	Initial Value	R/W	Description
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	UBID	0	R/W	User Break Disable Enables or disables user break interrupt request generation in the event of a user break condition match. 0: User break interrupt request is enabled 1: User break interrupt request is disabled

7.4 Examples of Use

Break on CPU Instruction Fetch Cycle

1. Register settings: UBARH = H'0000
   UBARL = H'0404
   UBBR = H'0054
   UBCR = H'0000

   Conditions set: Address: H'00000404
   Bus cycle: CPU, instruction fetch, read
   (operand size is not included in conditions)
   Interrupt requests enabled

   A user break interrupt will occur before the instruction at address H'00000404. If it is possible for the instruction at H'00000402 to accept an interrupt, the user break exception processing will be executed after execution of that instruction. The instruction at H'00000404 is not executed. The PC value saved is H'00000404.

2. Register settings: UBARH = H'0015
   UBARL = H'389C
   UBBR = H'0058
   UBCR = H'0000

   Conditions set: Address: H'0015389C
   Bus cycle: CPU, instruction fetch, write
   (operand size is not included in conditions)
   Interrupt requests enabled

   A user break interrupt does not occur because the instruction fetch cycle is not a write cycle.

3. Register settings: UBARH = H'0003
   UBARL = H'0147
   UBBR = H'0054
   UBCR = H'0000

   Conditions set: Address: H'00030147
   Bus cycle: CPU, instruction fetch, read
   (operand size is not included in conditions)
   Interrupt requests enabled

   A user break interrupt does not occur because the instruction fetch was performed for an even address. However, if the first instruction fetch address after the branch is an odd address set by these conditions, user break interrupt exception processing will be carried out after address error exception processing.

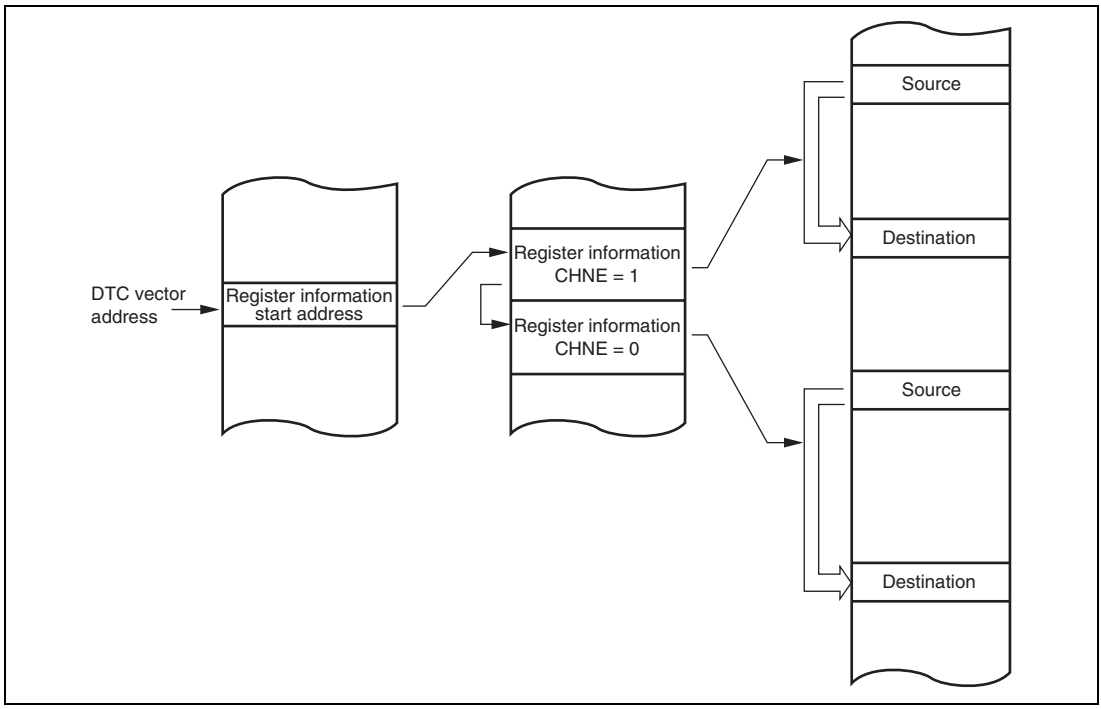

Figure 8.9 Chain Transfer

10.3.5 DMAC Operation Register (DMAOR)

The DMAOR is a 16-bit readable/writable register that specifies the transfer mode of the DMAC

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 8	PR1 PR0	0 0	R/W R/W	Priority Mode 1 and 0 These bits determine the priority level of channels for execution when transfer requests are made for several channels simultaneously. 00: CH0 > CH1 > CH2 > CH3 01: CH0 > CH2 > CH3 > CH1 10: CH2 > CH0 > CH1 > CH3 11: Round robin mode
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	AE	0	R/(W)*	Address Error Flag Indicates that an address error has occurred during DMA transfer. If this bit is set during a data transfer, transfers on all channels are suspended. The CPU cannot write a 1 to the AE bit. Clearing is effected by 0 write after 1 read. 0: No address error, DMA transfer enabled [Clearing condition] Write AE = 0 after reading AE = 1 1: Address error, DMA transfer disabled [Setting condition] Address error due to DMAC

11.2 Input/Output Pins

Table 11.2 Pin Configuration

Channel	Symbol	I/O	Function
Common	TCLKA	Input	External clock A input pin (Channel 1 phase counting mode A phase input)
	TCLKB	Input	External clock B input pin (Channel 1 phase counting mode B phase input)
	TCLKC	Input	External clock C input pin (Channel 2 phase counting mode A phase input)
	TCLKD	Input	External clock D input pin (Channel 2 phase counting mode B phase input)
0	TIOC0A	I/O	TGRA_0 input capture input/output compare output/PWM output pin
	TIOC0B	I/O	TGRB_0 input capture input/output compare output/PWM output pin
	TIOC0C	I/O	TGRC_0 input capture input/output compare output/PWM output pin
	TIOC0D	I/O	TGRD_0 input capture input/output compare output/PWM output pin
1	TIOC1A	I/O	TGRA_1 input capture input/output compare output/PWM output pin
	TIOC1B	I/O	TGRB_1 input capture input/output compare output/PWM output pin
2	TIOC2A	I/O	TGRA_2 input capture input/output compare output/PWM output pin
	TIOC2B	I/O	TGRB_2 input capture input/output compare output/PWM output pin
3	TIOC3A	I/O	TGRA_3 input capture input/output compare output/PWM output pin
	TIOC3B	I/O	TGRB_3 input capture input/output compare output/PWM output pin
	TIOC3C	I/O	TGRC_3 input capture input/output compare output/PWM output pin
	TIOC3D	I/O	TGRD_3 input capture input/output compare output/PWM output pin
4	TIOC4A	I/O	TGRA_4 input capture input/output compare output/PWM output pin
	TIOC4B	I/O	TGRB_4 input capture input/output compare output/PWM output pin
	TIOC4C	I/O	TGRC_4 input capture input/output compare output/PWM output pin
	TIOC4D	I/O	TGRD_4 input capture input/output compare output/PWM output pin

- TIORL_0, TIORL_3, TIORL_4

Bit	Bit Name	Initial Value	R/W	Description
7	IOD3	0	R/W	I/O Control D0 to D3
6	IOD2	0	R/W	Specify the function of TGRD.
5	IOD1	0	R/W	See the following tables.
4	IOD0	0	R/W	TIORL_0: Table 11.11 TIORL_3: Table 11.15 TIORL_4: Table 11.17
3	IOC3	0	R/W	I/O Control C0 to C3
2	IOC2	0	R/W	Specify the function of TGRC.
1	IOC1	0	R/W	See the following tables.
0	IOC0	0	R/W	TIORL_0: Table 11.19 TIORL_3: Table 11.23 TIORL_4: Table 11.25

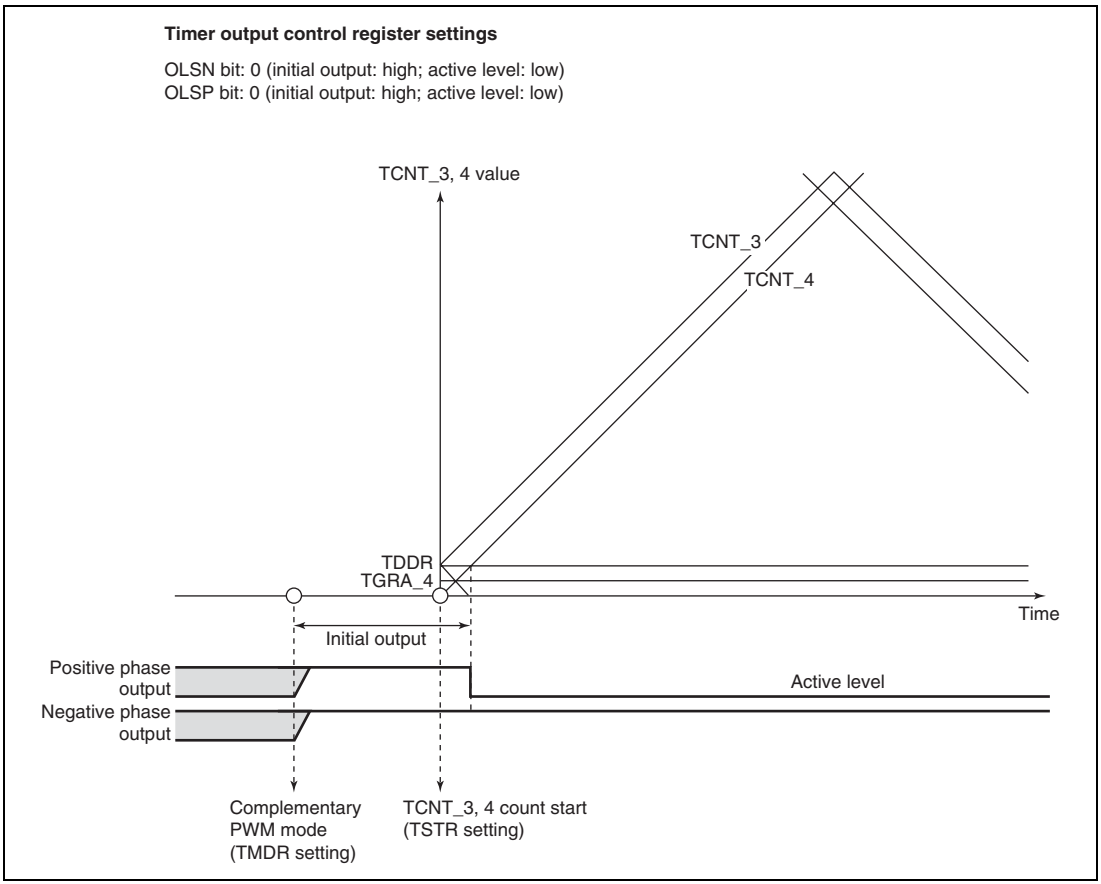

Figure 11.39 Example of Initial Output in Complementary PWM Mode (2)

Operation when Error Occurs during Complementary PWM Mode Operation, and Operation is Restarted in Reset-Synchronous PWM Mode: Figure 11.109 shows an explanatory diagram of the case where an error occurs in complementary PWM mode and operation is restarted in reset-synchronous PWM mode.

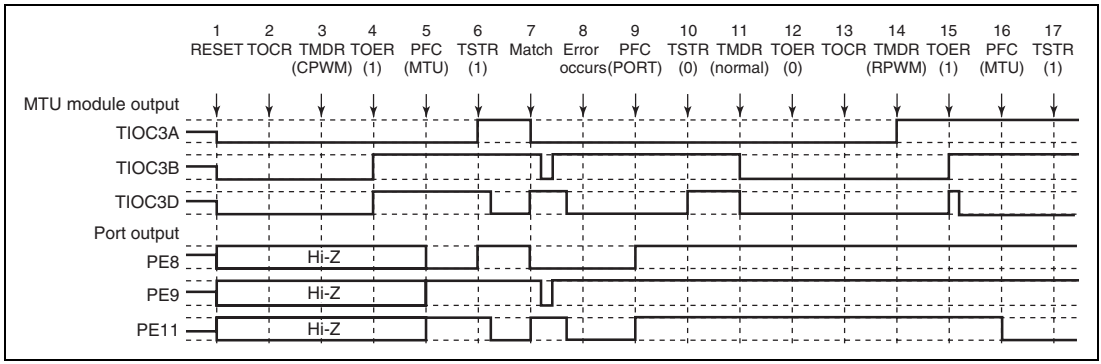

Figure 11.109 Error Occurrence in Complementary PWM Mode, Recovery in Reset-Synchronous PWM Mode

1 to 10 are the same as in figure 11.105.

11. Set normal mode. (MTU output goes low.)
12. Disable channel 3 and 4 output with TOER.
13. Select the reset-synchronous PWM mode output level and cyclic output enabling/disabling with TOCR.
14. Set reset-synchronous PWM.
15. Enable channel 3 and 4 output with TOER.
16. Set MTU output with the PFC.
17. Operation is restarted by TSTR.

Bit	Bit Name	Initial Value	R/W	Description
5	TE	0	R/W	Transmit Enable When this bit is set to 1, transmission is enabled. In this state, serial transmission is started when transmit data is written to TDR and the TDRE flag in SSR is cleared to 0. SMR setting must be made to decide the transfer format before setting the TE bit to 1. When this bit is cleared to 0, transmit operation is disabled, and the TDRE flag in SSR is fixed to 1.
4	RE	0	R/W	Receive Enable When this bit is set to 1, reception is enabled. Serial reception is started in this state when a start bit is detected in asynchronous mode or synchronous clock input is detected in clocked synchronous mode. SMR setting must be made to decide the receive format before setting the RE bit to 1. Clearing the RE bit to 0 disables reception and does not affect the RDRF, FER, PER, and ORER flags, which retain their states.
3	MPIE	0	R/W	Multiprocessor Interrupt Enable (enabled only when the MP bit in SMR is 1 in asynchronous mode) When this bit is set to 1, receive data in which the multiprocessor bit is 0 is skipped, and setting of the RDRF, FER, and ORER status flags in SSR is prohibited. On receiving data in which the multiprocessor bit is 1, this bit is automatically cleared and normal reception is resumed. For details, refer to section 13.5, Multiprocessor Communication Function. When receive data including MPB = 0 is received, receive data transfer from RSR to RDR, receive error detection, and setting of the RDRF, FER, and ORER flags in SSR, are not performed. When receive data including MPB = 1 is received, the MPB bit in SSR is set to 1, the MPIE bit is cleared to 0 automatically, and generation of RXI and ERI interrupts (when the TIE and RIE bits in SCR are set to 1) and FER and ORER flag setting are enabled.

13.4.5 Data Transmission (Asynchronous Mode)

Figure 13.6 shows an example of the operation for transmission in asynchronous mode. In transmission, the SCI operates as described below.

1. The SCI monitors the TDRE flag in SSR, and if is cleared to 0, recognizes that data has been written to TDR, and transfers the data from TDR to TSR.
2. After transferring data from TDR to TSR, the SCI sets the TDRE flag to 1 and starts transmission. If the TIE bit is set to 1 at this time, a transmit data empty interrupt request (TXI) is generated. Because the TXI interrupt routine writes the next transmit data to TDR before transmission of the current transmit data has finished, continuous transmission can be enabled.
3. Data is sent from the TxD pin in the following order: start bit, transmit data, parity bit or multiprocessor bit (may be omitted depending on the format), and stop bit.
4. The SCI checks the TDRE flag at the timing for sending the stop bit.
5. If the TDRE flag is 0, the data is transferred from TDR to TSR, the stop bit is sent, and then serial transmission of the next frame is started.
6. If the TDRE flag is 1, the TEND flag in SSR is set to 1, the stop bit is sent, and then the “mark state” is entered in which 1 is output. If the TEIE bit in SCR is set to 1 at this time, a TEI interrupt request is generated.

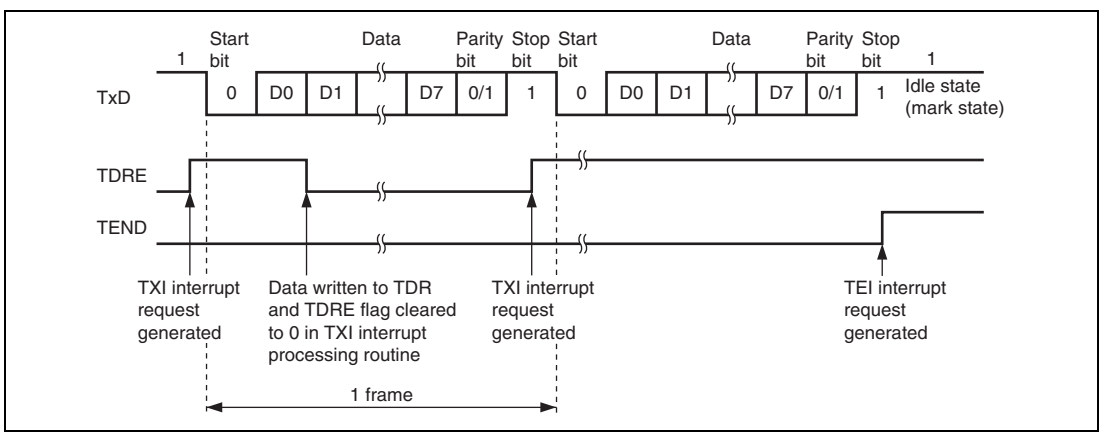

Figure 13.6 Example of Operation in Transmission in Asynchronous Mode (Example with 8-Bit Data, Parity, One Stop Bit)

Section 14 I²C Bus Interface (IIC) Option

The I²C bus interface is an optional feature. When using this optional feature, pay attention to the following point:

- A “W” is added to the product-type name of a mask-ROM product which includes an optional feature.

This LSI incorporates a single-channel I²C bus interface. The I²C bus interface conforms to the Philips I²C bus (Inter-IC bus) interface system and provides a subset of the functions. Note, however, that the configuration of the registers that control the I²C bus differs on some points from that of Phillips’.

Data transfer is carried out by the data line (SDA0) and clock line (SCL0). This makes the interface efficient in terms of the use of area for connectors and printed circuits.

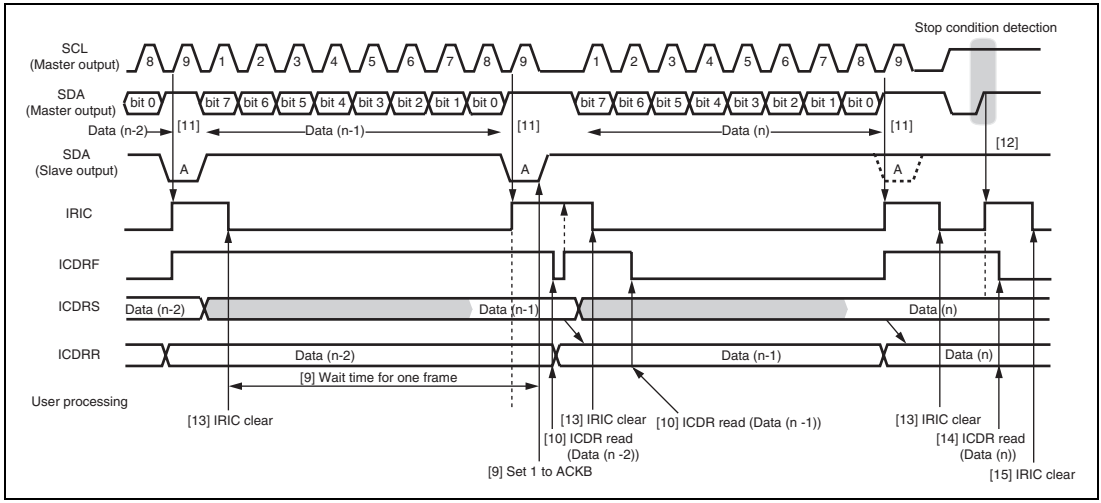

Figure 14.22 An Example of the Timing of Operations in Slave Receive Mode 2 (MLS = ACKB = 0, HNDS = 0)

Register	Bit	Bit Name	Initial Value	R/W	Description
PCCR	11	PC11MD	0*	R/W	PC11 Mode Selects the function of the PC11/A11 pin. 0: PC11 I/O (port) 1: A11 output (BSC)
PCCR	10	PC10MD	0*	R/W	PC10 Mode Selects the function of the PC10/A10 pin. 0: PC10 I/O (port) 1: A10 output (BSC)
PCCR	9	PC9MD	0*	R/W	PC9 Mode Selects the function of the PC9/A9 pin. 0: PC9 I/O (port) 1: A9 output (BSC)
PCCR	8	PC8MD	0*	R/W	PC8 Mode Selects the function of the PC8/A8 pin. 0: PC8 I/O (port) 1: A8 output (BSC)
PCCR	7	PC7MD	0*	R/W	PC7 Mode Selects the function of the PC7/A7 pin. 0: PC7 I/O (port) 1: A7 output (BSC)
PCCR	6	PC6MD	0*	R/W	PC6 Mode Selects the function of the PC6/A6 pin. 0: PC6 I/O (port) 1: A6 output (BSC)
PCCR	5	PC5MD	0*	R/W	PC5 Mode Selects the function of the PC5/A5 pin. 0: PC5 I/O (port) 1: A5 output (BSC)
PCCR	4	PC4MD	0*	R/W	PC4 Mode Selects the function of the PC4/A4 pin. 0: PC4 I/O (port) 1: A4 output (BSC)

- Port E Control Registers L1 and L2 (PECRL1 and PECRL2) in SH7145

Register	Bit	Bit Name	Initial Value	R/W	Description
PECRL1	15	PE15MD1	0	R/W	PE15 Mode
PECRL1	14	PE15MD0	0	R/W	Select the function of the PE15/TIOC4D/DACK1/$\overline{\text{IRQOUT}}$ pin. 00: PE15 I/O (port) 01: TIOC4D I/O (MTU) 10: DACK1 output (DMAC) 11: $\overline{\text{IRQOUT}}$ output (INTC)
PECRL1	13	PE14MD1	0	R/W	PE14 Mode
PECRL1	12	PE14MD0	0	R/W	Select the function of the PE14/TIOC4C/DACK0 pin. 00: PE14 I/O (port) 01: TIOC4C I/O (MTU) 10: DACK0 output (DMAC) 11: Setting prohibited
PECRL1	11	PE13MD1	0	R/W	PE13 Mode
PECRL1	10	PE13MD0	0	R/W	Select the function of the PE13/TIOC4B/$\overline{\text{MRES}}$ pin. 00: PE13 I/O (port) 01: TIOC4B I/O (MTU) 10: $\overline{\text{MRES}}$ input (INTC) 11: Setting prohibited
PECRL1	9	PE12MD1	0	R/W	PE12 Mode
PECRL1	8	PE12MD0	0	R/W	Select the function of the PE12/TIOC4A/TCK/TXD3 pin. Fixed to TCK input when using E10A (in DBGMD = high).* 00: PE12 I/O (port) 01: TIOC4A I/O (MTU) 10: Setting prohibited 11: TXD3 output (SCI)

22.1.2 Block Diagram

Figure 22.1 shows a block diagram of the H-UDI.

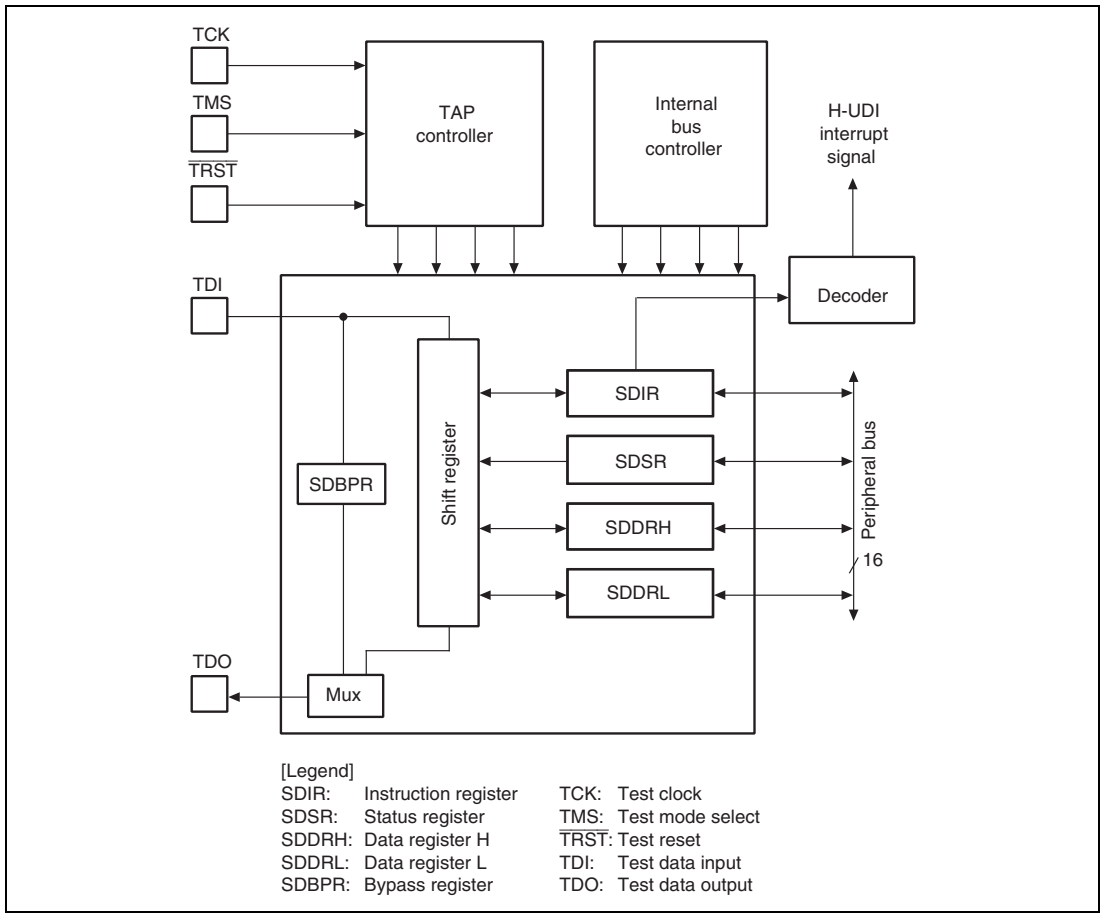

Figure 22.1 H-UDI Block Diagram

Register name	abbreviation	NO. of bits	Address	Module	Access size	NO. of Access states
Flash memory control register 1	FLMCR1	8	H'FFFF8580	FLASH	8, 16	φ reference
Flash memory control register 2	FLMCR2	8	H'FFFF8581	(Only in F-ZTAT version)	8	B:3
Erase block register 1	EBR1	8	H'FFFF8582		8, 16	W:6
Erase block register 2	EBR2	8	H'FFFF8583		8	
—	—	—	H'FFFF8584 to H'FFFF85FF		—	
User break address register H	UBARH	16	H'FFFF8600	UBC	8, 16, 32	φ reference
User break address register L	UBARL	16	H'FFFF8602		8, 16	B:3
User break address mask register H	UBAMRH	16	H'FFFF8604		8, 16, 32	W:3
User break address mask register L	UBAMRL	16	H'FFFF8606		8, 16	L:6
User break bus cycle register	UBBR	16	H'FFFF8608		8, 16, 32	
User break control register	UBCR	16	H'FFFF860A		8, 16	
—	—	—	H'FFFF860C to H'FFFF860F		—	
Timer control/status register	TCSR	8	H'FFFF8610	WDT	8*2/16*1	φ reference
Timer counter	TCNT*1	8	H'FFFF8610	*1: Write	16	B:3
Timer counter	TCNT*2	8	H'FFFF8611	*2: Read	8	W:3
Reset control/status register	RSTCSR*1	8	H'FFFF8612		16	
Reset control/status register	RSTCSR*2	8	H'FFFF8613		8	
Standby control register	SBYCR	8	H'FFFF8614	Power-down modes	8	φ reference
						B:3
—	—	—	H'FFFF8615 to H'FFFF8617	—	—	—
System control register	SYSCR	8	H'FFFF8618	Power-down modes	8	Pφ reference
—	—	—	H'FFFF8619 to H'FFFF861B		—	B:3
						W:3
Module standby control register 1	MSTCR1	16	H'FFFF861C		8, 16, 32	L:6
Module standby control register 2	MSTCR2	16	H'FFFF861E		8, 16	

Register name	abbreviation	NO. of bits	Address	Module	Access size	NO. of Access states
Bus control register 1	BCR1	16	H'FFFF8620	BSC	8, 16, 32	ϕ reference
Bus control register 2	BCR2	16	H'FFFF8622		8, 16	B:3
Wait control register 1	WCR1	16	H'FFFF8624		8, 16, 32	W:3
Wait control register 2	WCR2	16	H'FFFF8626		8, 16	L:6
RAM emulation register	RAMER	16	H'FFFF8628	FLASH (Only in F-ZTAT version)	8, 16	ϕ reference B:3 W:3
—	—	—	H'FFFF862A to H'FFFF86AF	—	—	—
DMA operation register	DMAOR	16	H'FFFF86B0	DMAC (for all channels)	8, 16	ϕ reference
—	—	—	H'FFFF86B2 to H'FFFF86BF		—	W:3 L:6
DMA source address register_0	SAR_0	32	H'FFFF86C0	DMAC (Channel 0)	8, 16, 32	
DMA destination address register_0	DAR_0	32	H'FFFF86C4		8, 16, 32	
DMA transfer count register_0	DMATCR_0	32	H'FFFF86C8		8, 16, 32	
DMA channel control register_0	CHCR_0	32	H'FFFF86CC		8, 16, 32	
DMA source address register_1	SAR_1	32	H'FFFF86D0	DMAC (Channel 1)	8, 16, 32	
DMA destination address register_1	DAR_1	32	H'FFFF86D4		8, 16, 32	
DMA transfer count register_1	DMATCR_1	32	H'FFFF86D8		8, 16, 32	
DMA channel control register_1	CHCR_1	32	H'FFFF86DC		8, 16, 32	
DMA source address register_2	SAR_2	32	H'FFFF86E0	DMAC (Channel 2)	8, 16, 32	
DMA destination address register_2	DAR_2	32	H'FFFF86E4		8, 16, 32	
DMA transfer count register_2	DMATCR_2	32	H'FFFF86E8		8, 16, 32	
DMA channel control register_2	CHCR_2	32	H'FFFF86EC		8, 16, 32	
DMA source address register_3	SAR_3	32	H'FFFF86F0	DMAC (Channel 3)	8, 16, 32	
DMA destination address register_3	DAR_3	32	H'FFFF86F4		8, 16, 32	
DMA transfer count register_3	DMATCR_3	32	H'FFFF86F8		8, 16, 32	
DMA channel control register_3	CHCR_3	32	H'FFFF86FC		8, 16, 32	

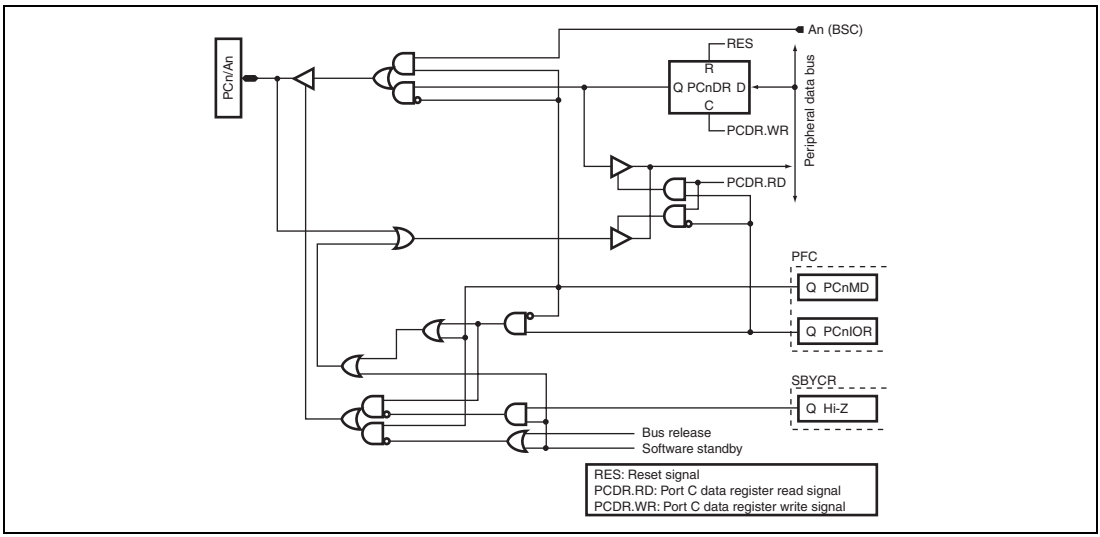

Figure D.22 PCn/An

	Symbol in Figure D.22		Available Products			
			SH7144		SH7145	
Pins	PCn	An	F-ZTAT version	Masked ROM version/ ROM less version	F-ZTAT version	Masked ROM version/ ROM less version
PC0/A0	PC0	A0 (BSC)	√	√	√	√
PC1/A1	PC1	A1 (BSC)	√	√	√	√
PC2/A2	PC2	A2 (BSC)	√	√	√	√
PC3/A3	PC3	A3 (BSC)	√	√	√	√
PC4/A4	PC4	A4 (BSC)	√	√	√	√
PC5/A5	PC5	A5 (BSC)	√	√	√	√
PC6/A6	PC6	A6 (BSC)	√	√	√	√
PC7/A7	PC7	A7 (BSC)	√	√	√	√
PC8/A8	PC8	A8 (BSC)	√	√	√	√
PC9/A9	PC9	A9 (BSC)	√	√	√	√
PC10/A10	PC10	A10 (BSC)	√	√	√	√
PC11/A11	PC11	A11 (BSC)	√	√	√	√
PC12/A12	PC12	A12 (BSC)	√	√	√	√
PC13/A13	PC13	A13 (BSC)	√	√	√	√
PC14/A14	PC14	A14 (BSC)	√	√	√	√
PC15/A15	PC15	A15 (BSC)	√	√	√	√