Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SCI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	98
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f7145fw50v

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Figure 11.25 Example of Phase Counting Mode 1 Operation 277
Figure 11.26 Example of Phase Counting Mode 2 Operation 278
Figure 11.27 Example of Phase Counting Mode 3 Operation 279
Figure 11.28 Example of Phase Counting Mode 4 Operation 280
Figure 11.29 Phase Counting Mode Application Example 281
Figure 11.30 Procedure for Selecting Reset-Synchronized PWM Mode 283
Figure 11.31 Reset-Synchronized PWM Mode Operation Example
(When TOCR's OLSN = 1 and OLSP = 1) 284
Figure 11.32 Block Diagram of Channels 3 and 4 in Complementary PWM Mode 287
Figure 11.33 Example of Complementary PWM Mode Setting Procedure 288
Figure 11.34 Complementary PWM Mode Counter Operation 290
Figure 11.35 Example of Complementary PWM Mode Operation 292
Figure 11.36 Example of PWM Cycle Updating 294
Figure 11.37 Example of Data Update in Complementary PWM Mode 296
Figure 11.38 Example of Initial Output in Complementary PWM Mode (1) 297
Figure 11.39 Example of Initial Output in Complementary PWM Mode (2) 298
Figure 11.40 Example of Complementary PWM Mode Waveform Output (1) 300
Figure 11.41 Example of Complementary PWM Mode Waveform Output (2) 300
Figure 11.42 Example of Complementary PWM Mode Waveform Output (3) 301
Figure 11.43 Example of Complementary PWM Mode 0% and 100% Waveform Output
(1) 301
Figure 11.44 Example of Complementary PWM Mode 0% and 100% Waveform Output
(2) 302
Figure 11.45 Example of Complementary PWM Mode 0% and 100% Waveform Output
(3) 302
Figure 11.46 Example of Complementary PWM Mode 0% and 100% Waveform Output
(4) 303
Figure 11.47 Example of Complementary PWM Mode 0% and 100% Waveform Output
(5) 303
Figure 11.48 Example of Toggle Output Waveform Synchronized with PWM Output 304
Figure 11.49 Counter Clearing Synchronized with Another Channel 305
Figure 11.50 Example of Output Phase Switching by External Input (1) 306
Figure 11.51 Example of Output Phase Switching by External Input (2) 307
Figure 11.52 Example of Output Phase Switching by Means of UF, VF, WF Bit Settings
(1) 307
Figure 11.53 Example of Output Phase Switching by Means of UF, VF, WF Bit Settings
(2) 308
Figure 11.54 Count Timing in Internal Clock Operation 313
Figure 11.55 Count Timing in External Clock Operation 313
Figure 11.56 Count Timing in External Clock Operation (Phase Counting Mode) 313

1.2 Internal Block Diagram

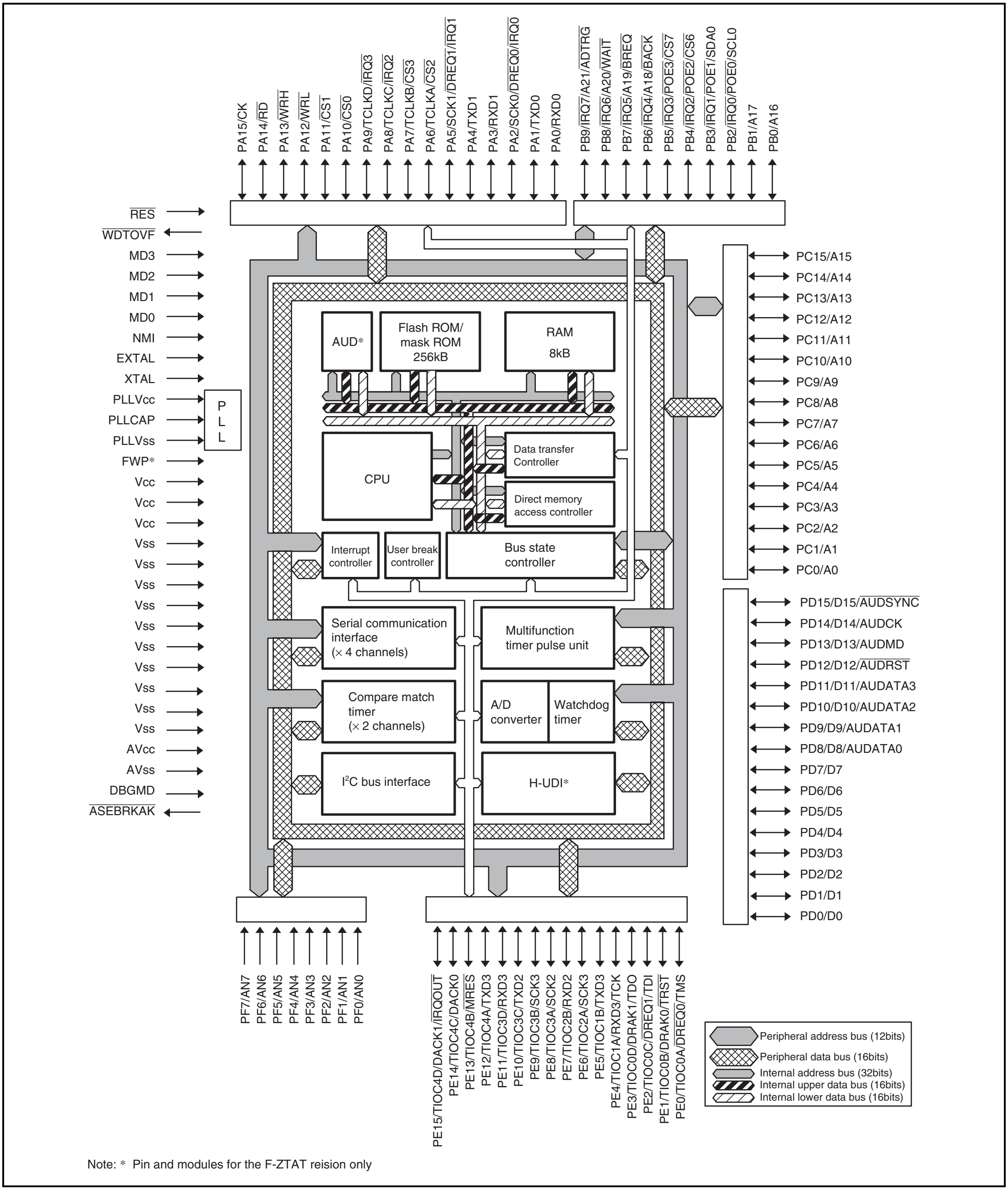

Figure 1.1 Internal Block Diagram of SH7144

Instruction	Instruction Code	Operation	Execution States	T Bit
`MOV.B @(R0,Rm),Rn`	`0000nnnnmmmm1100`	(R0 + Rm) → Sign extension → Rn	1	—
`MOV.W @(R0,Rm),Rn`	`0000nnnnmmmm1101`	(R0 + Rm) → Sign extension → Rn	1	—
`MOV.L @(R0,Rm),Rn`	`0000nnnnmmmm1110`	(R0 + Rm) → Rn	1	—
`MOV.B R0,@(disp,GBR)`	`11000000dddddddd`	R0 → (disp + GBR)	1	—
`MOV.W R0,@(disp,GBR)`	`11000001dddddddd`	R0 → (disp × 2 + GBR)	1	—
`MOV.L R0,@(disp,GBR)`	`11000010dddddddd`	R0 → (disp × 4 + GBR)	1	—
`MOV.B @(disp,GBR),R0`	`11000100dddddddd`	(disp + GBR) → Sign extension → R0	1	—
`MOV.W @(disp,GBR),R0`	`11000101dddddddd`	(disp × 2 + GBR) → Sign extension → R0	1	—
`MOV.L @(disp,GBR),R0`	`11000110dddddddd`	(disp × 4 + GBR) → R0	1	—
`MOVA @(disp,PC),R0`	`11000111dddddddd`	disp × 4 + PC → R0	1	—
`MOVT Rn`	`0000nnnn00101001`	T → Rn	1	—
`SWAP.B Rm,Rn`	`0110nnnnmmmm1000`	Rm → Swap bottom two bytes → Rn	1	—
`SWAP.W Rm,Rn`	`0110nnnnmmmm1001`	Rm → Swap two consecutive words → Rn	1	—
`XTRCT Rm,Rn`	`0010nnnnmmmm1101`	Rm: Middle 32 bits of Rn → Rn	1	—

The clock mode is selected by the input of MD2 and MD3 pins.

Table 3.2 Clock Mode Setting

	Pin Setting		Clock Ratio (when input clock is 1)		
Clock Mode No.	MD3	MD2	System clock (ϕ)	Peripheral clock (Pϕ)	System clock output (CK)
0	0	0	×1	×1	×1
1	0	1	×2	×2	×2
2	1	0	×4	×4*	×4
3	1	1	×4	×2	×4

Note: * The maximum clock input frequency is 10MHz because the pϕ is specified as 40MHz or less.

6.4 Interrupt Sources

There are five types of interrupt sources: NMI, user breaks, H-UDI, IRQ, and on-chip peripheral modules. Each interrupt has a priority expressed as a priority level (0 to 16, with 0 the lowest and 16 the highest). Giving an interrupt a priority level of 0 masks it.

6.4.1 External Interrupts

NMI Interrupts: The NMI interrupt has priority 16 and is always accepted. Input at the NMI pin is detected by edge. Use the NMI edge select bit (NMIE) in the interrupt control register 1 (ICR1) to select either the rising or falling edge. NMI interrupt exception processing sets the interrupt mask level bits (I3 to I0) in the status register (SR) to level 15.

IRQ Interrupts: IRQ interrupts are requested by input from pins $\overline{\text{IRQ0}}$ to $\overline{\text{IRQ7}}$. Set the IRQ sense select bits (IRQ0S to IRQ7S) of the interrupt control register 1 (ICR1) and IRQ edge select bit (IRQ0ES[1:0] to IRQ7ES[1:0]) of the interrupt control register 2 (ICR2) to select low level detection, falling edge detection, or rising edge detection for each pin. The priority level can be set from 0 to 15 for each pin using the interrupt priority registers A and B (IPRA and IPRB).

When IRQ interrupts are set to low level detection, an interrupt request signal is sent to the INTC during the period the $\overline{\text{IRQ}}$ pin is low level. Interrupt request signals are not sent to the INTC when the $\overline{\text{IRQ}}$ pin becomes high level. Interrupt request levels can be confirmed by reading the IRQ flags (IRQ0F to IRQ7F) of the IRQ status register (ISR).

When IRQ interrupts are set to falling edge detection, interrupt request signals are sent to the INTC upon detecting a change on the $\overline{\text{IRQ}}$ pin from high to low level. The results of detection for IRQ interrupt request are maintained until the interrupt request is accepted. It is possible to confirm that IRQ interrupt requests have been detected by reading the IRQ flags (IRQ0F to IRQ7F) of the IRQ status register (ISR), and by writing a 0 after reading a 1, IRQ interrupt request detection results can be cleared

In IRQ interrupt exception processing, the interrupt mask bits (I3 to I0) of the status register (SR) are set to the priority level value of the accepted IRQ interrupt. Figure 6.2 shows the block diagram of this IRQ7 to IRQ0 interrupts.

11.3.12 Timer Gate Control Register (TGCR)

TGCR is an 8-bit readable/writable register that controls the waveform output necessary for brushless DC motor control in reset-synchronized PWM mode/complementary PWM mode. These register settings are ineffective for anything other than complementary PWM mode/reset-synchronized PWM mode.

Bit	Bit Name	Initial value	R/W	Description
7	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
6	BDC	0	R/W	Brushless DC Motor This bit selects whether to make the functions of this register (TGCR) effective or ineffective. 0: Ordinary output 1: Functions of this register are made effective
5	N	0	R/W	Reverse Phase Output (N) Control This bit selects whether the level output or the reset-synchronized PWM/complementary PWM output while the reverse pins (TIOC3D, TIOC4C, and TIOC4D) are output. 0: Level output 1: Reset synchronized PWM/complementary PWM output
4	P	0	R/W	Positive Phase Output (P) Control This bit selects whether the level output or the reset-synchronized PWM/complementary PWM output while the positive pin (TIOC3B, TIOC4A, and TIOC4B) are output. 0: Level output 1: Reset synchronized PWM/complementary PWM output

Operation when Error Occurs during Reset-Synchronous PWM Mode Operation, and Operation is Restarted in Normal Mode: Figure 11.110 shows an explanatory diagram of the case where an error occurs in reset-synchronous PWM mode and operation is restarted in normal mode after re-setting.

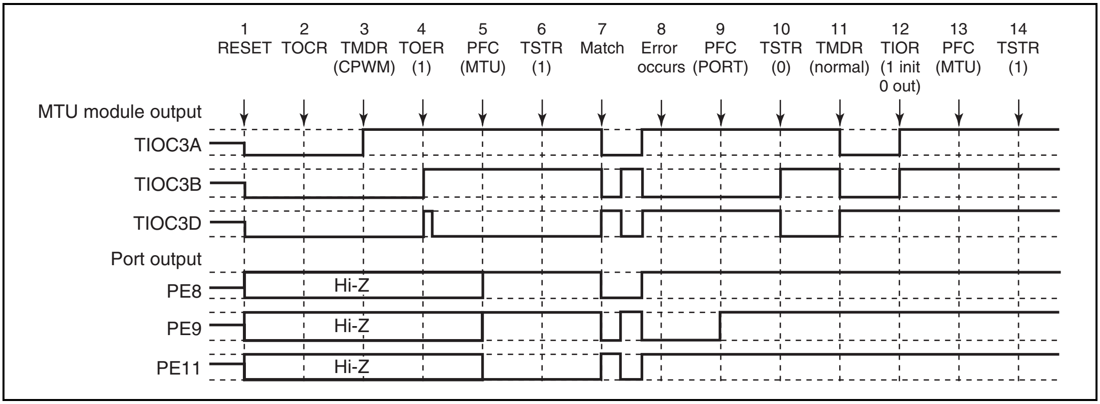

Figure 11.110 Error Occurrence in Reset-Synchronous PWM Mode, Recovery in Normal Mode

1. After a reset, MTU output is low and ports are in the high-impedance state.
2. Select the reset-synchronous PWM output level and cyclic output enabling/disabling with TOCR.
3. Set reset-synchronous PWM.
4. Enable channel 3 and 4 output with TOER.
5. Set MTU output with the PFC.
6. The count operation is started by TSTR.
7. The reset-synchronous PWM waveform is output on compare-match occurrence.
8. An error occurs.
9. Set port output with the PFC and output the inverse of the active level.
10. The count operation is stopped by TSTR. (MTU output becomes the reset-synchronous PWM output initial value.)
11. Set normal mode. (MTU positive phase output is low, and negative phase output is high.)
12. Initialize the pins with TIOR.
13. Set MTU output with the PFC.
14. Operation is restarted by TSTR.

Bit	Bit Name	Initial Value	R/W	Description
5	TE	0	R/W	Transmit Enable When this bit is set to 1, transmission is enabled. In this state, serial transmission is started when transmit data is written to TDR and the TDRE flag in SSR is cleared to 0. SMR setting must be made to decide the transfer format before setting the TE bit to 1. When this bit is cleared to 0, transmit operation is disabled, and the TDRE flag in SSR is fixed to 1.
4	RE	0	R/W	Receive Enable When this bit is set to 1, reception is enabled. Serial reception is started in this state when a start bit is detected in asynchronous mode or synchronous clock input is detected in clocked synchronous mode. SMR setting must be made to decide the receive format before setting the RE bit to 1. Clearing the RE bit to 0 disables reception and does not affect the RDRF, FER, PER, and ORER flags, which retain their states.
3	MPIE	0	R/W	Multiprocessor Interrupt Enable (enabled only when the MP bit in SMR is 1 in asynchronous mode) When this bit is set to 1, receive data in which the multiprocessor bit is 0 is skipped, and setting of the RDRF, FER, and ORER status flags in SSR is prohibited. On receiving data in which the multiprocessor bit is 1, this bit is automatically cleared and normal reception is resumed. For details, refer to section 13.5, Multiprocessor Communication Function. When receive data including MPB = 0 is received, receive data transfer from RSR to RDR, receive error detection, and setting of the RDRF, FER, and ORER flags in SSR, are not performed. When receive data including MPB = 1 is received, the MPB bit in SSR is set to 1, the MPIE bit is cleared to 0 automatically, and generation of RXI and ERI interrupts (when the TIE and RIE bits in SCR are set to 1) and FER and ORER flag setting are enabled.

13.3.8 Serial Direction Control Register (SDCR)

SDCR selects LSB-first or MSB-first transfer and sets the smart card interface. With an 8-bit data length, LSB-first/MSB-first selection is available regardless of the communication mode. With a 7-bit data length, LSB-first transfer must be selected. The description in this section assumes LSB-first transfer.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 1	R	Reserved The write value should always be 1. Operation cannot be guaranteed if 0 is written.
3	DIR	0	R/W	Data Transfer Direction Selects the serial/parallel conversion direction. 0: Transfer in LSB-first 1: Transfer in MSB-first The bit setting is valid only when the transfer data format is 8 bits. For 7-bit data, LSB-first is fixed.
2	SINV	0	R/W	Smart Card Data Invert Specifies inversion of the data logic level. The SINV bit does not affect the logic level of the parity bit. To invert the parity bit, invert the $O/\overline{E}$ bit in SMR. This bit is valid only in smart card interface mode. In normal asynchronous mode or clocked synchronous mode, clear this bit to 0. 0: TDR contents are transmitted as they are. Receive data is stored as it is in RDR 1: TDR contents are inverted before being transmitted. Receive data is stored in inverted form in RDR
1	—	1	R	Reserved This bit is always read as 1 and cannot be modified.
0	SMIF	0	R/W	Smart Card Interface Mode Select This bit is set to 1 to make the SCI operate in smart card interface mode. 0: Normal asynchronous mode or clocked synchronous mode 1: Smart card interface mode

Figure 14.1 is a block diagram of the I²C bus interface. Figure 14.2 shows an example of the connection of I²C bus interfaces. Since the I/O pins are driven only by the NMOS transistor, they operate in the same way as pins driven by an open-drain NMOS transistor. The voltage that can be applied to the I/O pins depends on the supply voltage of the LSI.

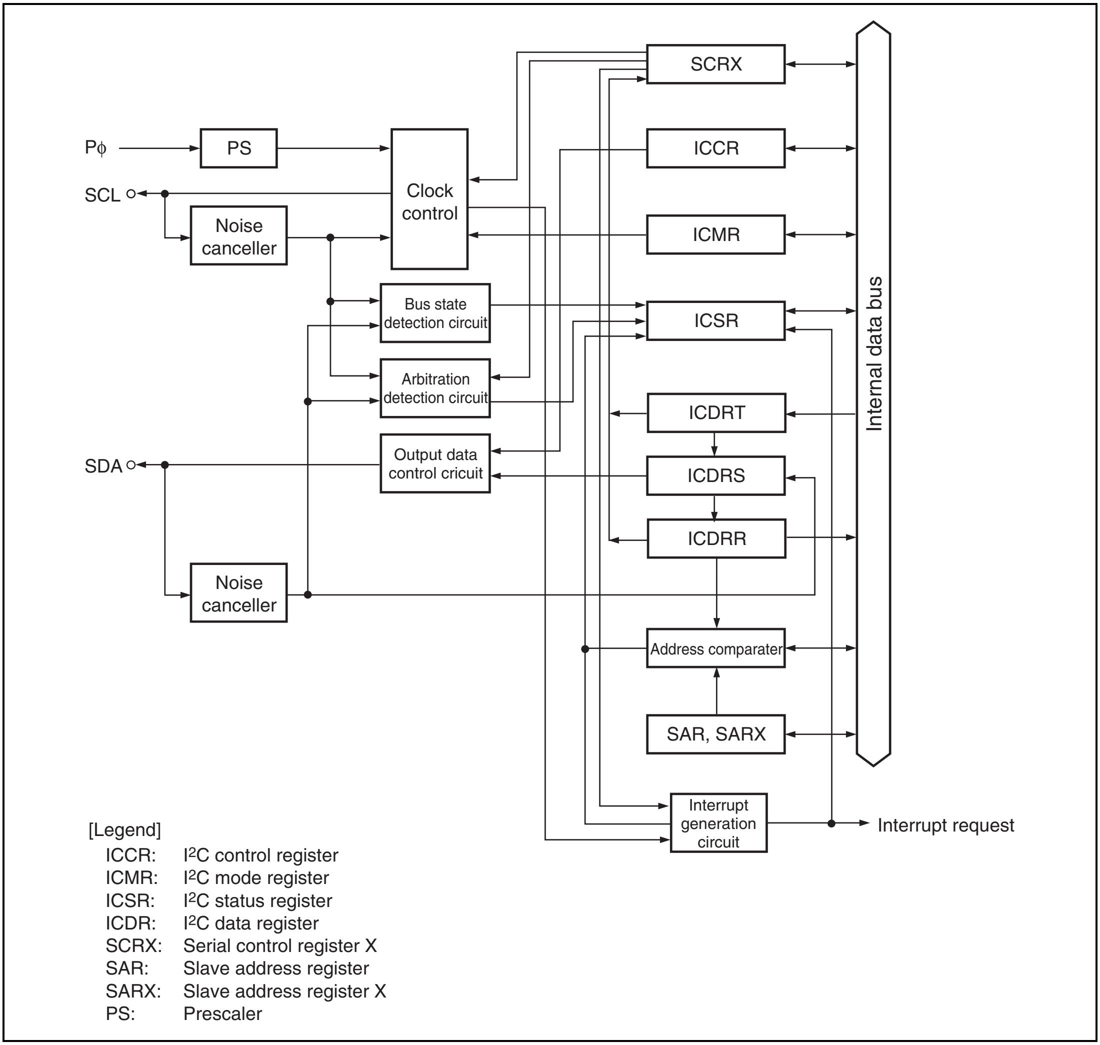

Figure 14.1 A Block Diagram of the I²C Bus Interface

14.3.7 Serial Control Register X (SCRX)

SCRX enables or disables I²C bus interface interrupts and confirms the state of reception and transmission.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	IICX	0	R/W	I²C Transfer Rate Select Along with bits CKS2 to CKS0 in the I²C bus mode register (ICMR), this bit selects the transfer rate in the master mode. For details on setting the transfer rate, see table 14.3.
4	IICE	0	R/W	I²C master Enable This bit controls access by the CPU to the I²C bus interface registers (ICCR, ICSR, ICDR/SARX, and ICMR/SAR) of the I²C bus interface. 0: Disables CPU access to the registers of the I²C bus interface. 1: Enables CPU access to the registers of the I²C bus interface.
3	HNDS	0	R/W	Hand-Shake Receive Select This bit enables/disables continuous reception in receive mode. When the HNDS bit is cleared to 0, receive operation is performed continuously after data has been received successfully while ICDRF flag is 0. When the HNDS bit is set to 1, SCL is fixed to the low level thus disabling the next data to be transferred. The bus line is released and next frame receive operation is enabled by reading the receive data in ICDR.
2	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

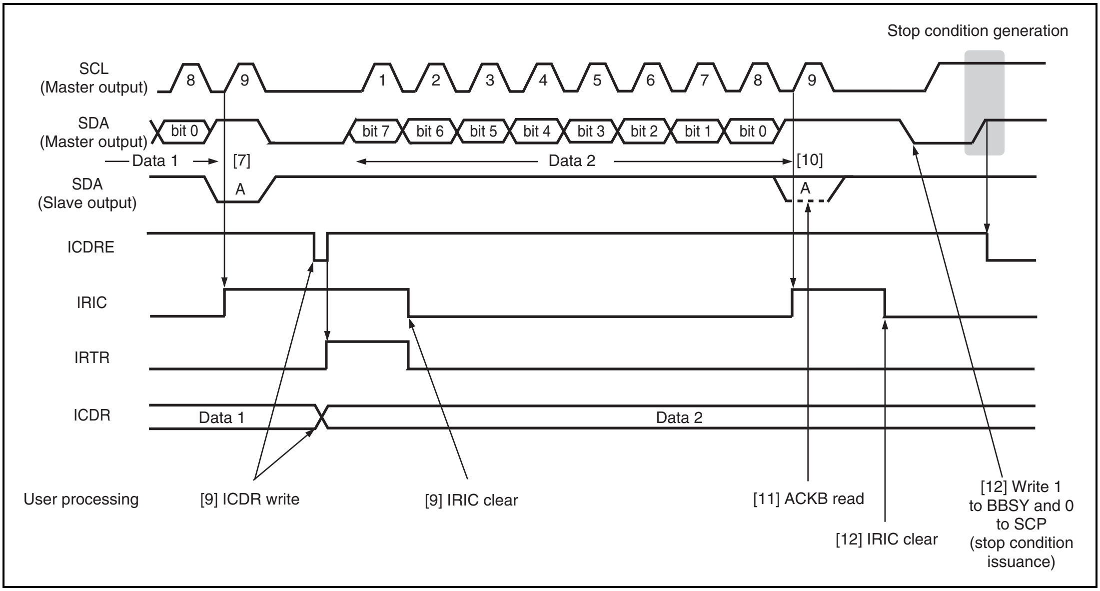

Figure 14.9 An Example of the Stop Condition Issuance Timing in Master Transmit Mode (MLS = WAIT = 0)

14. Confirm that the ICDRF flag is set to 1, and then read ICDR.
15. Clear the IRIC flag to 0.

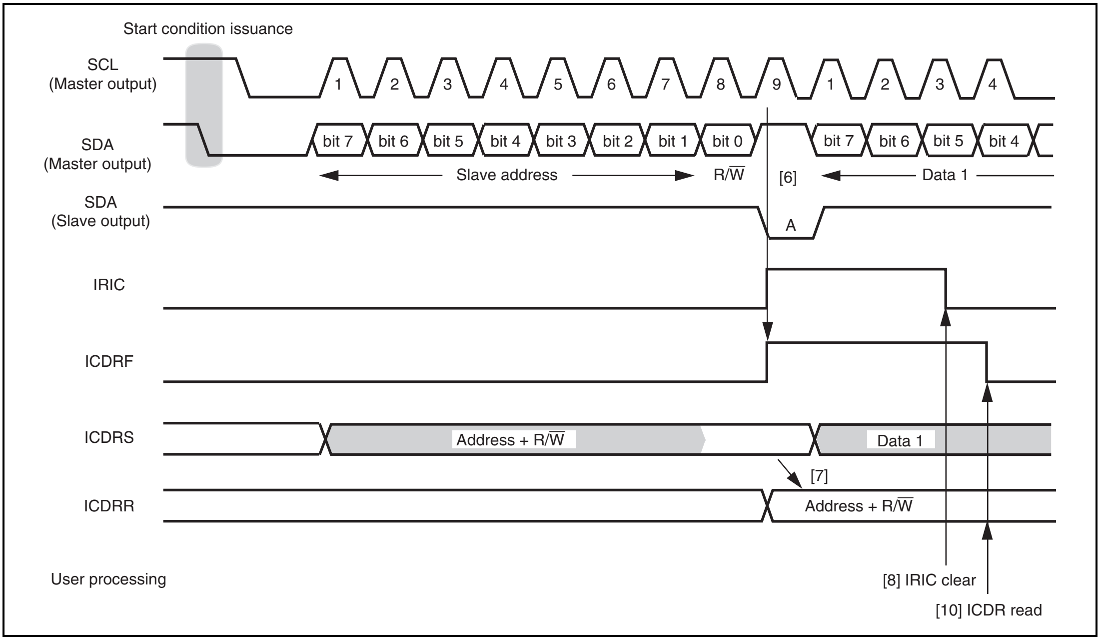

Figure 14.21 An Example of the Timing of Operations in Slave Receive Mode 1 (MLS = ACKB = 0, HNDS = 0)

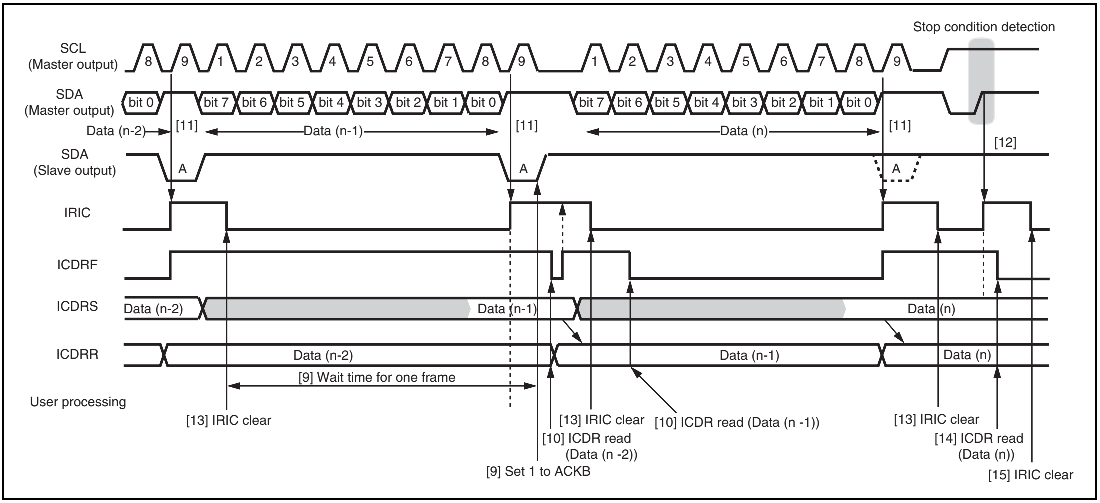

Figure 14.22 An Example of the Timing of Operations in Slave Receive Mode 2 (MLS = ACKB = 0, HNDS = 0)

15.3.3 A/D Control Register_0, 1 (ADCR_0, ADCR_1)

ADCR for each module controls A/D conversion started by an external trigger signal and selects the operating clock.

Bit	Bit Name	Initial Value	R/W	Description
7	TRGE	0	R/W	Trigger Enable Enables or disables triggering of A/D conversion by $\overline{\text{ADTRG}}$ or an MTU trigger. 0: A/D conversion triggering is disabled 1: A/D conversion triggering is enabled
6	CKS1	0	R/W	Clock Select 1, 0
5	CKS0	0	R/W	Select the A/D conversion time. 00: Pϕ/32 01: Pϕ/16 10: Pϕ/8 11: Pϕ/4 When changing the operating mode, first clear the ADST bit in the A/D control registers (ADCR) to 0. CKS[1,0] = b'11 can be set while Pϕ ≤ 25 MHz.
4	ADST	0	R/W	A/D Start Starts or stops A/D conversion. When this bit is set to 1, A/D conversion is started. When this bit is cleared to 0, A/D conversion is stopped and the A/D converter enters the idle state. In single or single-cycle scan mode, this bit is automatically cleared to 0 when A/D conversion ends on the selected single channel. In continuous scan mode, A/D conversion is continuously performed for the selected channels in sequence until this bit is cleared by a software, reset, or in software standby mode, or module standby mode.
3	ADCS	0	R/W	A/D Continuous Scan Selects either single-cycle scan or continuous scan in scan mode. This bit is valid only when scan mode is selected. 0: Single-cycle scan 1: Continuous scan When changing the operating mode, first clear the ADST bit in the A/D control registers (ADCR) to 0.

Register	Bit	Bit Name	Initial Value	R/W	Description
PACRL1	6	PA11MD	0*3	R/W	PA11 Mode Selects the function of the PA11/$\overline{\text{CS1}}$ pin. 0: PA11 I/O (port) 1: $\overline{\text{CS1}}$ output (BSC)
PACRL1	4	PA10MD	0*3	R/W	PA10 Mode Selects the function of the PA10/$\overline{\text{CS0}}$ pin. 0: PA10 I/O (port) 1: $\overline{\text{CS0}}$ output (BSC)
PACRL1	3	PA9MD1	0	R/W	PA9 Mode
PACRL1	2	PA9MD0	0	R/W	Select the function of the PA9/TCLKD/$\overline{\text{IRQ3}}$ pin. 00: PA9 I/O (port) 01: TCLKD input (MTU) 10: $\overline{\text{IRQ3}}$ input (INTC) 11: Setting prohibited
PACRL1	1	PA8MD1	0	R/W	PA8 Mode
PACRL1	0	PA8MD0	0	R/W	Select the function of the PA8/TCLKC/$\overline{\text{IRQ2}}$ pin. 00: PA8 I/O (port) 01: TCLKC input (MTU) 10: $\overline{\text{IRQ2}}$ input (INTC) 11: Setting prohibited
PACRL2	15	PA7MD1	0	R/W	PA7 Mode
PACRL2	14	PA7MD0	0	R/W	Select the function of the PA7/TCLKB/ $\overline{\text{CS3}}$ pin. 00: PA7 I/O (port) 01: TCLKB input (MTU) 10: $\overline{\text{CS3}}$ output (BSC) 11: Setting prohibited
PACRL2	13	PA6MD1	0	R/W	PA6 Mode
PACRL2	12	PA6MD0	0	R/W	Select the function of the PA6/TCLKA/ $\overline{\text{CS2}}$ pin. 00: PA6 I/O (port) 01: TCLKA input (MTU) 10: $\overline{\text{CS2}}$ output (BSC) 11: Setting prohibited

19.4 Input/Output Pins

The flash memory is controlled by means of the pins shown in table 19.2.

Table 19.2 Pin Configuration

Pin Name	I/O	Function
$\overline{\text{RES}}$	Input	Reset
FWP*[1]	Input	Flash programming/erasing protection by hardware
MD1	Input	Sets this LSI's operating mode
MD0	Input	Sets this LSI's operating mode
TxD1 (PA4)*[2]	Output	Serial transmit data output
RxD1 (PA3)*[2]	Input	Serial receive data input

Notes: 1. Protection cannot be made to flash memory programming/erasing regardless of the setting of the FWP pin when using E10A (when DBGMD is high)

2. In boot mode, SCI pins are fixed, and PA3 and PA4 pins are used as SCI pins.

23.4.3 Operation

Operation starts in RAM monitor mode when $\overline{\text{AUDRST}}$ is asserted, AUDMD is driven high, then $\overline{\text{AUDRST}}$ is negated.

Figure 23.5 shows an example of a read operation, and figure 23.6 an example of a write operation.

When $\overline{\text{AUDSYNC}}$ is asserted, input from the AUDATA pins begins. When a command, address, or data (writing only) is input in the format shown in figure 23.4, execution of read/write access to the specified address is started. During internal execution, the AUD returns Not Ready (0000). When execution is completed, the Ready flag (0001) is returned (figures 23.5 and 23.6). Table 23.2 shows the Ready flag format.

In a read, data of the specified size is output when $\overline{\text{AUDSYNC}}$ is negated following detection of this flag (figure 23.5).

If a command other than the above is input in DIR, the AUD treats this as a command error, disables processing, and sets bit 1 in the Ready flag to 1. If a read/write operation initiated by the command specified in DIR causes a bus error, the AUD disables processing and sets bit 2 in the Ready flag to 1 (figure 23.7).

Bus error conditions are shown below.

1. Word access to address 4n+1 or 4n+3
2. Longword access to address 4n+1, 4n+2, or 4n+3
3. Longword access to on-chip I/O 8-bit area
4. Access to external area in single-chip mode

Table 23.2 Ready Flag Format

Bit 3	Bit 2	Bit 1	Bit 0
Fixed at 0	0: Normal status 1: Bus error	0: Normal status 1: Command error	0: Not ready 1: Ready

Register abbreviation	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Module
—	—	—	—	—	—	—	—	—	—
BCR1	—	—	MTURWE	—	—	—	—	—	BSC
	A3LG	A2LG	A1LG	A0LG	A3SZ	A2SZ	A1SZ	A0SZ	
BCR2	IW31	IW30	IW21	IW20	IW11	IW10	IW01	IW00	
	CW3	CW2	CW1	CW0	SW3	SW2	SW1	SW0	
WCR1	W33	W32	W31	W30	W23	W22	W21	W20	
	W13	W12	W11	W10	W03	W02	W01	W00	
WCR2	—	—	—	—	—	—	—	—	
	—	—	—	—	DSW3	DSW2	DSW1	DSW0	
—	—	—	—	—	—	—	—	—	—
RAMER	—	—	—	—	—	—	—	—	FLASH (Only in F-ZTAT version)
	—	—	—	—	RAMS	RAM2	RAM1	RAM0	
—	—	—	—	—	—	—	—	—	—
DMAOR	—	—	—	—	—	—	PR1	PR0	DMAC for all channels
	—	—	—	—	—	AE	NMIF	DME	
SAR_0									DMAC (Channel 0)
DAR_0									
DMATCR_0	—	—	—	—	—	—	—	—	
CHCR_0	—	—	—	—	—	—	—	—	
	—	—	—	—	—	RL	AM	AL	
	DM1	DM0	SM1	SM0	RS3	RS2	RS1	RS0	
	—	DS	TM	TS1	TS0	IE	TE	DE	

SH7144 Group, SH7145 Group
Hardware Manual

Renesas Electronics Corporation
1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan

REJ09B0108-0400