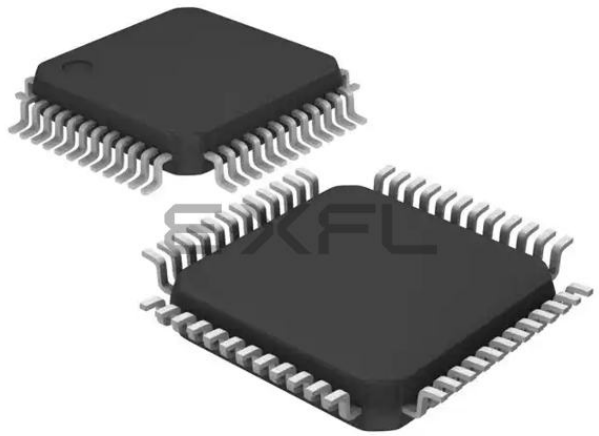

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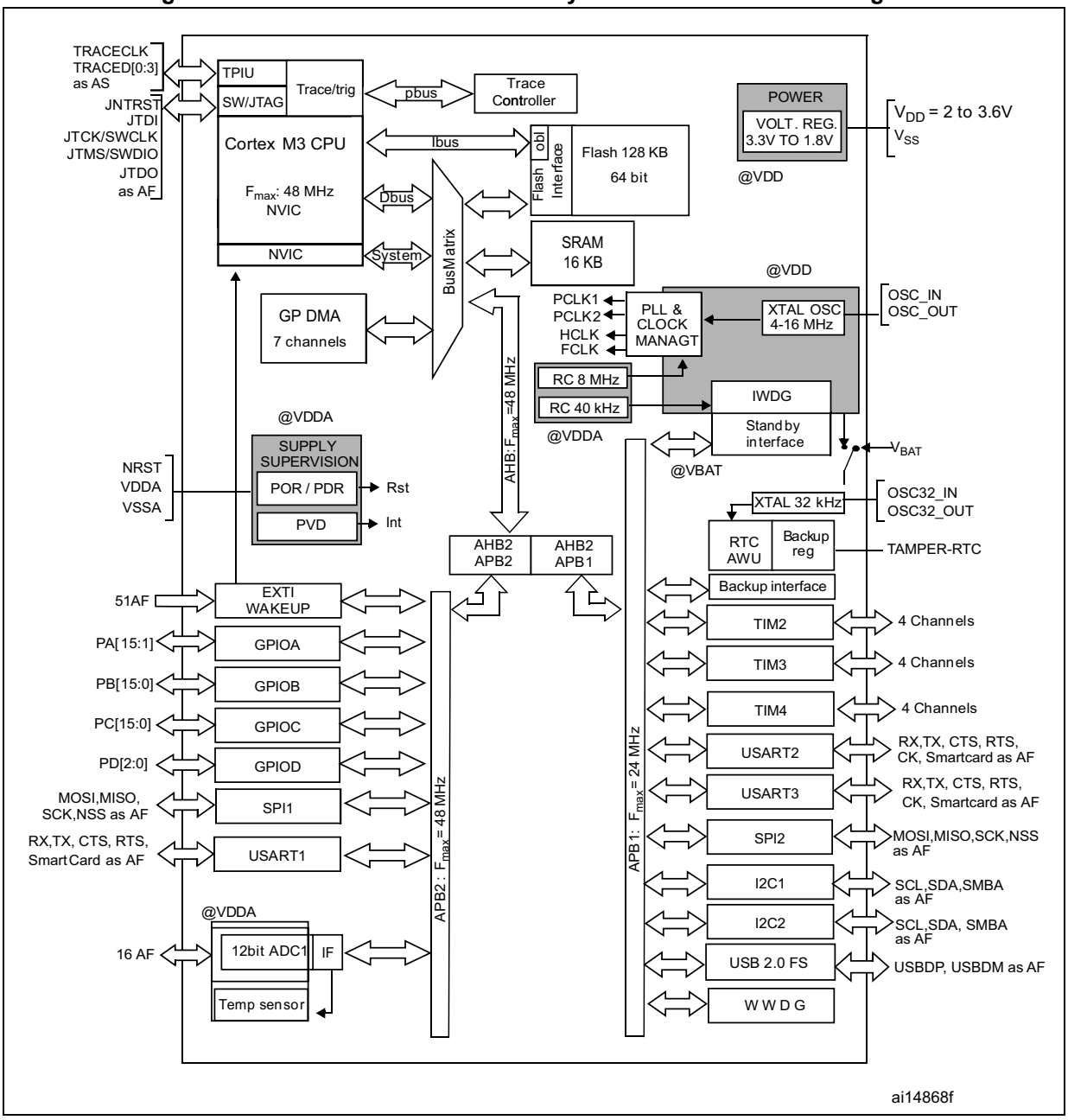
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f102c8t6

Contents

Figure 1. STM32F102T8 medium-density USB access line block diagram



1. AF = alternate function on I/O port pin.
2. T_A = –40 °C to +85 °C (junction temperature up to 105 °C).

CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity, In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

Embedded SRAM

10 or 16 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

Nested vectored interrupt controller (NVIC)

The STM32F102xx medium-density USB access line embeds a nested vectored interrupt controller able to handle up to 36 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detectors lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect external line with pulse width lower than the Internal APB2 clock period. Up to 51 GPIOs are connected to the 16 external interrupt lines.

Clocks and startup

System clock selection is performed on startup. however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the High Speed APB (APB2) and the low Speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 48 MHz. See *Figure 2* for details on the clock tree.

register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock. it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

General-purpose timers (TIMx)

There are 3 synchronizable general-purpose timers embedded in the STM32F102xx medium-density USB access line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture, output compare, PWM or one-pulse mode output. This gives up to 12 input captures / output compares / PWMs on the LQFP48 and LQFP64 packages.
The general-purpose timers can work together via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode.

Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

I²C bus

Two I²C bus interfaces can operate in multi-master and slave modes. They can support standard and fast modes. They support dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

Table 4. Medium-density STM32F102xx pin definitions

Pins		Pin name	Type[1]	I / O level[2]	Main function[3] (after reset)	Alternate functions[3] [4]	
LQFP48	LQFP64					Default	Remap
1	1	V_{BAT}	S	-	V_{BAT}	-	-
2	2	PC13-TAMPER-RTC[5]	I/O	-	PC13[6]	TAMPER-RTC	-
3	3	PC14-OSC32_IN[5]	I/O	-	PC14[6]	OSC32_IN	-
4	4	PC15-OSC32_OUT[5]	I/O	-	PC15[6]	OSC32_OUT	-
5	5	OSC_IN	I/O	FT	OSC_IN	-	PD0[7]
6	6	OSC_OUT	I/O	FT	OSC_OUT	-	PD1[7]
7	7	NRST	I/O	-	NRST	-	-
-	8	PC0	I/O	-	PC0	ADC_IN10	-
-	9	PC1	I/O	-	PC1	ADC_IN11	-
-	10	PC2	I/O	-	PC2	ADC_IN12	-
-	11	PC3	I/O	-	PC3	ADC_IN13	-
8	12	V_{SSA}	S	-	V_{SSA}	-	-
9	13	V_{DDA}	S	-	V_{DDA}	-	-
10	14	PA0-WKUP	I/O	-	PA0	WKUP/USART2_CTS/ ADC_IN0/ TIM2_CH1_ETR[8]	-
11	15	PA1	I/O	-	PA1	USART2_RTS/ ADC_IN1/TIM2_CH2[8]	-
12	16	PA2	I/O	-	PA2	USART2_TX/ ADC_IN2/TIM2_CH3[8]	-
13	17	PA3	I/O	-	PA3	USART2_RX/ ADC_IN3/TIM2_CH4[8]	-
-	18	V_{SS_4}	S	-	V_{SS_4}	-	-
-	19	V_{DD_4}	S	-	V_{DD_4}	-	-
14	20	PA4	I/O	-	PA4	SPI1_NSS[8]/ADC_IN4 USART2_CK/	-
15	21	PA5	I/O	-	PA5	SPI1_SCK[8]/ADC_IN5	-
16	22	PA6	I/O	-	PA6	SPI1_MISO[8]/ADC_IN6/ TIM3_CH1[8]	-
17	23	PA7	I/O	-	PA7	SPI1_MOSI[8]/ADC_IN7/ TIM3_CH2[8]	-
-	24	PC4	I/O	-	PC4	ADC_IN14	-
-	25	PC5	I/O	-	PC5	ADC_IN15	-
18	26	PB0	I/O	-	PB0	ADC_IN8/TIM3_CH3[8]	-
19	27	PB1	I/O	-	PB1	ADC_IN9/TIM3_CH4[8]	-

Table 4. Medium-density STM32F102xx pin definitions (continued)

Pins		Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3) (4)	
LQFP48	LQFP64					Default	Remap
20	28	PB2	I/O	FT	PB2/BOOT1	-	-
21	29	PB10	I/O	FT	PB10	I2C2_SCL/ USART3_TX(8)	TIM2_CH3
22	30	PB11	I/O	FT	PB11	I2C2_SDA/ USART3_RX(8)	TIM2_CH4
23	31	V_{SS_1}	S	-	V_{SS_1}	-	-
24	32	V_{DD_1}	S	-	V_{DD_1}	-	-
25	33	PB12	I/O	FT	PB12	SPI2_NSS / I2C2_SMBA/ USART3_CK(8)	-
26	34	PB13	I/O	FT	PB13	SPI2_SCK(8)/ USART3_CTS	-
27	35	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_RTS	-
28	36	PB15	I/O	FT	PB15	SPI2_MOSI	-
-	37	PC6	I/O	FT	PC6	-	TIM3_CH1
-	38	PC7	I/O	FT	PC7	-	TIM3_CH2
-	39	PC8	I/O	FT	PC8	-	TIM3_CH3
-	40	PC9	I/O	FT	PC9	-	TIM3_CH4
29	41	PA8	I/O	FT	PA8	USART1_CK/MCO	-
30	42	PA9	I/O	FT	PA9	USART1_TX(8)	-
31	43	PA10	I/O	FT	PA10	USART1_RX(8)	-
32	44	PA11	I/O	FT	PA11	USART1_CTS/USB_DM	-
33	45	PA12	I/O	FT	PA12	USART1_RTS/USB_DP	-
34	46	PA13	I/O	FT	JTMS-SWDIO	-	PA13
35	47	V_{SS_2}	S	-	V_{SS_2}	-	-
36	48	V_{DD_2}	S	-	V_{DD_2}	-	-
37	49	PA14	I/O	FT	JTCK/ SWCLK	-	PA14
38	50	PA15	I/O	FT	JTDI	-	TIM2_CH1_ETR / PA15 /SPI1_NSS
-	51	PC10	I/O	FT	PC10	-	USART3_TX
-	52	PC11	I/O	FT	PC11	-	USART3_RX
-	53	PC12	I/O	FT	PC12	-	USART3_CK
-	54	PD2	I/O	FT	PD2	TIM3_ETR	-

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

2. Refer to application note AN2868 “STM32F10xxx internal RC oscillator (HSI) calibration” available from the ST website www.st.com.
3. Guaranteed by design, not tested in production.
4. Based on characterization, not tested in production.
5. The actual frequency of HSI oscillator may be impacted by a reflow, but does not drift out of the specified range.

Low-speed internal (LSI) RC oscillator

Table 24. LSI oscillator characteristics (1)

Symbol	Parameter	Min(2)	Typ	Max	Unit
f_{LSI}	Frequency	30	40	60	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.65	1.2	µA

1. V_{DD} = 3 V, T_A = –40 to 85 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in *Table 25* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 25. Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	1.8	µs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	3.6	µs
	Wakeup from Stop mode (regulator in low-power mode)	5.4	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	50	µs

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

5.3.8 PLL characteristics

The parameters given in *Table 26* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports), This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 30. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/48 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C.	0.1 MHz to 30 MHz	7	dBµV
			30 MHz to 130 MHz	8	
			130 MHz to 1GHz	13	
			SAE EMI Level	3.5	-

5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 31. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	II	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78 IC latch-up standard.

Table 32. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

5.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 33*.

Table 33. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

5.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 34* are derived from tests performed under the conditions summarized in *Table 8*. All I/Os are CMOS and TTL compliant.

Table 34. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	Standard IO input low level voltage	-	-	$0.28*(V_{DD}-2\ V)+0.8\ V$(1)	V
		IO FT(3) input low level voltage	-	-	$0.32*(V_{DD}-2V)+0.75\ V$(1)	
		All I/Os except BOOT0	-	-	$0.35V_{DD}$(2)	
V_{IH}	High level input voltage	Standard IO input high level voltage	$0.41*(V_{DD}-2\ V)+1.3\ V$(1)	-	-	
		IO FT(3) input high level voltage	$0.42*(V_{DD}-2\ V)+1\ V$(1)	-	-	
		All I/Os except BOOT0	$0.65V_{DD}$(2)	-	-	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis(4)	-	200	-	-	mV
	IO FT Schmitt trigger voltage hysteresis(4)	-	5% V_{DD}(5)	-	-	
I_{lkg}	Input leakage current (6)	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/Os	-	-	±1	µA
		V_{IN} = 5 V I/O FT	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(7)	$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(7)	$V_{IN} = V_{DD}$	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation.
2. Tested in production.
3. FT = Five-volt tolerant, In order to sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
4. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
5. With a minimum of 100 mV.
6. Leakage could be higher than max, if negative current is injected on adjacent pins.
7. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required), Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 20* and *Figure 21* for standard I/Os, and in *Figure 22* and *Figure 23* for 5 V tolerant I/Os.

Figure 20. Standard I/O input characteristics - CMOS port

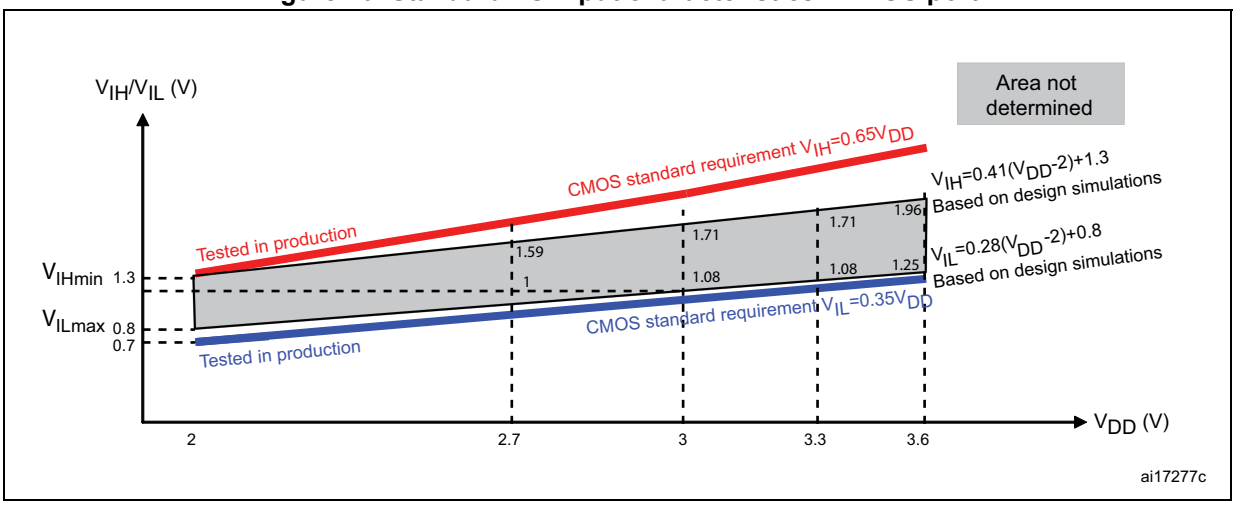
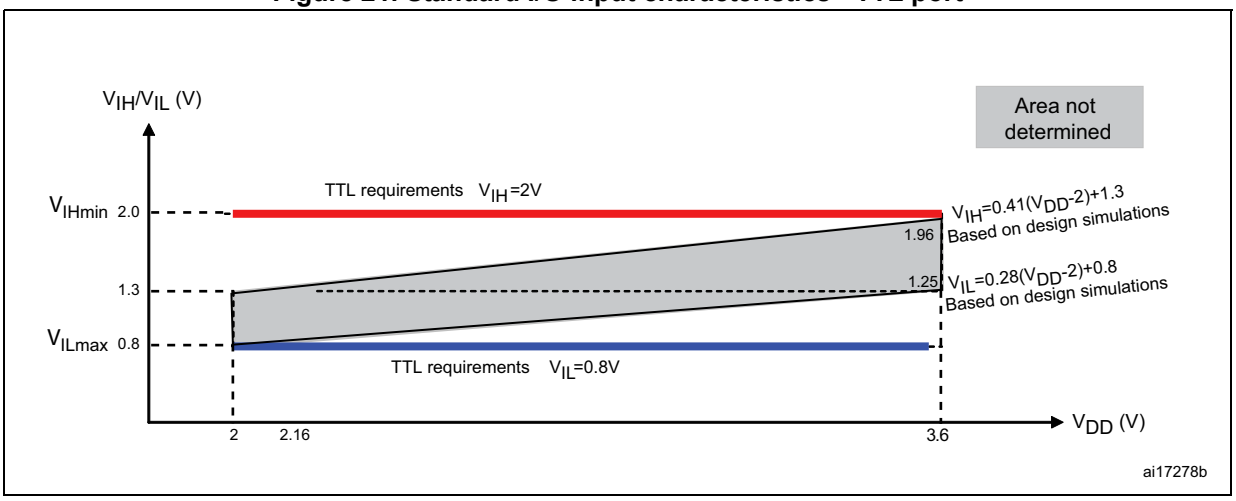


Figure 21. Standard I/O input characteristics - TTL port



Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 24* and *Table 36*, respectively.

Unless otherwise specified, the parameters given in *Table 36* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 36. I/O AC characteristics(1)

MODEx [1:0] bit value(1)	Symbol	Parameter	Conditions	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		25(3)	
11	$F_{max(IO)out}$	Maximum Frequency(2)	C_L= 30 pF, V_{DD} = 2.7 V to 3.6 V	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 24*.
3. Guaranteed by design, not tested in production.

5.3.15 TIM timer characteristics

The parameters given in *Table 38* are guaranteed by design.

Refer to *Section 5.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 38. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	20.84	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 48 MHz	0	24	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	0.0208	1365	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	89.48	s

1. TIMx is used as a general term to refer to the TIM2, TIM3 and TIM4 timers.

5.3.16 Communications interfaces

I²C interface characteristics

The STM32F102xx medium-density USB access line I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

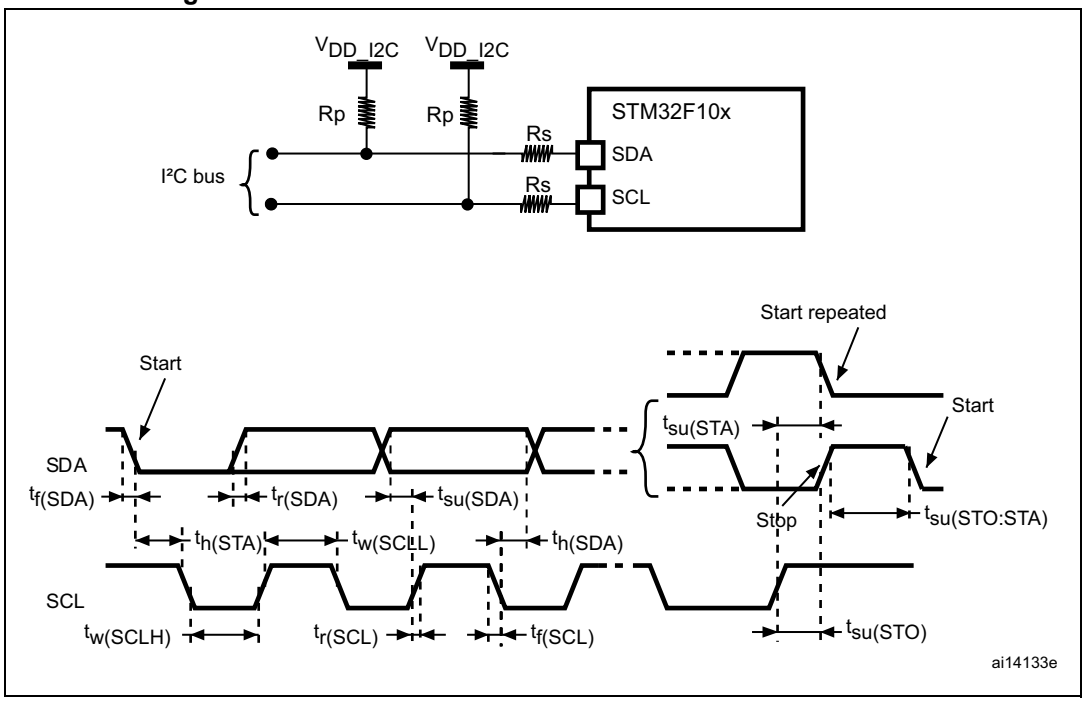
The I²C characteristics are described in *Table 39*. Refer also to *Section 5.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 39. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)(2)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	-	3450(3)	-	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
t_{SP}	Pulse width of spikes that are suppressed by the analog filter	0	50(4)	0	50(4)	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Values guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I^2C frequencies. It must be at least 4 MHz to achieve fast mode I^2C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I2C fast mode clock.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of the SCL signal.
4. The analog filter minimum filtered spikes is above $t_{SP(max)}$ to ensure that spikes width up to $t_{SP(max)}$ are filtered.

Figure 26. I²C bus AC waveforms and measurement circuit(1)



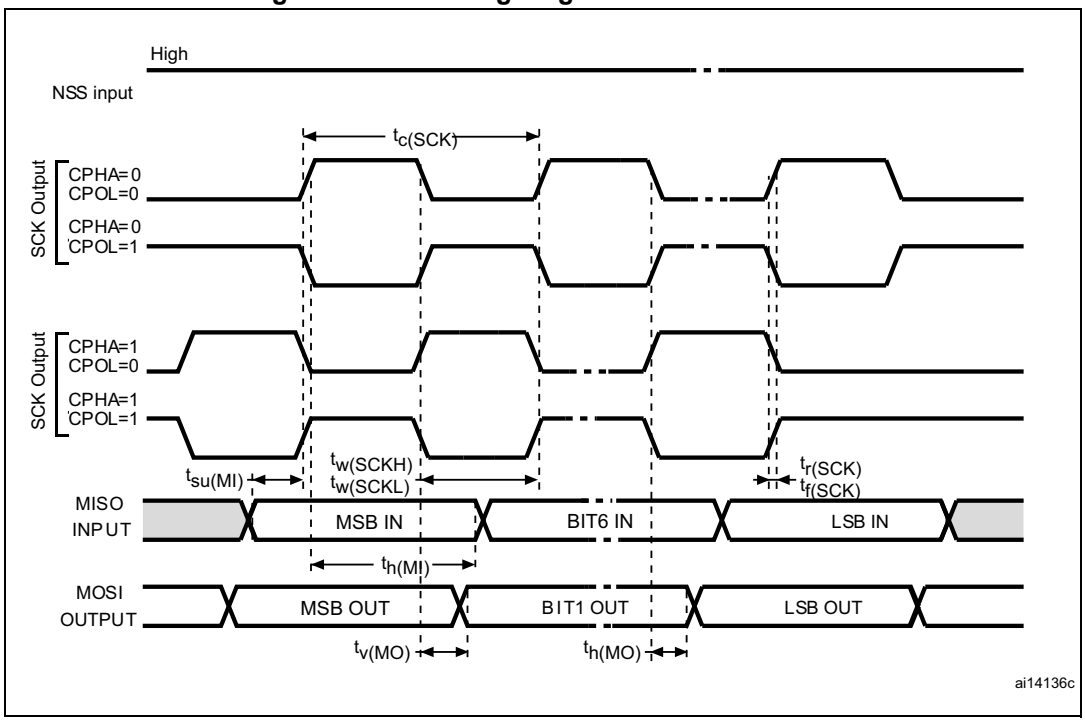
1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 40. SCL frequency (f_{PCLK1}= 36 MHz, V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I²C speed.
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

Figure 29. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

USB characteristics

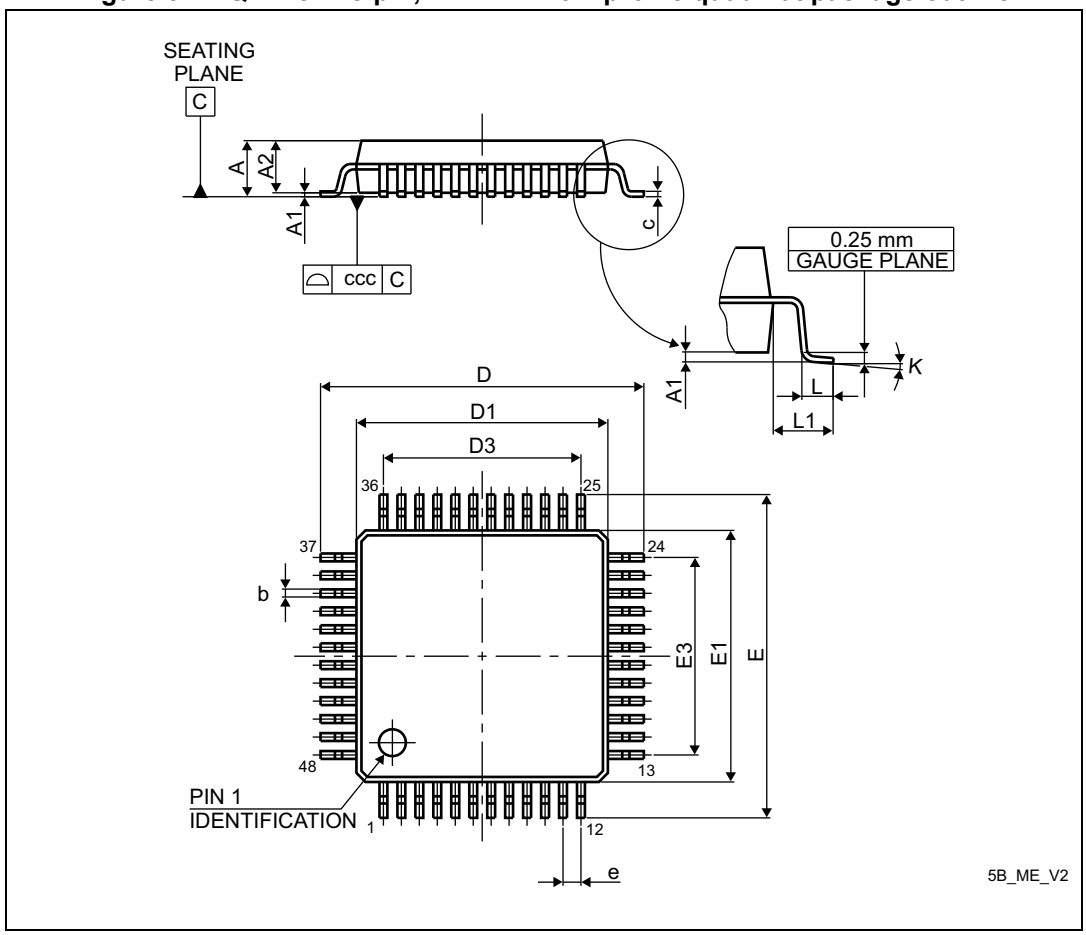
The USB interface is USB-IF certified (Full Speed).

Table 42. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$	USB transceiver startup time	1	µs

6.2 LQFP48 package information

Figure 37. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 54. Document revision history (continued)

Date	Revision	Changes
02-Aug-2013	5	Removed sentence in “Unless otherwise specified the parameters ...” in *I2C interface characteristics* section. Added V_{IN} in *Table 8: General operating conditions*. Added note *5* in *Table 23: HSI oscillator characteristics* Modified charge device model in *Table 33: ESD absolute maximum ratings* Updated ‘V_{IL}’ and ‘V_{IH}’ in *Table 34: I/O static characteristics* Added notes to *Figure 20: Standard I/O input characteristics - CMOS port*, *Figure 21: Standard I/O input characteristics - TTL port*, *Figure 22: 5 V tolerant I/O input characteristics - CMOS port* and *Figure 23: 5 V tolerant I/O input characteristics - TTL port* Updated *Figure 24: I/O AC characteristics definition* Updated note *2.* and *3.* in *Table 39: I^2C characteristics* Updated *Figure 26: I2C bus AC waveforms and measurement circuit(1)* Updated title of *Table 40: SCL frequency (f_{PCLK1}= 36 MHz, V_{DD_I2C} = 3.3 V)* Updated *Table 47: ADC characteristics* Updated *Section 6.1: Package mechanical data*
03-Jun-2015	6	Updated *Table 18: Peripheral current consumption* and *Table 39: I^2C characteristics* Updated *Section 6: Package characteristics* Updated *Section 6.1: LQFP64 package information* with addition of *Device marking for LQFP64* and *Figure 36*. Updated *Section 6.2: LQFP48 package information* with addition of *Device marking for LQFP48* and *Figure 39*. Updated Disclaimer.