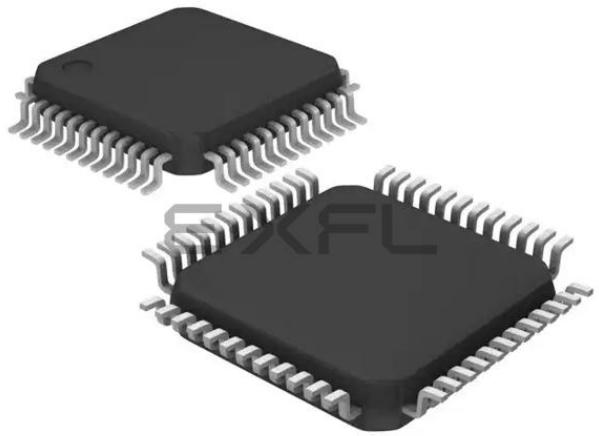

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f102cbt6

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of STM32F102x8 and STM32F102xB medium-density USB access line microcontrollers. For more details on the whole STMicroelectronics STM32F102xx family. please refer to *Section 2.2: Full compatibility throughout the family*.

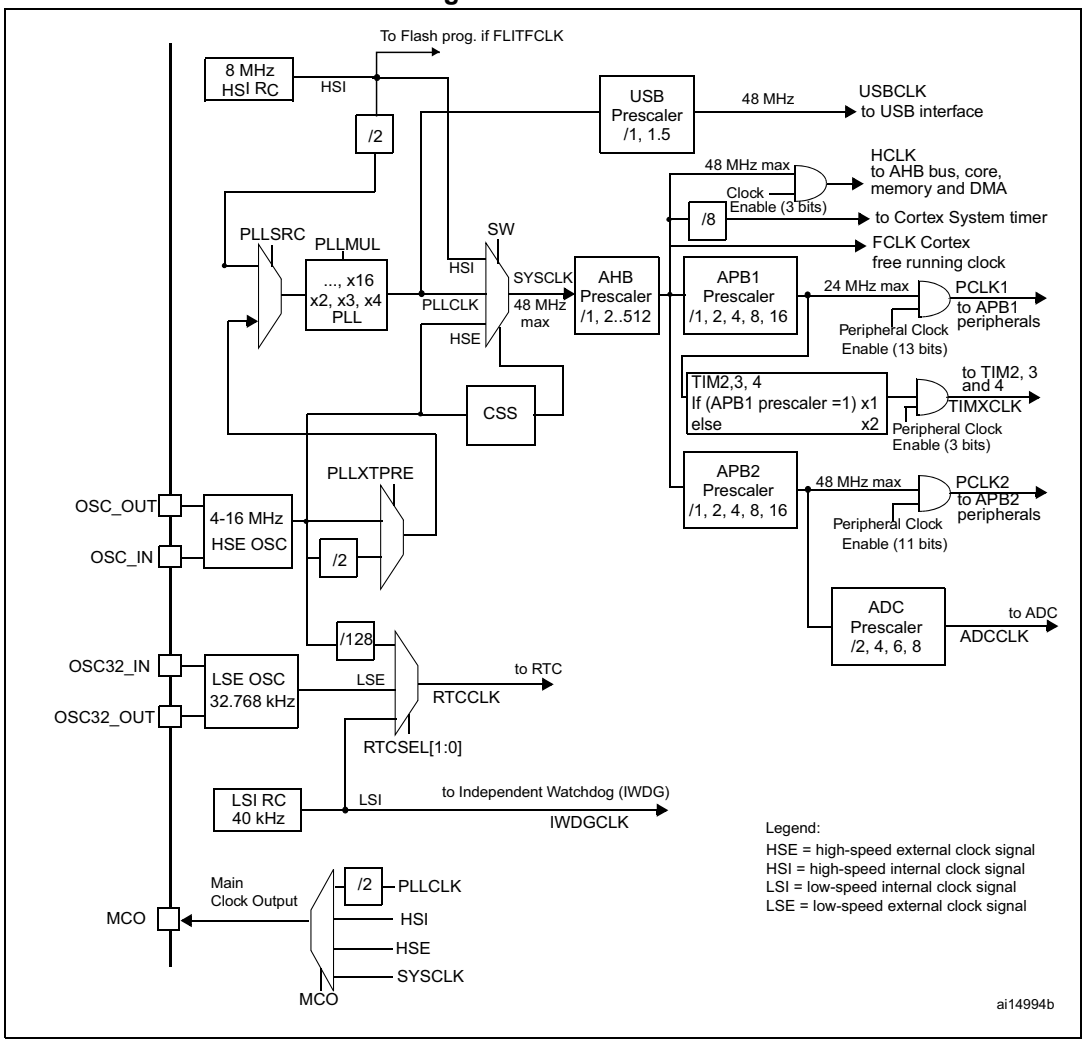
The medium-density STM32F102xx datasheet should be read in conjunction with the low-, medium- and high-density STM32F10xxx reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual.*

The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the ARM® website.

Figure 2. Clock tree



1. For the USB function to be available, both HSE and PLL must be enabled, with the USB clock output (USBCLK) at 48 MHz.
2. To have an ADC conversion time of 1.2 µs, APB2 must be at 12 MHz, 24 MHz or 48 MHz.
3. The Flash memory programming interface clock (FLITFCLK) is always the HSI clock.

Low-power modes

The STM32F102xx medium-density USB access line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop** mode

  The Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.
  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and registers content are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general purpose timers TIMx and ADC.

RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3 Pinout and pin description

Figure 3. STM32F102xx medium-density USB access line LQFP48 pinout

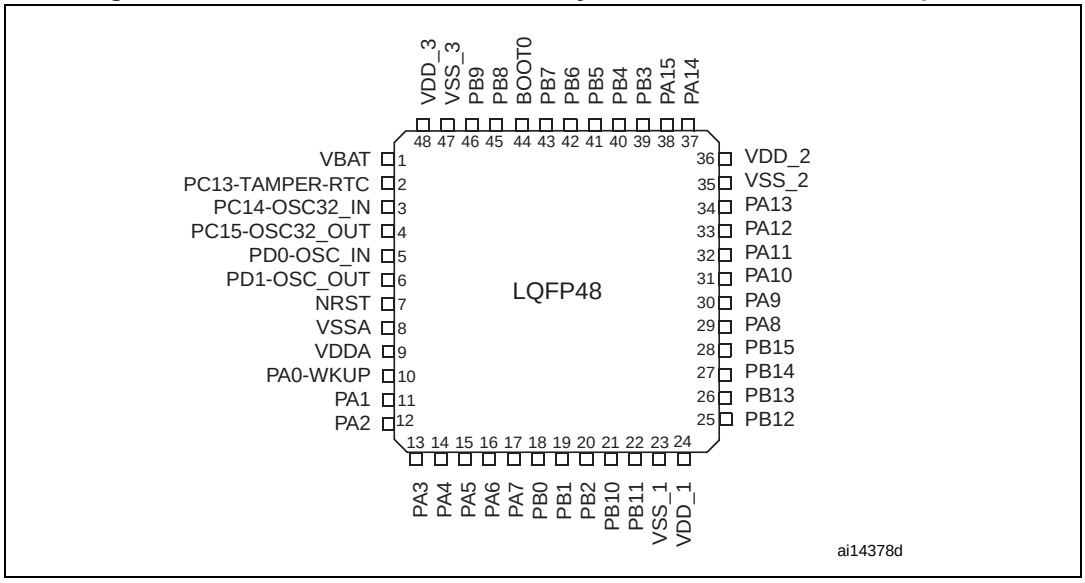
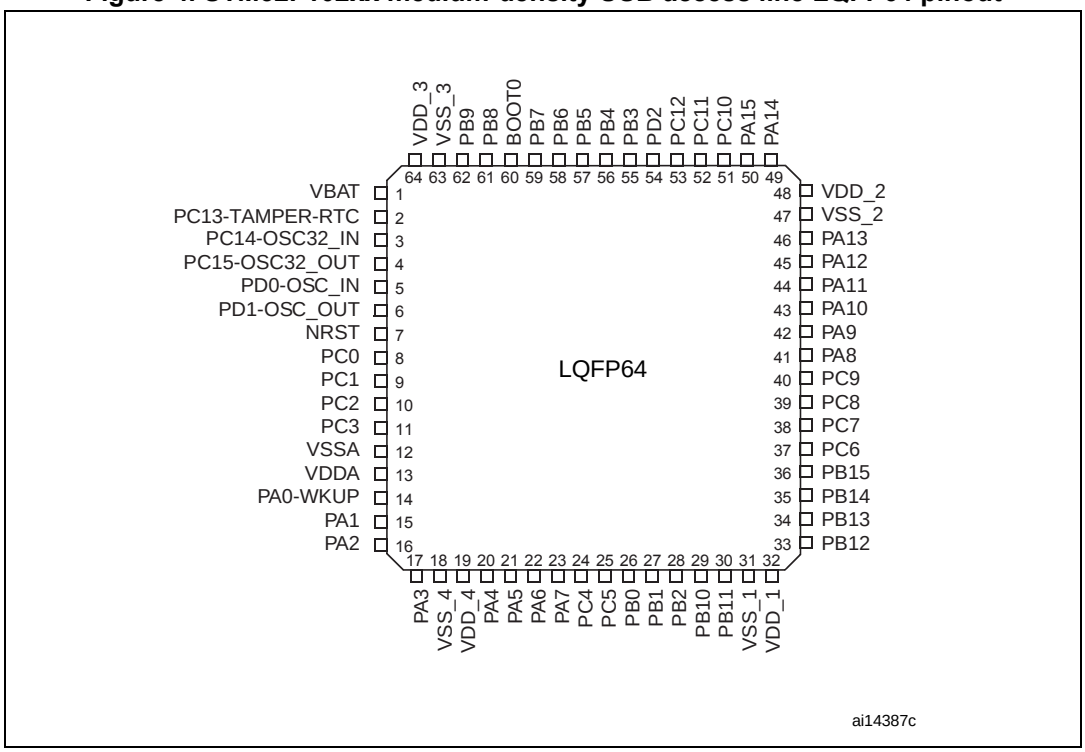


Figure 4. STM32F102xx medium-density USB access line LQFP64 pinout



5.3 Operating conditions

5.3.1 General operating conditions

Table 8. General operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-		0	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-		0	24	
f_{PCLK2}	Internal APB2 clock frequency	-		0	48	
V_{DD}	Standard operating voltage	-		2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	Must be the same potential as V_{DD}(2)		2	3.6	V
	Analog operating voltage (ADC used)			2.4	3.6	
V_{IN}	I/O input voltage	Standard IO		–0.3	V_{DD}+ 0.3	
		FTIO(3)	2 V < V_{DD} ≤ 3.6 V	–0.3	5.5	
			V_{DD} = 2 V	–0.3	5.2	
		BOOT0		0	5.5	
P_D	Power dissipation at T_A = 85 °C(4)	LQFP48		-	363	mW
		LQFP64		-	444	
T_A	Ambient temperature	Maximum power dissipation		–40	85	°C
		Low power dissipation(5)		–40	105	°C
T_J	Junction temperature range	-		–40	105	°C

1. When the ADC is used, refer to *Table 45: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.
3. To sustain a voltage higher than V_{DD}+0.3 V, the internal pull-up/pull-down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see *Section 6.3: Thermal characteristics*).
5. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see *Section 6.3: Thermal characteristics*).

5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 9. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	

Figure 10. Typical current consumption in Run mode versus temperature (at 3.6 V) - code with data processing running from RAM, peripherals enabled

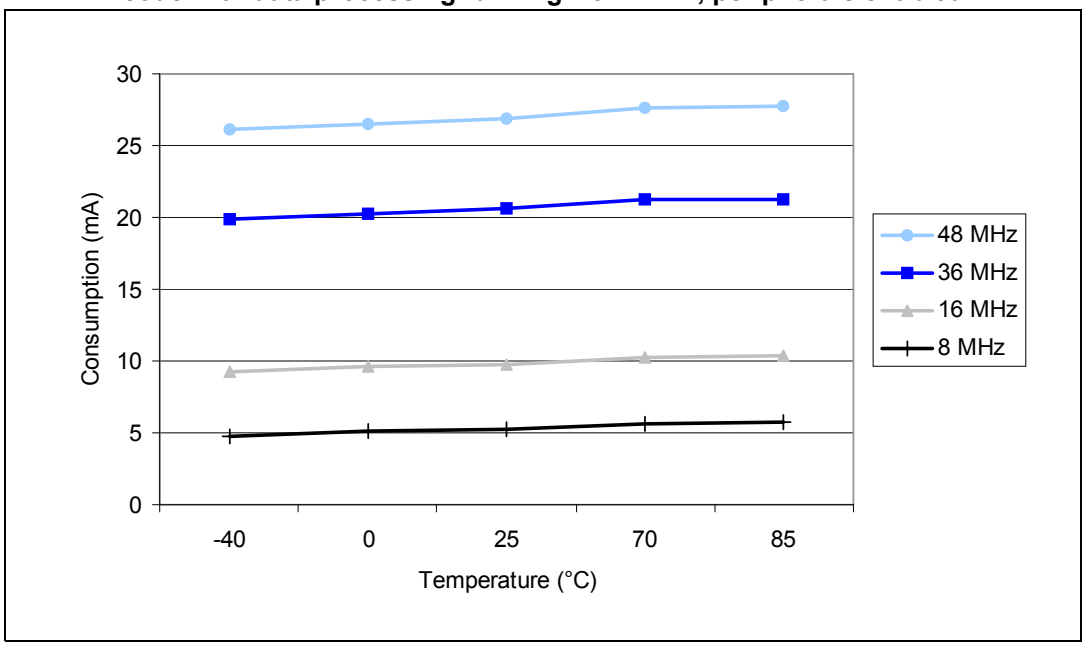
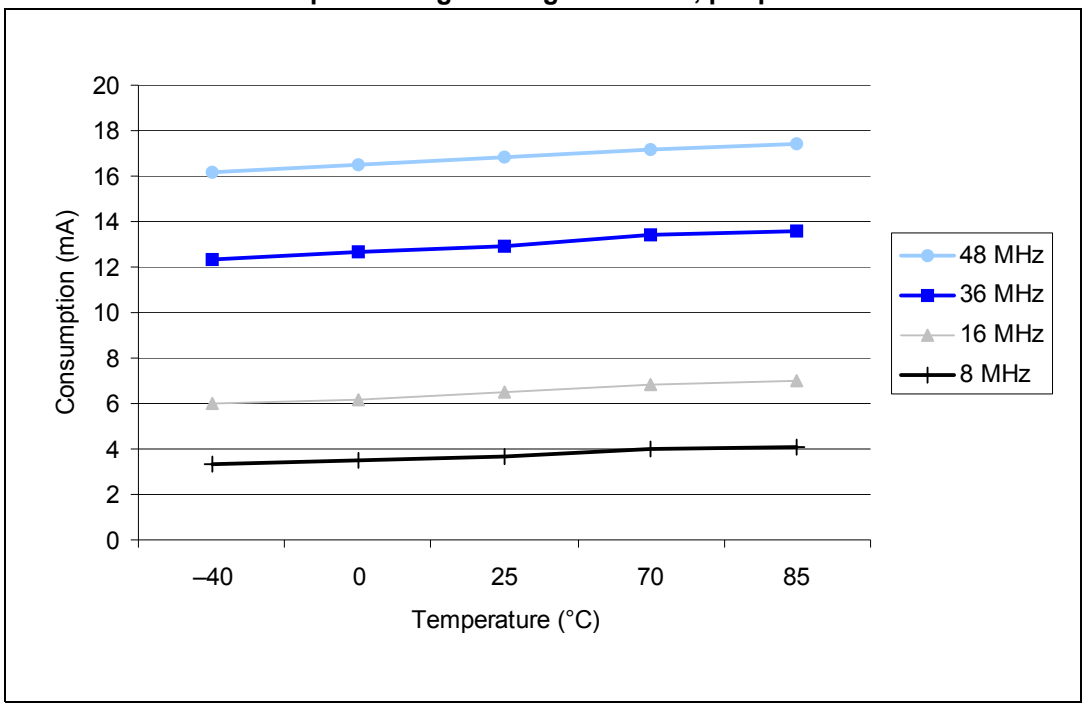


Figure 11. Typical current consumption in Run mode versus temperature (at 3.6 V) - code with data processing running from RAM, peripherals disabled



3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 17. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1) All peripherals enabled(2)	Typ(1) All peripherals disabled	Unit
I_{DD}	Supply current in Sleep mode	External clock(3)	48 MHz	9.9	3.9	mA
			36 MHz	7.6	3.1	
			24 MHz	5.3	2.3	
			16 MHz	3.8	1.8	
			8 MHz	2.1	1.2	
			4 MHz	1.6	1.1	
			2 MHz	1.3	1	
			1 MHz	1.11	0.98	
			500 kHz	1.04	0.96	
			125 kHz	0.98	0.95	
		Running on High Speed Internal RC (HSI), AHB prescaler used to reduce the frequency	48 MHz	9.3	3.3	
			36 MHz	7	2.5	
			24 MHz	4.8	1.8	
			16 MHz	3.2	1.2	
			8 MHz	1.6	0.6	
			4 MHz	1	0.5	
			2 MHz	0.72	0.47	
			1 MHz	0.56	0.44	
			500 kHz	0.49	0.42	
			125 kHz	0.43	0.41	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 18*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions as summarized in *Table 5*.

Table 18. Peripheral current consumption(1)

Peripheral		µA/MHz
AHB (up to 48 MHz)	DMA1	16.53
	BusMatrix(2)	8.33
APB1 (up to 24 MHz)	APB1-Bridge	10.28
	TIM2	32.50
	TIM3	31.39
	TIM4	31.94
	SPI2	4.17
	USART2	12.22
	USART3	12.22
	I2C1	10.00
	I2C2	10.00
	USB	17.78
	WWDG	2.50
	PWR	1.67
	BKP	2.50
	IWDG	11.67
APB2 (up to 48 MHz)	APB2-Bridge	3.75
	GPIOA	6.67
	GPIOB	6.53
	GPIOC	6.53
	GPIOD	6.53
	SPI1	4.72
	USART1	11.94
	ADC1(3) (4)	17.50

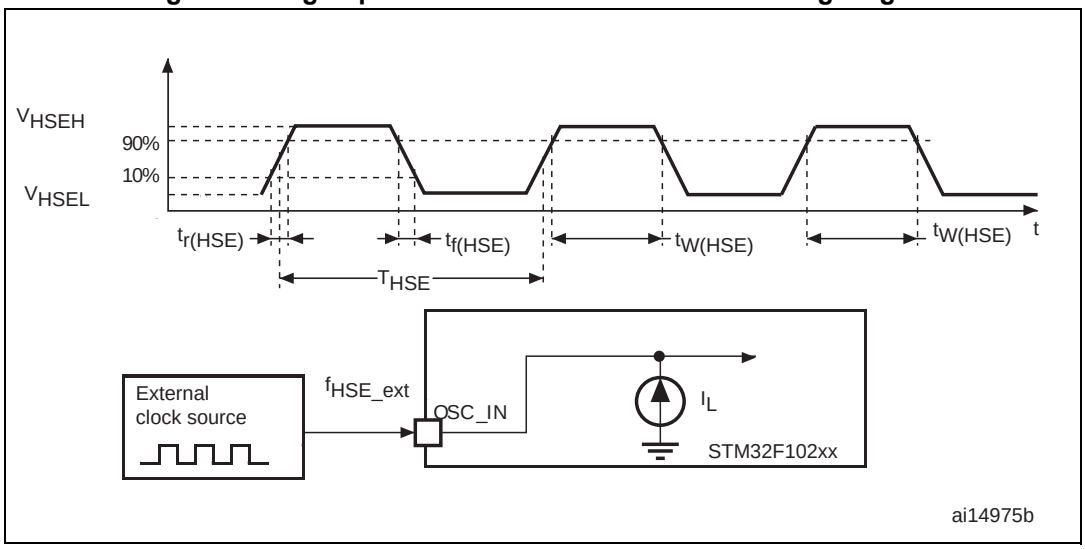
1. f_{HCLK} = 48 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.

Table 20. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)		-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle		30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Figure 16. High-speed external clock source AC timing diagram



Output voltage levels

Unless otherwise specified, the parameters given in *Table 35* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*. All I/Os are CMOS and TTL compliant.

Table 35. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output Low level voltage for an I/O pin when 8 pins are sunk at the same time	CMOS port(2). I_{IO} = +8 mA. 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output High level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	TTL port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +20 mA(4) 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–1.3	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +6 mA(4) 2.0 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Based on characterization data, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 24* and *Table 36*, respectively.

Unless otherwise specified, the parameters given in *Table 36* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 36. I/O AC characteristics(1)

MODEx [1:0] bit value(1)	Symbol	Parameter	Conditions	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		25(3)	
11	$F_{max(IO)out}$	Maximum Frequency(2)	C_L= 30 pF, V_{DD} = 2.7 V to 3.6 V	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 24*.
3. Guaranteed by design, not tested in production.

5.3.15 TIM timer characteristics

The parameters given in *Table 38* are guaranteed by design.

Refer to *Section 5.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 38. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	20.84	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 48 MHz	0	24	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	0.0208	1365	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	89.48	s

1. TIMx is used as a general term to refer to the TIM2, TIM3 and TIM4 timers.

5.3.16 Communications interfaces

I²C interface characteristics

The STM32F102xx medium-density USB access line I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in *Table 39*. Refer also to *Section 5.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Figure 31. ADC accuracy characteristics

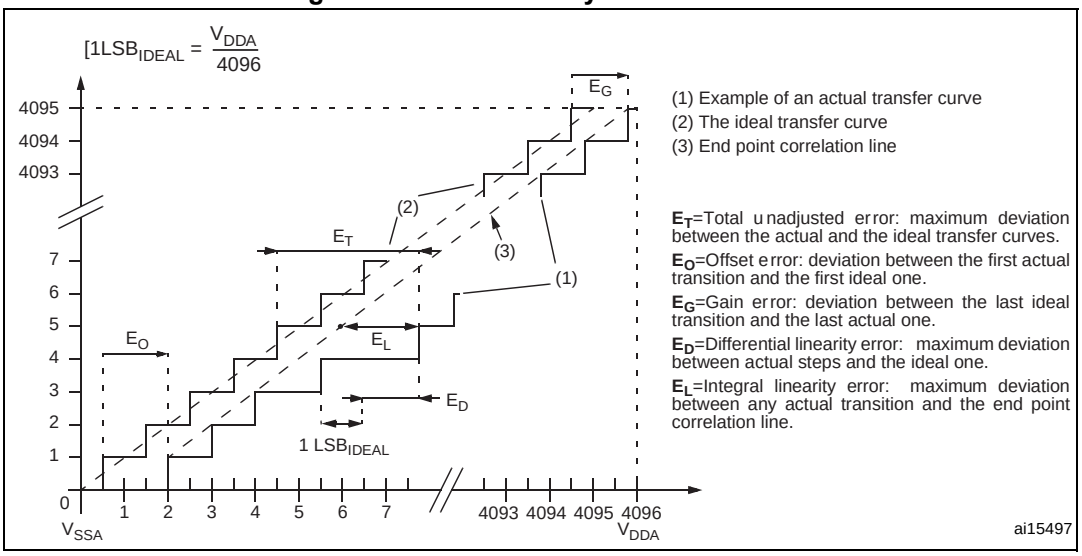
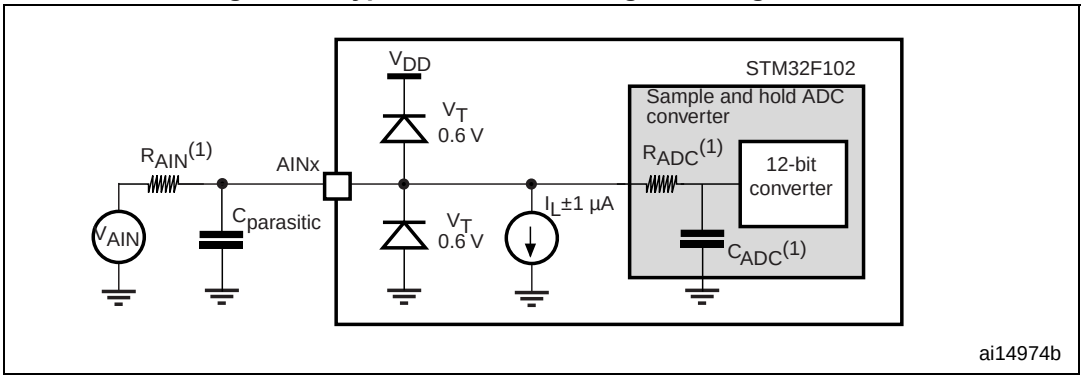


Figure 32. Typical connection diagram using the ADC

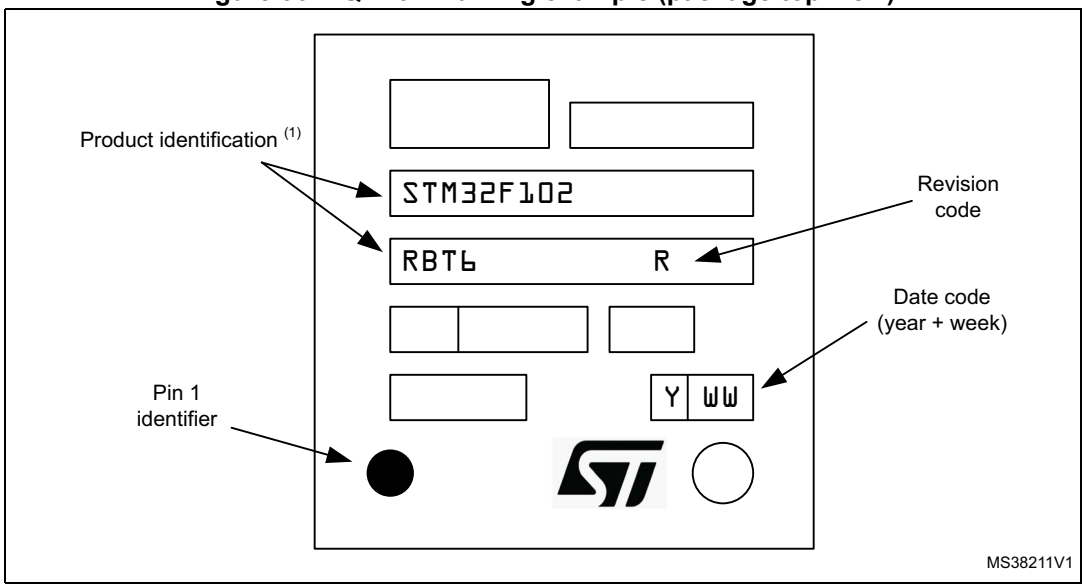


1. Refer to *Table 46* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

Device marking for LQFP64

Figure 36 is an example of topside marking orientation versus pin 1 identifier location.

Figure 36. LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7 Ordering information scheme

Table 53. Ordering information scheme

Example: STM32 F 102 C 8 T 6 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

102 = USB access line, USB 2.0 full-speed interface

Pin count

C = 48 pins

R = 64 pins

Flash memory size

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

Package

T = LQFP

Temperature range

6 = Industrial temperature range, –40 to 85 °C.

Options

xxx = programmed parts

TR = tape and reel

Table 54. Document revision history (continued)

Date	Revision	Changes
02-Aug-2013	5	Removed sentence in “Unless otherwise specified the parameters ...” in *I2C interface characteristics* section. Added V_{IN} in *Table 8: General operating conditions*. Added note *5* in *Table 23: HSI oscillator characteristics* Modified charge device model in *Table 33: ESD absolute maximum ratings* Updated ‘V_{IL}’ and ‘V_{IH}’ in *Table 34: I/O static characteristics* Added notes to *Figure 20: Standard I/O input characteristics - CMOS port*, *Figure 21: Standard I/O input characteristics - TTL port*, *Figure 22: 5 V tolerant I/O input characteristics - CMOS port* and *Figure 23: 5 V tolerant I/O input characteristics - TTL port* Updated *Figure 24: I/O AC characteristics definition* Updated note *2.* and *3.* in *Table 39: I^2C characteristics* Updated *Figure 26: I2C bus AC waveforms and measurement circuit(1)* Updated title of *Table 40: SCL frequency (f_{PCLK1}= 36 MHz, V_{DD_I2C} = 3.3 V)* Updated *Table 47: ADC characteristics* Updated *Section 6.1: Package mechanical data*
03-Jun-2015	6	Updated *Table 18: Peripheral current consumption* and *Table 39: I^2C characteristics* Updated *Section 6: Package characteristics* Updated *Section 6.1: LQFP64 package information* with addition of *Device marking for LQFP64* and *Figure 36*. Updated *Section 6.2: LQFP48 package information* with addition of *Device marking for LQFP48* and *Figure 39*. Updated Disclaimer.