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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f102rbt6

List of figures

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of STM32F102x8 and STM32F102xB medium-density USB access line microcontrollers. For more details on the whole STMicroelectronics STM32F102xx family. please refer to *Section 2.2: Full compatibility throughout the family*.

The medium-density STM32F102xx datasheet should be read in conjunction with the low-, medium- and high-density STM32F10xxx reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual.*

The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the ARM® website.

2 Description

The STM32F102xx medium-density USB access line incorporates the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a 48 MHz frequency, high-speed embedded memories (Flash memory of 64 or 128 Kbytes and SRAM of 10 or 16 Kbytes), and an extensive range of enhanced peripherals and I/Os connected to two APB buses. All devices offer standard communication interfaces (two I^2Cs, two SPIs, one USB and three USARTs), one 12-bit ADC and three general-purpose 16-bit timers.

The STM32F102xx family operates in the –40 to +85 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F102xx medium-density USB access line is delivered in the LQFP48 7 × 7 mm and LQFP64 10 × 10 mm packages.

The STM32F102xx medium-density USB access line microcontrollers are suitable for a wide range of applications.

- Application control and user interface
- Medical and handheld equipment
- PC peripherals, gaming and GPS platforms
- Industrial applications: PLC, inverters, printers, and scanners
- Alarm systems, Video intercom, and HVAC

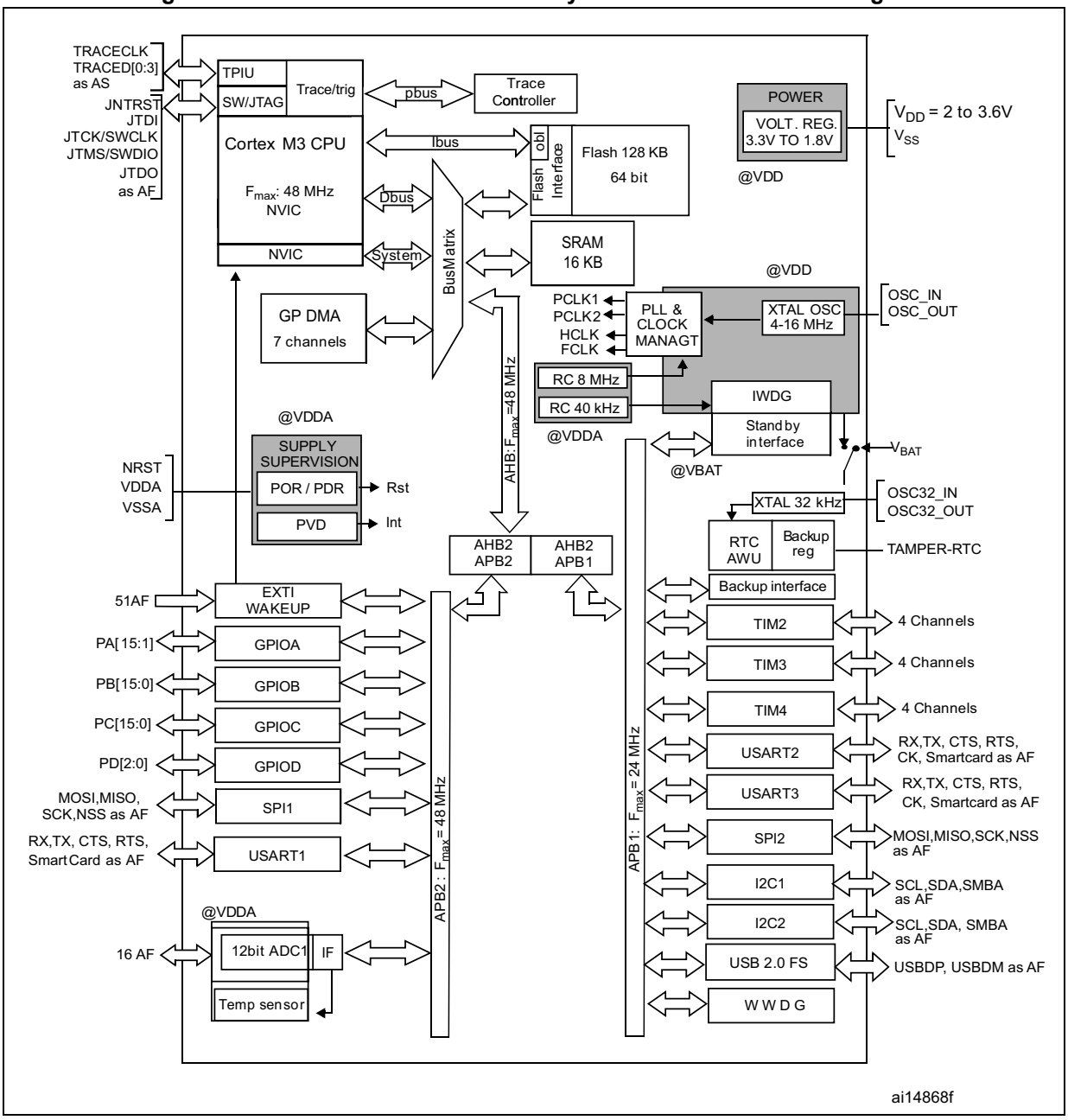
Figure 1 shows the general block diagram of the device family.

2.1 Device overview

Table 2. STM32F102x8 and STM32F102xB medium-density USB access line features and peripheral counts

Peripheral		STM32F102Cx		STM32F102Rx	
Flash - Kbytes		64	128	64	128
SRAM - Kbytes		10	16	10	16
Timers	General-purpose	3	3	3	3
Communication interfaces	SPI	2	2	2	2
	I^2C	2	2	2	2
	USART	3	3	3	3
	USB	1	1	1	1
12-bit synchronized ADC number of channels		1 10 channels		1 16 channels	
GPIOs		37		51	
CPU frequency		48 MHz			
Operating voltage		2.0 to 3.6 V			
Operating temperatures		Ambient temperature: –40 to +85 °C (see *Table 8*) Junction temperature: –40 to +105 °C (see *Table 8*)			
Packages		LQFP48		LQFP64	

Figure 1. STM32F102T8 medium-density USB access line block diagram



1. AF = alternate function on I/O port pin.
2. T_A = –40 °C to +85 °C (junction temperature up to 105 °C).

Universal synchronous/asynchronous receiver transmitter (USART)

The available USART interfaces communicate at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, support IrDA SIR ENDEC, are ISO 7816 compliant and have LIN Master/Slave capability.
The USART interfaces can be served by the DMA controller.

Serial peripheral interface (SPI)

Two SPIs are able to communicate up to 12 Mbit/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.
Both SPIs can be served by the DMA controller.

Universal serial bus (USB)

The STM32F102xx medium-density USB access line embeds an USB device peripheral compatible with the USB Full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

ADC (analog to digital converter)

The 12-bit analog to digital converter has up to 16 external channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

Temperature sensor

The temperature sensor has to generate a a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

Serial wire JTAG debug port (SWJ-DP)

The ARM® SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Table 4. Medium-density STM32F102xx pin definitions

Pins		Pin name	Type[1]	I / O level[2]	Main function[3] (after reset)	Alternate functions[3] [4]	
LQFP48	LQFP64					Default	Remap
1	1	V_{BAT}	S	-	V_{BAT}	-	-
2	2	PC13-TAMPER-RTC[5]	I/O	-	PC13[6]	TAMPER-RTC	-
3	3	PC14-OSC32_IN[5]	I/O	-	PC14[6]	OSC32_IN	-
4	4	PC15-OSC32_OUT[5]	I/O	-	PC15[6]	OSC32_OUT	-
5	5	OSC_IN	I/O	FT	OSC_IN	-	PD0[7]
6	6	OSC_OUT	I/O	FT	OSC_OUT	-	PD1[7]
7	7	NRST	I/O	-	NRST	-	-
-	8	PC0	I/O	-	PC0	ADC_IN10	-
-	9	PC1	I/O	-	PC1	ADC_IN11	-
-	10	PC2	I/O	-	PC2	ADC_IN12	-
-	11	PC3	I/O	-	PC3	ADC_IN13	-
8	12	V_{SSA}	S	-	V_{SSA}	-	-
9	13	V_{DDA}	S	-	V_{DDA}	-	-
10	14	PA0-WKUP	I/O	-	PA0	WKUP/USART2_CTS/ ADC_IN0/ TIM2_CH1_ETR[8]	-
11	15	PA1	I/O	-	PA1	USART2_RTS/ ADC_IN1/TIM2_CH2[8]	-
12	16	PA2	I/O	-	PA2	USART2_TX/ ADC_IN2/TIM2_CH3[8]	-
13	17	PA3	I/O	-	PA3	USART2_RX/ ADC_IN3/TIM2_CH4[8]	-
-	18	V_{SS_4}	S	-	V_{SS_4}	-	-
-	19	V_{DD_4}	S	-	V_{DD_4}	-	-
14	20	PA4	I/O	-	PA4	SPI1_NSS[8]/ADC_IN4 USART2_CK/	-
15	21	PA5	I/O	-	PA5	SPI1_SCK[8]/ADC_IN5	-
16	22	PA6	I/O	-	PA6	SPI1_MISO[8]/ADC_IN6/ TIM3_CH1[8]	-
17	23	PA7	I/O	-	PA7	SPI1_MOSI[8]/ADC_IN7/ TIM3_CH2[8]	-
-	24	PC4	I/O	-	PC4	ADC_IN14	-
-	25	PC5	I/O	-	PC5	ADC_IN15	-
18	26	PB0	I/O	-	PB0	ADC_IN8/TIM3_CH3[8]	-
19	27	PB1	I/O	-	PB1	ADC_IN9/TIM3_CH4[8]	-

Table 4. Medium-density STM32F102xx pin definitions (continued)

Pins		Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3) (4)	
LQFP48	LQFP64					Default	Remap
20	28	PB2	I/O	FT	PB2/BOOT1	-	-
21	29	PB10	I/O	FT	PB10	I2C2_SCL/ USART3_TX(8)	TIM2_CH3
22	30	PB11	I/O	FT	PB11	I2C2_SDA/ USART3_RX(8)	TIM2_CH4
23	31	V_{SS_1}	S	-	V_{SS_1}	-	-
24	32	V_{DD_1}	S	-	V_{DD_1}	-	-
25	33	PB12	I/O	FT	PB12	SPI2_NSS / I2C2_SMBA/ USART3_CK(8)	-
26	34	PB13	I/O	FT	PB13	SPI2_SCK(8)/ USART3_CTS	-
27	35	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_RTS	-
28	36	PB15	I/O	FT	PB15	SPI2_MOSI	-
-	37	PC6	I/O	FT	PC6	-	TIM3_CH1
-	38	PC7	I/O	FT	PC7	-	TIM3_CH2
-	39	PC8	I/O	FT	PC8	-	TIM3_CH3
-	40	PC9	I/O	FT	PC9	-	TIM3_CH4
29	41	PA8	I/O	FT	PA8	USART1_CK/MCO	-
30	42	PA9	I/O	FT	PA9	USART1_TX(8)	-
31	43	PA10	I/O	FT	PA10	USART1_RX(8)	-
32	44	PA11	I/O	FT	PA11	USART1_CTS/USB_DM	-
33	45	PA12	I/O	FT	PA12	USART1_RTS/USB_DP	-
34	46	PA13	I/O	FT	JTMS-SWDIO	-	PA13
35	47	V_{SS_2}	S	-	V_{SS_2}	-	-
36	48	V_{DD_2}	S	-	V_{DD_2}	-	-
37	49	PA14	I/O	FT	JTCK/ SWCLK	-	PA14
38	50	PA15	I/O	FT	JTDI	-	TIM2_CH1_ETR / PA15 /SPI1_NSS
-	51	PC10	I/O	FT	PC10	-	USART3_TX
-	52	PC11	I/O	FT	PC11	-	USART3_RX
-	53	PC12	I/O	FT	PC12	-	USART3_CK
-	54	PD2	I/O	FT	PD2	TIM3_ETR	-

Table 6. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	
$I_{INJ(PIN)}$ (2)	Injected current five volt tolerant pins(3)	-5/+0	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 5* for maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 5* for maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 7. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

2. To have the Standby consumption with RTC ON, add I_{DD_VBAT} (Low-speed oscillator and RTC ON) to I_{DD} Standby (when V_{DD} is present the Backup Domain is powered by V_{DD} supply).
3. Based on characterization, not tested in production.

Figure 12. Typical current consumption on V_{BAT} with RTC on versus temperature at different V_{BAT} values

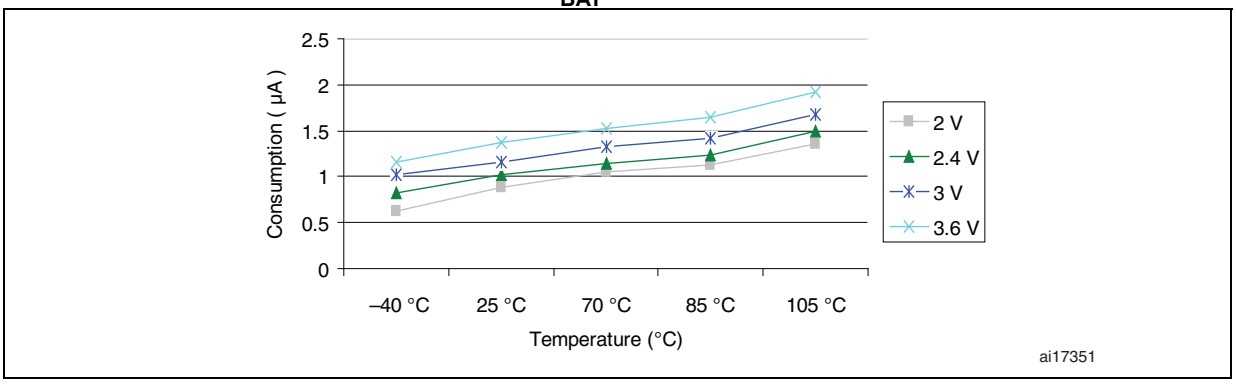
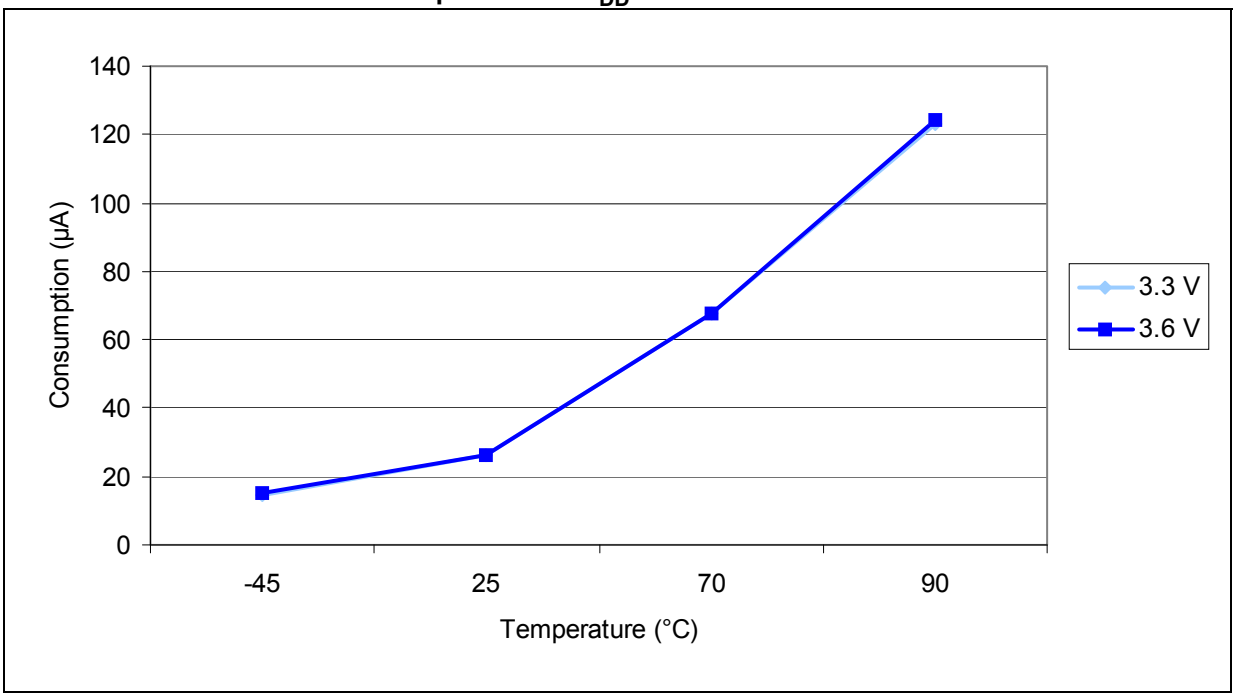


Figure 13. Typical current consumption in Stop mode with regulator in Run mode versus temperature at V_{DD} = 3.3 V and 3.6 V



Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz)
- Prefetch is on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK/4}$, $f_{PCLK2} = f_{HCLK/2}$, $f_{ADCCLK} = f_{PCLK2}/4$

The parameters given in *Table 16* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 16. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1) All peripherals enabled(2)	Typ(1) All peripherals disabled	Unit
I_{DD}	Supply current in Run mode	External clock(3)	48 MHz	24.2	18.6	mA
			36 MHz	19	14.8	
			24 MHz	12.9	10.1	
			16 MHz	9.3	7.4	
			8 MHz	5.5	4.6	
			4 MHz	3.3	2.8	
			2 MHz	2.2	1.9	
			1 MHz	1.6	1.45	
			500 kHz	1.3	1.25	
			125 kHz	1.08	1.06	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	48 MHz	23.5	17.9	
			36 MHz	18.3	14.1	
			24 MHz	12.2	9.5	
			16 MHz	8.5	6.8	
			8 MHz	4.9	4	
			4 MHz	2.7	2.2	
			2 MHz	1.6	1.4	
			1 MHz	1.02	0.9	
			500 kHz	0.73	0.67	
			125 kHz	0.5	0.48	

1. Typical values are measures at $T_A = 25$ °C, $V_{DD} = 3.3$ V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 21*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 21. HSE 4-16 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	30	-	pF
i_2	HSE driving current	V_{DD} = 3.3 V V_{IN} = V_{SS} with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization results, not tested in production.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 18*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports), This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 30. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/48 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C.	0.1 MHz to 30 MHz	7	dBµV
			30 MHz to 130 MHz	8	
			130 MHz to 1GHz	13	
			SAE EMI Level	3.5	-

5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 31. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	II	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78 IC latch-up standard.

Table 32. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

Figure 22. 5 V tolerant I/O input characteristics - CMOS port

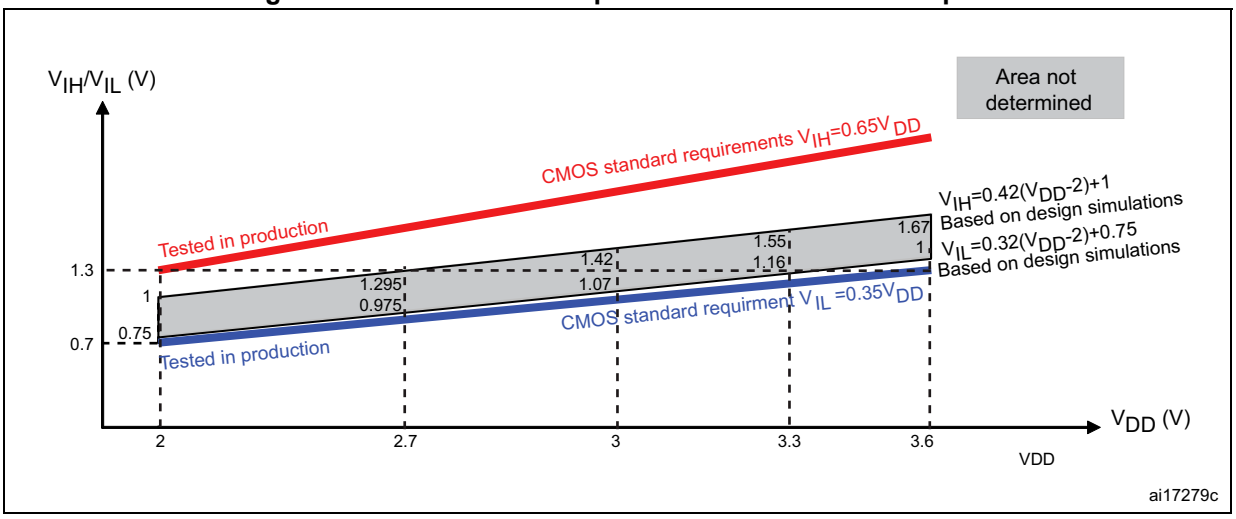
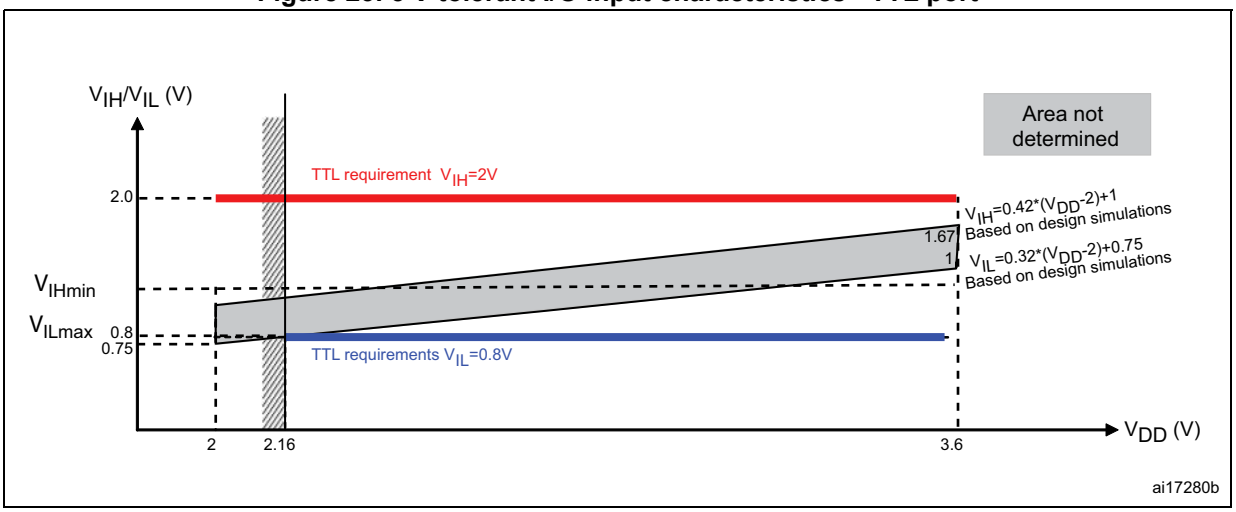


Figure 23. 5 V tolerant I/O input characteristics - TTL port



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ±3 mA. When using the GPIOs PC13 to PC15 in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum ratings specified in *Section 5.2*.

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 6*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 6*).

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 24* and *Table 36*, respectively.

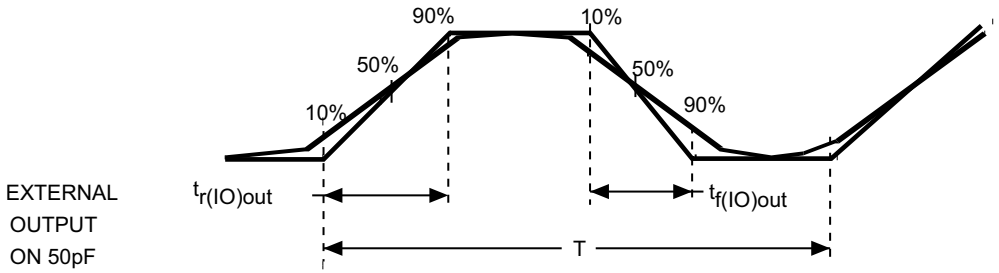
Unless otherwise specified, the parameters given in *Table 36* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 36. I/O AC characteristics(1)

MODEx [1:0] bit value(1)	Symbol	Parameter	Conditions	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		25(3)	
11	$F_{max(IO)out}$	Maximum Frequency(2)	C_L= 30 pF, V_{DD} = 2.7 V to 3.6 V	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 24*.
3. Guaranteed by design, not tested in production.

Figure 24. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%)
when loaded by 50pF

ai14131c

5.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 34*).

Unless otherwise specified, the parameters given in *Table 37* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 37. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	–0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	300	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Table 39. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)(2)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	-	3450(3)	-	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
t_{SP}	Pulse width of spikes that are suppressed by the analog filter	0	50(4)	0	50(4)	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Values guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I^2C frequencies. It must be at least 4 MHz to achieve fast mode I^2C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I2C fast mode clock.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of the SCL signal.
4. The analog filter minimum filtered spikes is above $t_{SP(max)}$ to ensure that spikes width up to $t_{SP(max)}$ are filtered.

Table 46. R_{AIN} max for f_{ADC} = 12 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.13	0.4
7.5	0.63	5.9
13.5	1.13	11.4
28.5	2.38	25.2
41.5	3.46	37.2
55.5	4.63	50
71.5	5.96	NA
239.5	19.96	NA

1. Data guaranteed by design, not tested in production.

Table 47. ADC accuracy - limited test conditions(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{PCLK2} = 48 MHz. f_{ADC} = 12 MHz, R_{AIN} < 10 kΩ. V_{DDA} = 3 V to 3.6 V T_A = 25 °C Measurements made after ADC calibration	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	

1. ADC DC accuracy values are measured after internal calibration.
2. Based on characterization, not tested in production.

Table 48. ADC accuracy(1) (2) (3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK2} = 48 MHz. f_{ADC} = 12 MHz, R_{AIN} < 10 kΩ. V_{DDA} = 2.4 V to 3.6 V Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
3. ADC accuracy vs. negative injection current: Injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.13* does not affect the ADC accuracy.
4. Based on characterization, not tested in production.

6.4.1 Evaluating the maximum junction temperature for an application

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 53: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature. Here, only temperature range 6 is available (–40 to 85 °C).

The following example shows how to calculate the temperature range needed for a given application, making it possible to check whether the required temperature range is compatible with the STM32F102xx junction temperature range.

Example: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output mode at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW

P_{Dmax} = 175 + 272 = 447 mW

Thus: P_{Dmax} = 447 mW

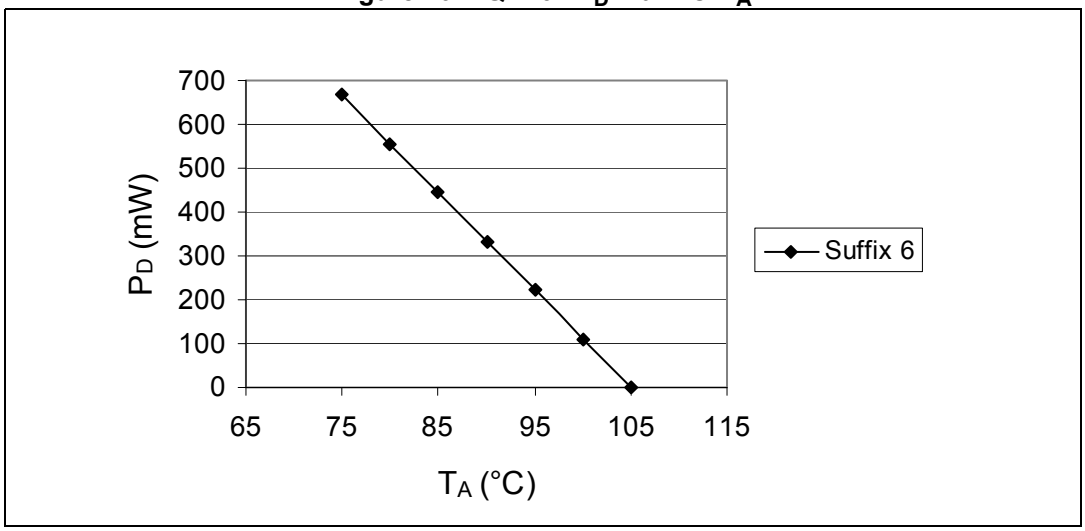
Using the values obtained in *Table 52* T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

T_{Jmax} = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.1 °C = 102.1 °C

This is within the junction temperature range of the STM32F102xx (–40 < T_J < 105 °C).

Figure 40. LQFP64 P_D max vs. T_A



8 Revision history

Table 54. Document revision history

Date	Revision	Changes
23-Sep-2008	1	Initial release.
23-Apr-2009	2	I/O information clarified *on page 1*. *Figure 1: STM32F102T8 medium-density USB access line block diagram* and *Figure 5: Memory map* modified. In *Table 4: Medium-density STM32F102xx pin definitions*: PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column. P_D value added for LQFP64 package in *Table 8: General operating conditions*. Note modified in *Table 13: Maximum current consumption in Run mode, code with data processing running from Flash* and *Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM*. *Figure 13*, *Figure 14* and *Figure 15* show typical curves. *Figure 31: ADC accuracy characteristics* modified. *Figure 33: Power supply and reference decoupling* modified. *Table 20: High-speed external user clock characteristics* and *Table 21: Low-speed external user clock characteristics* modified. ACC_{HSI} max values modified in *Table 24: HSI oscillator characteristics*. Small text changes.
22-Sep-2009	3	*Note 5.* updated in *Table 4: Medium-density STM32F102xx pin definitions*. V_{RERINT} and T_{Coeff} added to *Table 12: Embedded internal reference voltage*. Typical I_{DD_VBAT} value added in *Table 16: Typical and maximum current consumptions in Stop and Standby modes*. *Figure 12: Typical current consumption on VBAT with RTC on versus temperature at different VBAT values* added. f_{HSE_ext} min modified in *Table 20: High-speed external user clock characteristics*. C_{L1} and C_{L2} replaced by C in *Table 22: HSE 4-16 MHz oscillator characteristics* and *Table 23: LSE oscillator characteristics (fLSE = 32.768 kHz)*, notes modified and moved below the tables. *Table 24: HSI oscillator characteristics* modified. Conditions removed from *Table 26: Low-power mode wakeup timings*. *Note 1.* modified below *Figure 18: Typical application with an 8 MHz crystal*. *Figure 25: Recommended NRST pin protection* modified. IEC 1000 standard updated to IEC 61000 and SAE J1752/3 updated to IEC 61967-2 in *Section 5.3.10: EMC characteristics on page 48*. Jitter added to *Table 27: PLL characteristics*. *Table 43: SPI characteristics* modified. C_{ADC} and R_{AIN} parameters modified in *Table 47: ADC characteristics*. R_{AIN} max values modified in *Table 48: RAIN max for fADC = 12 MHz*. Small text changes.