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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f102rbt6tr

2 Description

The STM32F102xx medium-density USB access line incorporates the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a 48 MHz frequency, high-speed embedded memories (Flash memory of 64 or 128 Kbytes and SRAM of 10 or 16 Kbytes), and an extensive range of enhanced peripherals and I/Os connected to two APB buses. All devices offer standard communication interfaces (two I^2Cs, two SPIs, one USB and three USARTs), one 12-bit ADC and three general-purpose 16-bit timers.

The STM32F102xx family operates in the –40 to +85 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

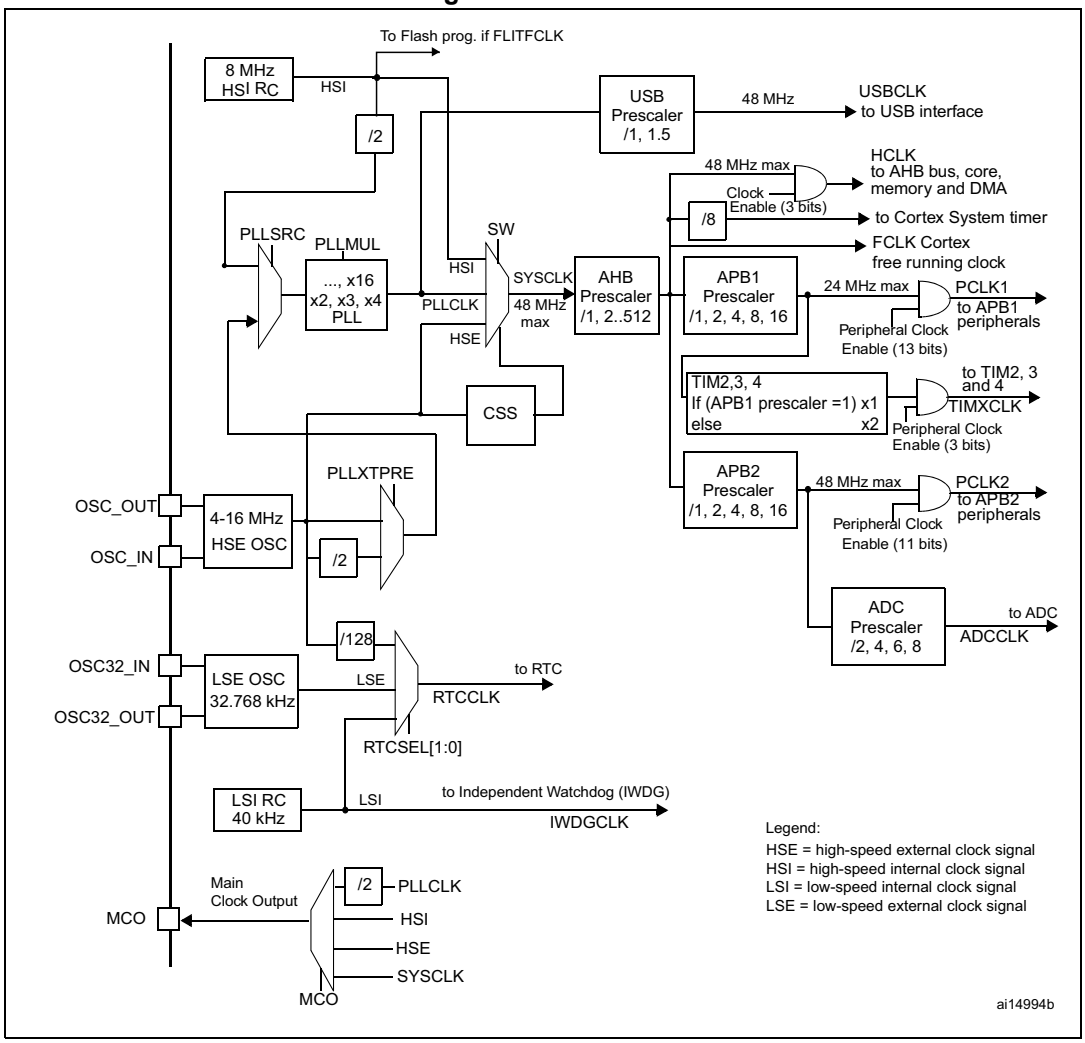
The STM32F102xx medium-density USB access line is delivered in the LQFP48 7 × 7 mm and LQFP64 10 × 10 mm packages.

The STM32F102xx medium-density USB access line microcontrollers are suitable for a wide range of applications.

- Application control and user interface
- Medical and handheld equipment
- PC peripherals, gaming and GPS platforms
- Industrial applications: PLC, inverters, printers, and scanners
- Alarm systems, Video intercom, and HVAC

Figure 1 shows the general block diagram of the device family.

Figure 2. Clock tree



1. For the USB function to be available, both HSE and PLL must be enabled, with the USB clock output (USBCLK) at 48 MHz.
2. To have an ADC conversion time of 1.2 µs, APB2 must be at 12 MHz, 24 MHz or 48 MHz.
3. The Flash memory programming interface clock (FLITFCLK) is always the HSI clock.

2.2 Full compatibility throughout the family

The STM32F102xx is a complete family whose members are fully pin-to-pin, software and feature compatible. In the reference manual, the STM32F102x4 and STM32F102x6 are referred to as low-density devices and the STM32F102x8 and STM32F102xB are referred to as medium-density devices.

Low-density devices are an extension of the STM32F102x8/B devices, they are specified in the STM32F102x4/6 datasheet. Low-density devices feature lower Flash memory and RAM capacities, a timer and a few communication interfaces less.
The STM32F102x4 and STM32F102x6 are a drop-in replacement for the STM32F102x8/B medium-density devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.

Moreover the STM32F102xx family is fully compatible with all existing STM32F101xx access line and STM32F103xx performance line devices.

Table 3. STM32F102xx USB access line family

Pinout	Low-density STM32F102xx devices		Medium-density STM32F102xx devices	
	16 KB Flash	32 KB Flash(1)	64 KB Flash	128 KB Flash
	4 KB RAM	6 KB RAM	10 KB RAM	16 KB RAM
64 48	2 × USARTs, 2 × 16-bit timers 1 × SPI, 1 × I^2C, 1 × ADC, 1 × USB		3 × USARTs, 3 × 16-bit timers 2 × SPIs, 2 × I2Cs, 1 × ADC, 1 × USB	
36	-	-	2 × USARTs, 3 × 16-bit timers 1× SPI, 1× I2C, 1 × ADC, 1 × USB	-

1. For orderable part numbers that do not show the A internal code after the temperature range code (6), the reference datasheet for electrical characteristics is that of the STM32F102x8/B medium-density devices.

2.3 Overview

ARM® Cortex®-M3 core with embedded Flash and SRAM

The ARM® Cortex®-M3 processor is the latest generation of ARM® processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM® core in the memory size usually associated with 8- and 16-bit devices.

The STM32F102xx medium-density USB access line having an embedded ARM® core is therefore compatible with all ARM® tools and software.

Embedded Flash memory

64 or 128 Kbytes of embedded Flash is available for storing programs and data.

CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity, In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

Embedded SRAM

10 or 16 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

Nested vectored interrupt controller (NVIC)

The STM32F102xx medium-density USB access line embeds a nested vectored interrupt controller able to handle up to 36 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detectors lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect external line with pulse width lower than the Internal APB2 clock period. Up to 51 GPIOs are connected to the 16 external interrupt lines.

Clocks and startup

System clock selection is performed on startup. however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the High Speed APB (APB2) and the low Speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 48 MHz. See *Figure 2* for details on the clock tree.

register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock. it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

General-purpose timers (TIMx)

There are 3 synchronizable general-purpose timers embedded in the STM32F102xx medium-density USB access line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture, output compare, PWM or one-pulse mode output. This gives up to 12 input captures / output compares / PWMs on the LQFP48 and LQFP64 packages.
The general-purpose timers can work together via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode.

Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

I²C bus

Two I²C bus interfaces can operate in multi-master and slave modes. They can support standard and fast modes. They support dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

Universal synchronous/asynchronous receiver transmitter (USART)

The available USART interfaces communicate at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, support IrDA SIR ENDEC, are ISO 7816 compliant and have LIN Master/Slave capability.
The USART interfaces can be served by the DMA controller.

Serial peripheral interface (SPI)

Two SPIs are able to communicate up to 12 Mbit/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.
Both SPIs can be served by the DMA controller.

Universal serial bus (USB)

The STM32F102xx medium-density USB access line embeds an USB device peripheral compatible with the USB Full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

ADC (analog to digital converter)

The 12-bit analog to digital converter has up to 16 external channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

Temperature sensor

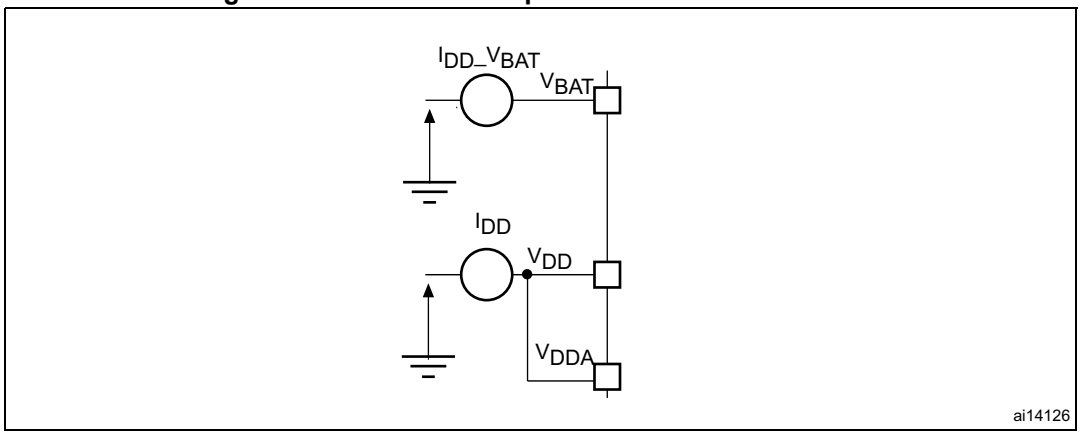
The temperature sensor has to generate a a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

Serial wire JTAG debug port (SWJ-DP)

The ARM® SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

5.1.7 Current consumption measurement

Figure 9. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 5: Voltage characteristics*, *Table 6: Current characteristics*, and *Table 7: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD} - V_{SS}$	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five volt tolerant pin	V_{SS} – 0.3	V_{DD} + 4.0	
	Input voltage on any other pin	V_{SS} – 0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.11: Absolute maximum ratings (electrical sensitivity)*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 6: Current characteristics* for the maximum allowed injected current values.

Table 11. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +85 °C	1.16	1.20	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	-	5.1	17.1(2)	µs
V_{RERINT}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V ±10 mV	-	-	10	mV
T_{Coeff}(2)	Temperature coefficient	-	-	-	100	ppm/ °C

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 9: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz)
- Prefetch in on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK/2}$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 12* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 18*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions as summarized in *Table 5*.

Table 18. Peripheral current consumption(1)

Peripheral		µA/MHz
AHB (up to 48 MHz)	DMA1	16.53
	BusMatrix(2)	8.33
APB1 (up to 24 MHz)	APB1-Bridge	10.28
	TIM2	32.50
	TIM3	31.39
	TIM4	31.94
	SPI2	4.17
	USART2	12.22
	USART3	12.22
	I2C1	10.00
	I2C2	10.00
	USB	17.78
	WWDG	2.50
	PWR	1.67
	BKP	2.50
	IWDG	11.67
APB2 (up to 48 MHz)	APB2-Bridge	3.75
	GPIOA	6.67
	GPIOB	6.53
	GPIOC	6.53
	GPIOD	6.53
	SPI1	4.72
	USART1	11.94
	ADC1(3) (4)	17.50

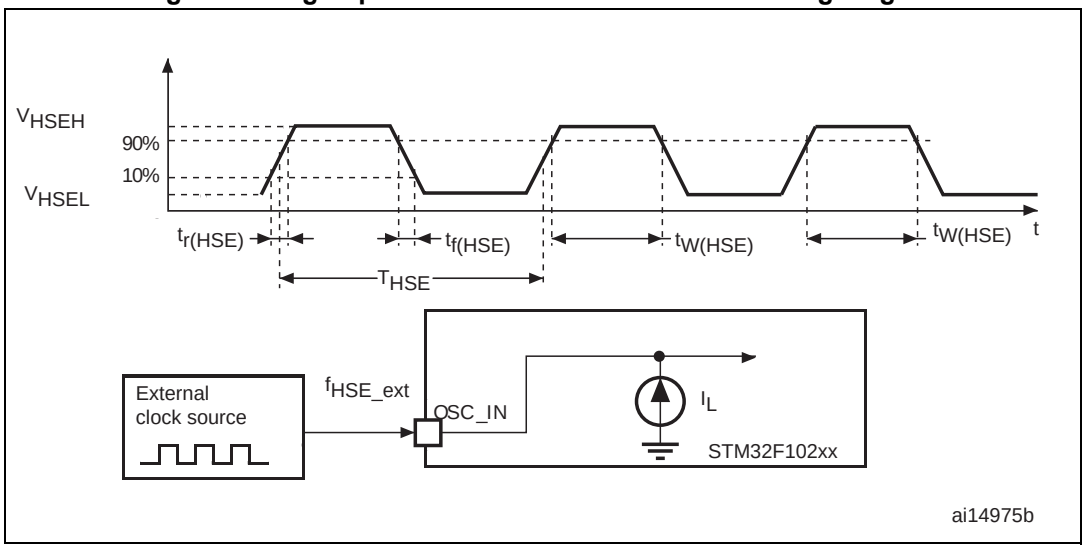
1. f_{HCLK} = 48 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.

Table 20. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)		-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle		30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Figure 16. High-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 21*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 21. HSE 4-16 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	30	-	pF
i_2	HSE driving current	V_{DD} = 3.3 V V_{IN} = V_{SS} with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization results, not tested in production.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 18*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

2. Refer to application note AN2868 “STM32F10xxx internal RC oscillator (HSI) calibration” available from the ST website www.st.com.
3. Guaranteed by design, not tested in production.
4. Based on characterization, not tested in production.
5. The actual frequency of HSI oscillator may be impacted by a reflow, but does not drift out of the specified range.

Low-speed internal (LSI) RC oscillator

Table 24. LSI oscillator characteristics (1)

Symbol	Parameter	Min(2)	Typ	Max	Unit
f_{LSI}	Frequency	30	40	60	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.65	1.2	µA

1. V_{DD} = 3 V, T_A = –40 to 85 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in *Table 25* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 25. Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	1.8	µs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	3.6	µs
	Wakeup from Stop mode (regulator in low-power mode)	5.4	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	50	µs

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

5.3.8 PLL characteristics

The parameters given in *Table 26* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Figure 22. 5 V tolerant I/O input characteristics - CMOS port

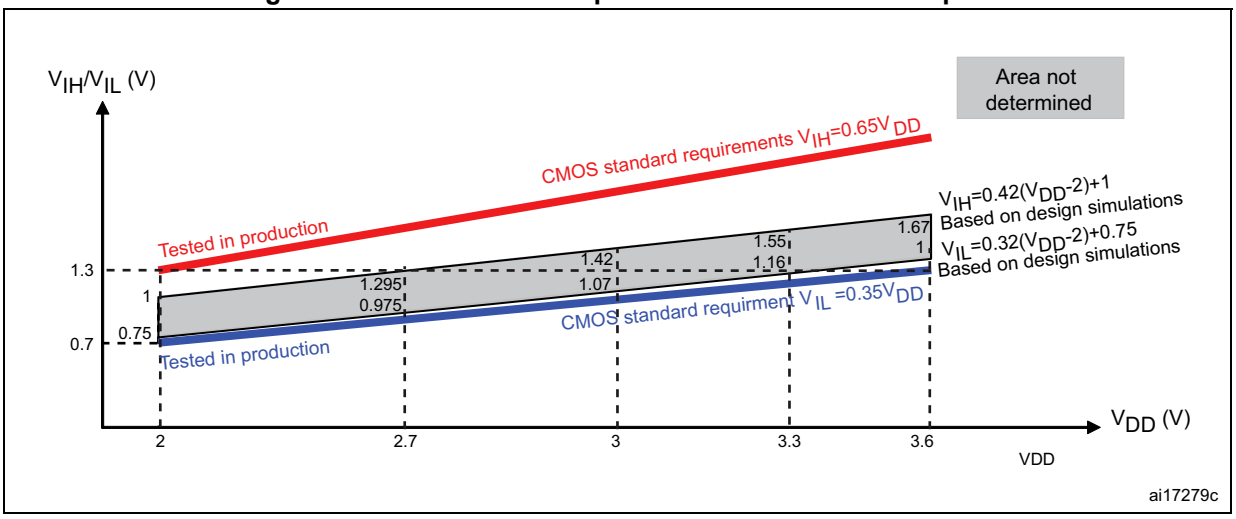
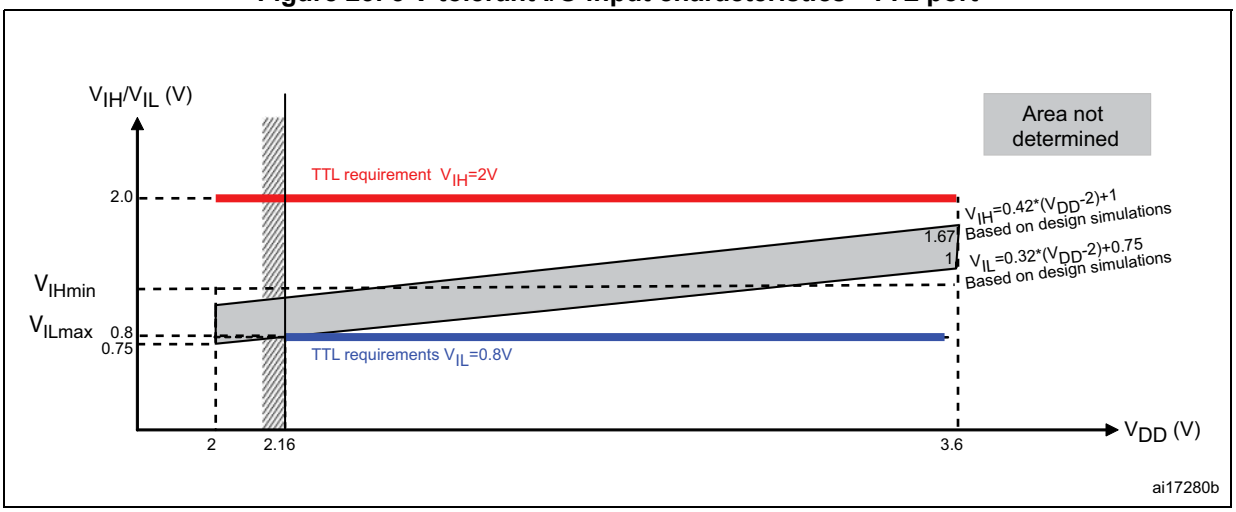


Figure 23. 5 V tolerant I/O input characteristics - TTL port



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ±3 mA. When using the GPIOs PC13 to PC15 in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum ratings specified in *Section 5.2*.

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 6*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 6*).

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 8*.

Refer to *Section 5.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 41. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	$2t_{PCLK}$	-	
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	50	60	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5	-	
		Slave mode	5	-	
$t_{h(MI)}$ (1)	Data input hold time	Master mode	5	-	
$t_{h(SI)}$ (1)		Slave mode	4	-	
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	$3t_{PCLK}$	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	2	10	
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	25	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	5	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$ (1)		Master mode (after enable edge)	2	-	

1. Based on characterization, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 27. SPI timing diagram - slave mode and CPHA=0

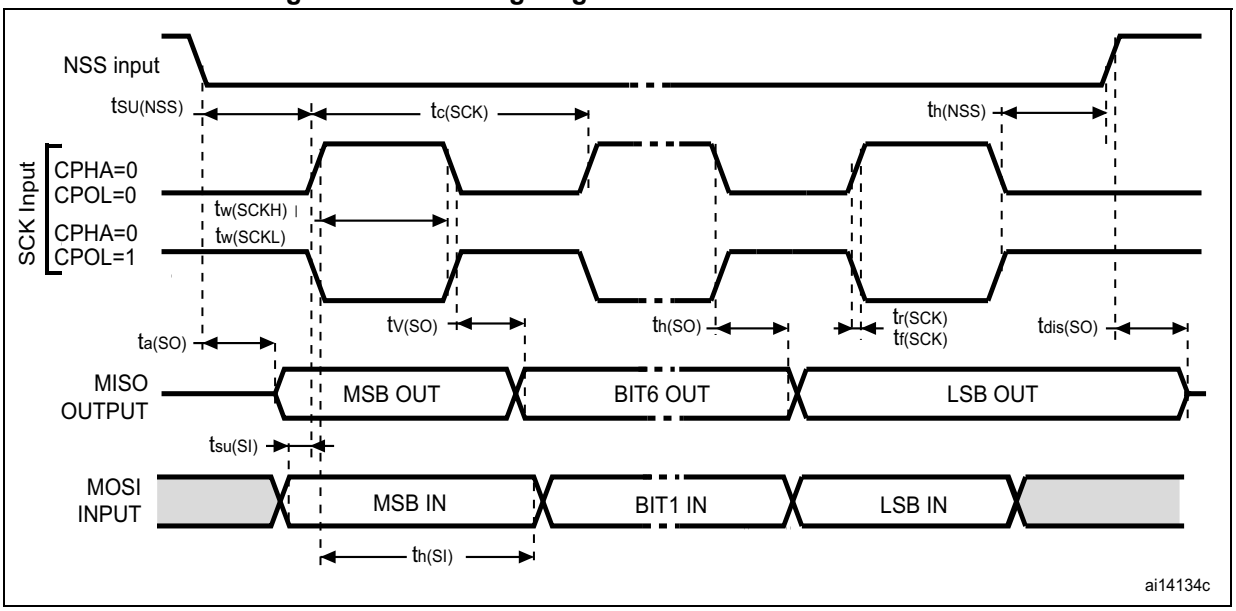
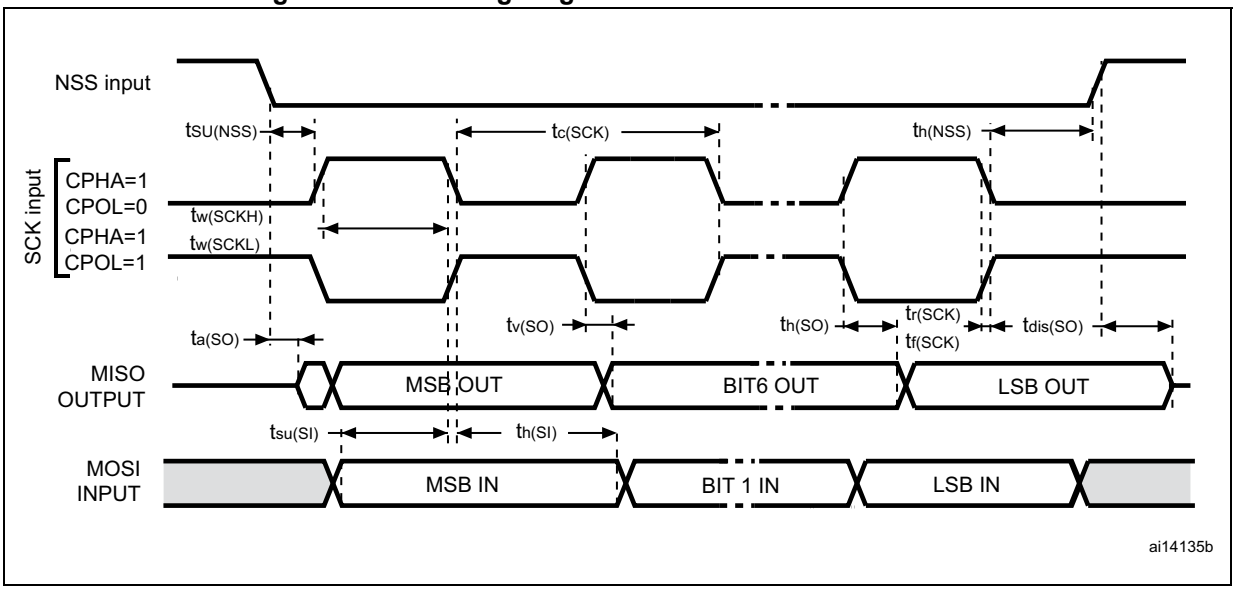


Figure 28. SPI timing diagram - slave mode and CPHA=1(1)



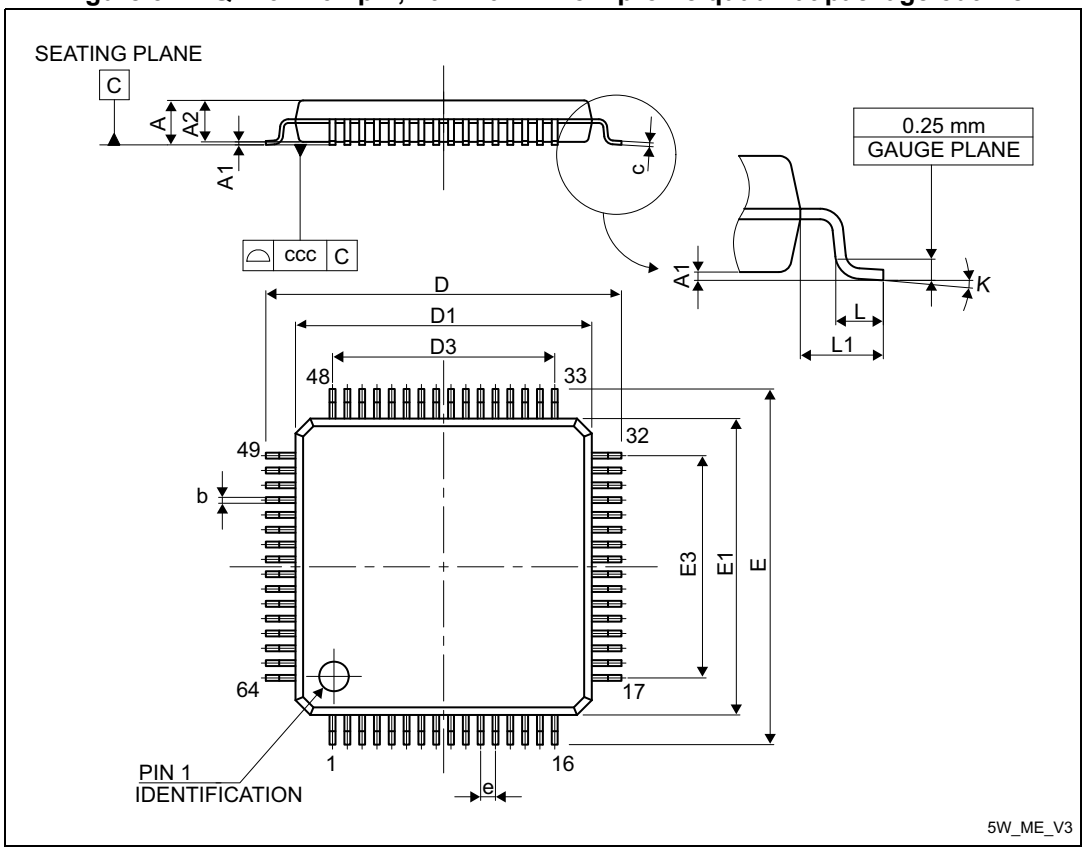
1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

6 Package characteristics

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

6.1 LQFP64 package information

Figure 34. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 50. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

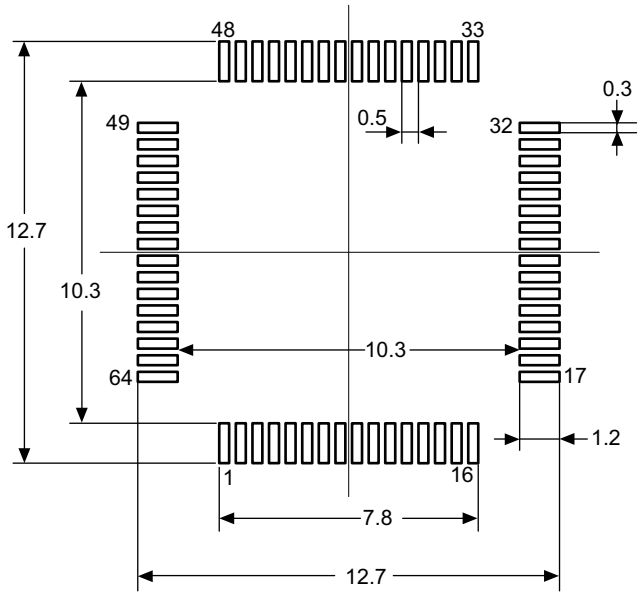
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106

Table 50. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 35. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Table 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

8 Revision history

Table 54. Document revision history

Date	Revision	Changes
23-Sep-2008	1	Initial release.
23-Apr-2009	2	I/O information clarified *on page 1*. *Figure 1: STM32F102T8 medium-density USB access line block diagram* and *Figure 5: Memory map* modified. In *Table 4: Medium-density STM32F102xx pin definitions*: PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column. P_D value added for LQFP64 package in *Table 8: General operating conditions*. Note modified in *Table 13: Maximum current consumption in Run mode, code with data processing running from Flash* and *Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM*. *Figure 13*, *Figure 14* and *Figure 15* show typical curves. *Figure 31: ADC accuracy characteristics* modified. *Figure 33: Power supply and reference decoupling* modified. *Table 20: High-speed external user clock characteristics* and *Table 21: Low-speed external user clock characteristics* modified. ACC_{HSI} max values modified in *Table 24: HSI oscillator characteristics*. Small text changes.
22-Sep-2009	3	*Note 5.* updated in *Table 4: Medium-density STM32F102xx pin definitions*. V_{RERINT} and T_{Coeff} added to *Table 12: Embedded internal reference voltage*. Typical I_{DD_VBAT} value added in *Table 16: Typical and maximum current consumptions in Stop and Standby modes*. *Figure 12: Typical current consumption on VBAT with RTC on versus temperature at different VBAT values* added. f_{HSE_ext} min modified in *Table 20: High-speed external user clock characteristics*. C_{L1} and C_{L2} replaced by C in *Table 22: HSE 4-16 MHz oscillator characteristics* and *Table 23: LSE oscillator characteristics (fLSE = 32.768 kHz)*, notes modified and moved below the tables. *Table 24: HSI oscillator characteristics* modified. Conditions removed from *Table 26: Low-power mode wakeup timings*. *Note 1.* modified below *Figure 18: Typical application with an 8 MHz crystal*. *Figure 25: Recommended NRST pin protection* modified. IEC 1000 standard updated to IEC 61000 and SAE J1752/3 updated to IEC 61967-2 in *Section 5.3.10: EMC characteristics on page 48*. Jitter added to *Table 27: PLL characteristics*. *Table 43: SPI characteristics* modified. C_{ADC} and R_{AIN} parameters modified in *Table 47: ADC characteristics*. R_{AIN} max values modified in *Table 48: RAIN max for fADC = 12 MHz*. Small text changes.

Table 54. Document revision history (continued)

Date	Revision	Changes
27-Sep-2012	4	*Figure 2: Clock tree*: added FLITFCLK and *Note 3.*, and modified *Note 1.*. Updated *Note 2.* in *Table 41: I2C characteristics*. Updated *Figure 25: Recommended NRST pin protection*. Changed $t_{w(SCKH)}$ to $t_{w(SCLH)}$, $t_{w(SCKL)}$ to $t_{w(SCLL)}$, $t_{r(SCK)}$ to $t_{r(SCL)}$, $t_{f(SCK)}$ to $t_{f(SCL)}$, and $t_{su(STA:STO)}$ to $t_{w(STO:STA)}$ in *Figure 26: I2C bus AC waveforms and measurement circuit(1)*. Changed note for I_{lkg} and R_{PU} and updated *Note 1.*content in *Table 36: I/O static characteristics*. Updated text related to CMOS and TTL compliance and added *Figure 20*, *Figure 21*, *Figure 22*, and *Figure 23*. Updated *Section : Output driving current*. In *Table 43: SPI characteristics*, removed note 1 related to SPI1 remapped characteristics. Added $DuCy_{(HSI)}$ in *Table 24: HSI oscillator characteristics*. *Table 23: LSE oscillator characteristics (fLSE = 32.768 kHz)*: removed note 2 related to oscillator selection, updated *Note 2.*, and $t_{SU(LSE)}$ specified for various ambient temperature values. Updated *Note 2.* and *Note 3.* below *Figure 35: Recommended footprint (dimensions in mm)(1)(2)(3)*. *Table 37: Output voltage characteristics*: updated V_{OL} and V_{OH} conditions for TTL and CMOS outputs and added *Note 2.*. Replaced “TBD” by “-” for “max” specification of “Supply current in Standby mode” in *Table 16: Typical and maximum current consumptions in Stop and Standby modes*. Removed “except for analog inputs” from paragraph “GPIOS (general-purpose inputs/outputs) in *Chapter 2.3: Overview*. Updated $t_{w(HSE)}$ min value in *Table 20: High-speed external user clock characteristics*. Added *Note 2.* in *Table 5: Voltage characteristics*. Updated *Note 3.*, *Note 4.* and *Note 5.* in *Table 6: Current characteristics*. Updated *Note 1.* in *Table 38: I/O AC characteristics*. Added *Chapter 5.3.12: I/O current injection characteristics*. Updated *Note 2.* in *Table 41: I2C characteristics*. Updated “Output driving current” paragraph in *Chapter 5.3.13: I/O port characteristics*. Removed Note 4 and updated *Note 3.* in *Table 41: I2C characteristics*. Updated *Figure 29: SPI timing diagram - master mode(1)* (SCK Output instead of Input). Replaced every occurrence of USBDP or USBDM by USB_DP or USB_DM, respectively.