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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p87lpc764bdh-512

ORDERING INFORMATION

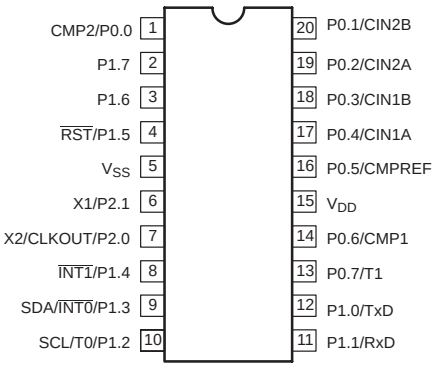
Type number	Package				
	Name	Description	Frequency	Temperature Range (°C)	Version
P87LPC764BD/01	SO20	plastic small outline package; 20 leads; body width 7.5 mm	20 MHz (5 V), 10 MHz (3 V)	0 to +70	SOT163-1
P87LPC764BD	SO20	plastic small outline package; 20 leads; body width 7.5 mm	20 MHz (5 V), 10 MHz (3 V)	0 to +70	SOT163-1
P87LPC764BDH/01	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	20 MHz (5 V) 10 MHz (3 V)	0 to +70	SOT360-1
P87LPC764BDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	20 MHz (5 V) 10 MHz (3 V)	0 to +70	SOT360-1
P87LPC764BN	DIP20	plastic dual in-line package; 20 leads (300 mil)	20 MHz (5 V), 10 MHz (3 V)	0 to +70	SOT146-1
P87LPC764FN	DIP20	plastic dual in-line package; 20 leads (300 mil)	20 MHz (5 V), 10 MHz (3 V)	–40 to +85	SOT146-1
P87LPC764FD	SO20	plastic small outline package; 20 leads; body width 7.5 mm	20 MHz (5 V), 10 MHz (3 V)	–40 to +85	SOT163-1
P87LPC764FDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	20 MHz (5 V), 10 MHz (3 V)	–40 to +85	SOT360-1
P87LPC764HDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	16 MHz (5 V)	–40 to +125	SOT360-1

DEVICE COMPARISON TABLE[1]

Part type	Internal RC oscillator
P87LPC764BD/01, BDH/01	±2.5% to 5%
P87LPC764BDH, HDH	±10%
P87LPC764BD, BN, FN, FD, FDH	±25%

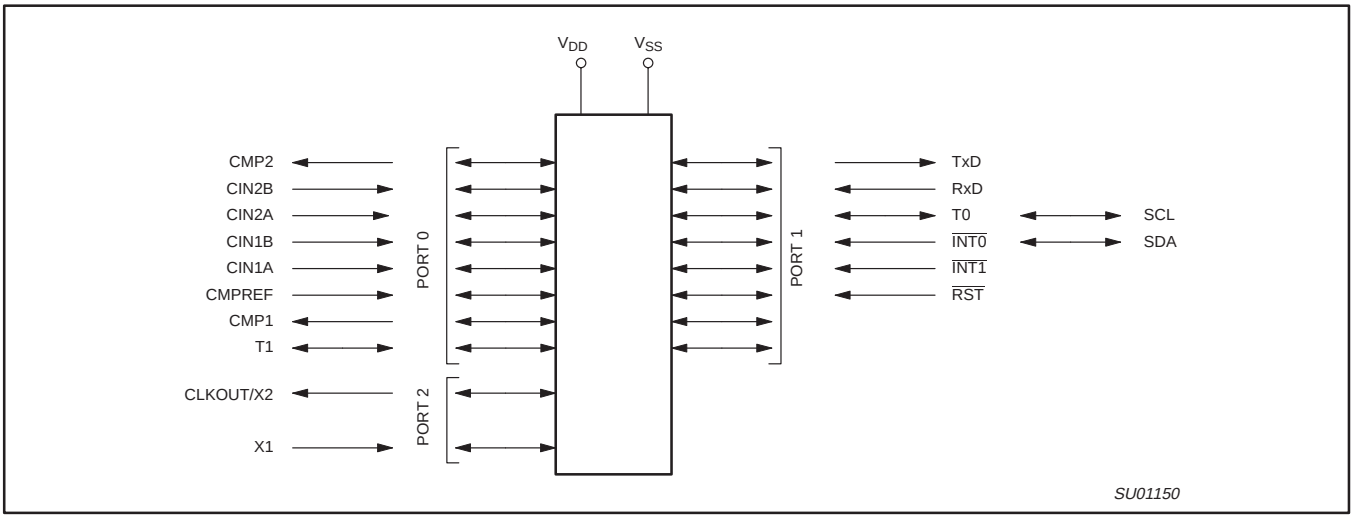
NOTE:
1. Please see AC and DC characteristics for more details.

PIN CONFIGURATION, 20-PIN DIP, SO, AND TSSOP PACKAGES

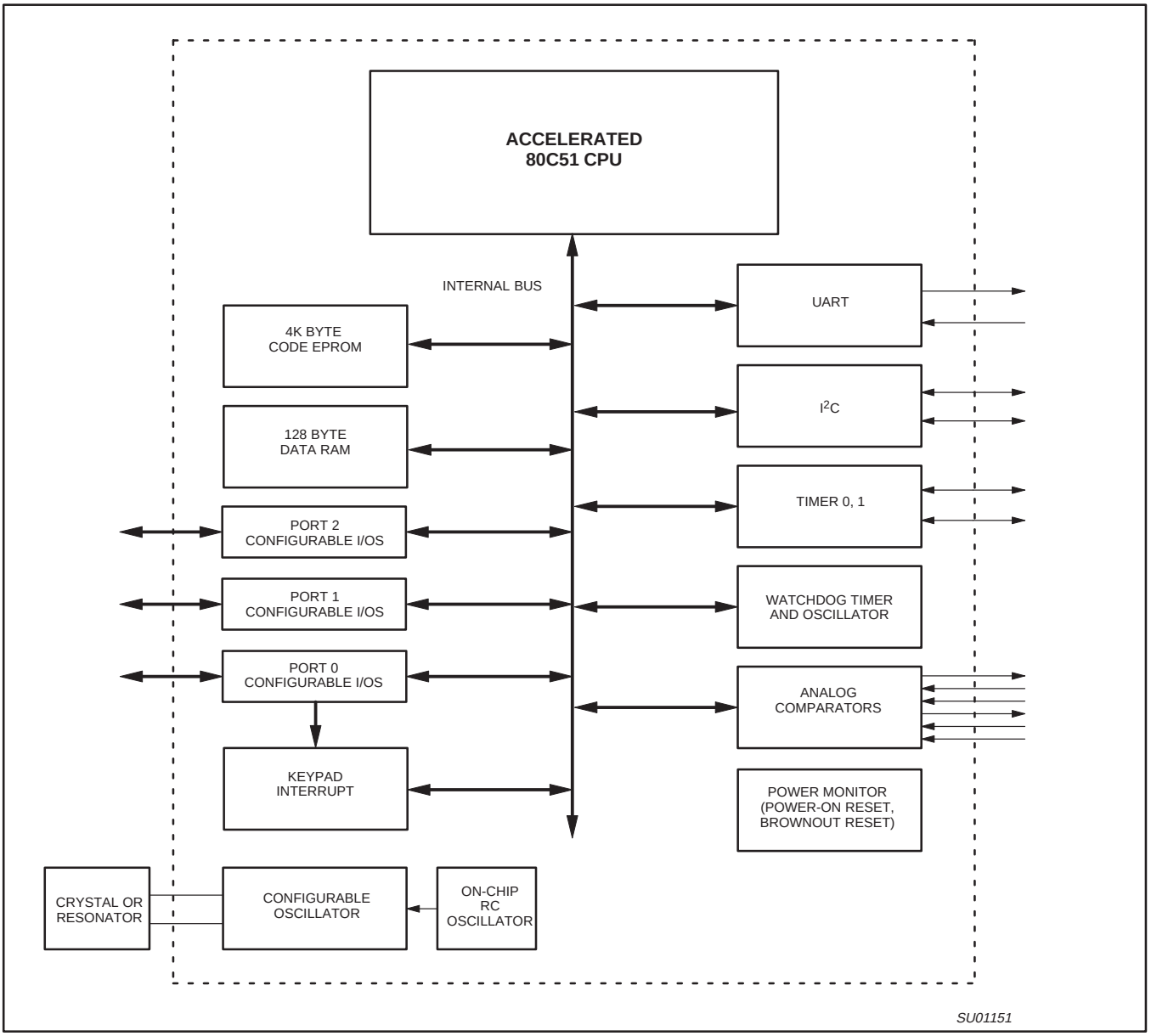


SU01149

LOGIC SYMBOL



BLOCK DIAGRAM



PIN DESCRIPTIONS

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION		
P0.0–P0.7	1, 13, 14, 16–20	I/O	**Port 0**: Port 0 is an 8-bit I/O port with a user-configurable output type. Port 0 latches are configured in the quasi-bidirectional mode and have either ones or zeros written to them during reset, as determined by the PRHI bit in the UCFG1 configuration byte. The operation of port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to the section on I/O port configuration and the DC Electrical Characteristics for details. The Keyboard Interrupt feature operates with port 0 pins. Port 0 also provides various special functions as described below.		
	1	O	**P0.0**	**CMP2**	Comparator 2 output.
	20	I	**P0.1**	**CIN2B**	Comparator 2 positive input B.
	19	I	**P0.2**	**CIN2A**	Comparator 2 positive input A.
	18	I	**P0.3**	**CIN1B**	Comparator 1 positive input B.
	17	I	**P0.4**	**CIN1A**	Comparator 1 positive input A.
	16	I	**P0.5**	**CMPREF**	Comparator reference (negative) input.
	14	O	**P0.6**	**CMP1**	Comparator 1 output.
	13	I/O	**P0.7**	**T1**	Timer/counter 1 external count input or overflow output.
P1.0–P1.7	2–4, 8–12	I/O	**Port 1**: Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. Port 1 latches are configured in the quasi-bidirectional mode and have either ones or zeros written to them during reset, as determined by the PRHI bit in the UCFG1 configuration byte. The operation of the configurable port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to the section on I/O port configuration and the DC Electrical Characteristics for details. Port 1 also provides various special functions as described below.		
	12	O	**P1.0**	**TxD**	Transmitter output for the serial port.
	11	I	**P1.1**	**RxD**	Receiver input for the serial port.
	10	I/O	**P1.2**	**T0**	Timer/counter 0 external count input or overflow output.
		I/O		**SCL**	I^2C serial clock input/output. When configured as an output, P1.2 is open drain, in order to conform to I^2C specifications.
	9	I	**P1.3**	**$\overline{\text{INT0}}$**	External interrupt 0 input.
		I/O		**SDA**	I^2C serial data input/output. When configured as an output, P1.3 is open drain, in order to conform to I^2C specifications.
	8	I	**P1.4**	**$\overline{\text{INT1}}$**	External interrupt 1 input.
	4	I	**P1.5**	**$\overline{\text{RST}}$**	External Reset input (if selected via EPROM configuration). A low on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. When used as a port pin, P1.5 is a Schmitt trigger input only.
P2.0–P2.1	6, 7	I/O	**Port 2**: Port 2 is a 2-bit I/O port with a user-configurable output type. Port 2 latches are configured in the quasi-bidirectional mode and have either ones or zeros written to them during reset, as determined by the PRHI bit in the UCFG1 configuration byte. The operation of port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to the section on I/O port configuration and the DC Electrical Characteristics for details. Port 2 also provides various special functions as described below.		
	7	O	**P2.0**	**X2**	Output from the oscillator amplifier (when a crystal oscillator option is selected via the EPROM configuration).
				CLKOUT	CPU clock divided by 6 clock output when enabled via SFR bit and in conjunction with internal RC oscillator or external clock input.
	6	I	**P2.1**	**X1**	Input to the oscillator circuit and internal clock generator circuits (when selected via the EPROM configuration).
V_{SS}	5	I	**Ground**: 0V reference.		
V_{DD}	15	I	**Power Supply**: This is the power supply voltage for normal operation as well as Idle and Power Down modes.		

SPECIAL FUNCTION REGISTERS

Name	Description	SFR Address	Bit Functions and Addresses MSB							LSB	Reset Value
			E7	E6	E5	E4	E3	E2	E1	E0	
ACC*	Accumulator	E0h									00h
AUXR1#	Auxiliary Function Register	A2h	KBF	BOD	BOI	LPEP	SRST	0	–	DPS	02h[1]
			F7	F6	F5	F4	F3	F2	F1	F0	
B*	B register	F0h									00h
CMP1#	Comparator 1 control register	ACh	–	–	CE1	CP1	CN1	OE1	CO1	CMF1	00h[1]
CMP2#	Comparator 2 control register	ADh	–	–	CE2	CP2	CN2	OE2	CO2	CMF2	00h[1]
DIVM#	CPU clock divide-by-M control	95h									00h
DPTR:	Data pointer (2 bytes)										
DPH	Data pointer high byte	83h									00h
DPL	Data pointer low byte	82h									00h
			CF	CE	CD	CC	CB	CA	C9	C8	
I2CFG#*	I^2C configuration register	C8h/RD	SLAVEN	MASTRQ	0	TIRUN	–	–	CT1	CT0	00h[1]
		C8h/WR	SLAVEN	MASTRQ	CLRTI	TIRUN	–	–	CT1	CT0	
			DF	DE	DD	DC	DB	DA	D9	D8	
I2CON#*	I^2C control register	D8h/RD	RDAT	ATN	DRDY	ARL	STR	STP	MASTER	–	80h[1]
		D8h/WR	CXA	IDLE	CDR	CARL	CSTR	CSTP	XSTR	XSTP	
I2DAT#	I^2C data register	D9h/RD	RDAT	0	0	0	0	0	0	0	80h
		D9h/WR	XDAT	x	x	x	x	x	x	x	
			AF	AE	AD	AC	AB	AA	A9	A8	
IEN0*	Interrupt enable 0	A8h	EA	EWD	EBO	ES	ET1	EX1	ET0	EX0	00h
			EF	EE	ED	EC	EB	EA	E9	E8	
IEN1#*	Interrupt enable 1	E8h	ETI	–	EC1	–	–	EC2	EKB	EI2	00h[1]
			BF	BE	BD	BC	BB	BA	B9	B8	
IP0*	Interrupt priority 0	B8h	–	PWD	PBO	PS	PT1	PX1	PT0	PX0	00h[1]
IP0H#	Interrupt priority 0 high byte	B7h	–	PWDH	PBOH	PSH	PT1H	PX1H	PT0H	PX0H	00h[1]
			FF	FE	FD	FC	FB	FA	F9	F8	
IP1*	Interrupt priority 1	F8h	PTI	–	PC1	–	–	PC2	PKB	PI2	00h[1]
IP1H#	Interrupt priority 1 high byte	F7h	PTIH	–	PC1H	–	–	PC2H	PKBH	PI2H	00h[1]
KBI#	Keyboard Interrupt	86h									00h
			87	86	85	84	83	82	81	80	
P0*	Port 0	80h	T1	CMP1	CMPREF	CIN1A	CIN1B	CIN2A	CIN2B	CMP2	Note 2
			97	96	95	94	93	92	91	90	
P1*	Port 1	90h	(P1.7)	(P1.6)	$\overline{RST}$	$\overline{INT1}$	$\overline{INT0}$	T0	RxD	TxD	Note 2
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0h	–	–	–	–	–	–	X1	X2	Note 2
P0M1#	Port 0 output mode 1	84h	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	00h
P0M2#	Port 0 output mode 2	85h	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00H
P1M1#	Port 1 output mode 1	91h	(P1M1.7)	(P1M1.6)	–	(P1M1.4)	–	–	(P1M1.1)	(P1M1.0)	00h[1]
P1M2#	Port 1 output mode 2	92h	(P1M2.7)	(P1M2.6)	–	(P1M2.4)	–	–	(P1M2.1)	(P1M2.0)	00h[1]
P2M1#	Port 2 output mode 1	A4h	P2S	P1S	P0S	ENCLK	T1OE	T0OE	(P2M1.1)	(P2M1.0)	00h
P2M2#	Port 2 output mode 2	A5h	–	–	–	–	–	–	(P2M2.1)	(P2M2.0)	00h[1]
PCON	Power control register	87h	SMOD1	SMOD0	BOF	POF	GF1	GF0	PD	IDL	Note 3

External Interrupt Inputs

The P87LPC764 has two individual interrupt inputs as well as the Keyboard Interrupt function. The latter is described separately elsewhere in this section. The two interrupt inputs are identical to those present on the standard 80C51 microcontroller.

The external sources can be programmed to be level-activated or transition-activated by setting or clearing bit IT1 or IT0 in Register TCON. If ITn = 0, external interrupt n is triggered by a detected low at the $\overline{INTn}$ pin. If ITn = 1, external interrupt n is edge triggered. In this mode if successive samples of the $\overline{INTn}$ pin show a high in one cycle and a low in the next cycle, interrupt request flag IEn in TCON is set, causing an interrupt request.

Since the external interrupt pins are sampled once each machine cycle, an input high or low should hold for at least 6 CPU Clocks to ensure proper sampling. If the external interrupt is transition-activated, the external source has to hold the request pin high for at least one machine cycle, and then hold it low for at least one machine cycle. This is to ensure that the transition is seen and that interrupt request flag IEn is set. IEn is automatically cleared by the CPU when the service routine is called.

If the external interrupt is level-activated, the external source must hold the request active until the requested interrupt is actually generated. If the external interrupt is still asserted when the interrupt service routine is completed another interrupt will be generated. It is not necessary to clear the interrupt flag IEn when the interrupt is level sensitive, it simply tracks the input pin level.

If an external interrupt is enabled when the P87LPC764 is put into Power Down or Idle mode, the interrupt will cause the processor to wake up and resume operation. Refer to the section on Power Reduction Modes for details.

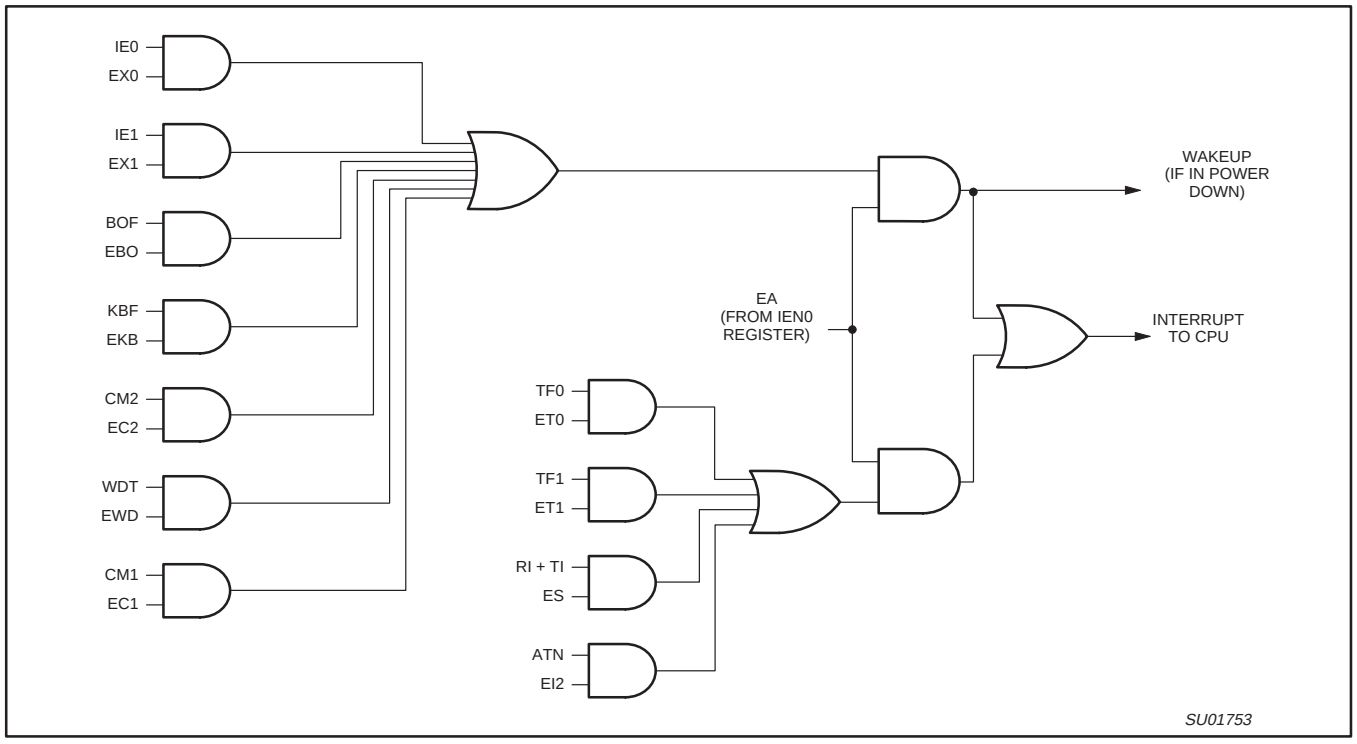


Figure 9. Interrupt Sources, Interrupt Enables, and Power Down Wakeup Sources

I/O Ports

The P87LPC764 has 3 I/O ports, port 0, port 1, and port 2. The exact number of I/O pins available depend upon the oscillator and reset options chosen. At least 15 pins of the P87LPC764 may be used as I/Os when a two-pin external oscillator and an external reset circuit are used. Up to 18 pins may be available if fully on-chip oscillator and reset configurations are chosen.

All but three I/O port pins on the P87LPC764 may be software configured to one of four types on a bit-by-bit basis, as shown in Table 4. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input only. Two configuration registers for each port choose the output type for each port pin.

Table 4. Port Output Configuration Settings

PxM1.y	PxM2.y	Port Output Mode
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance)
1	1	Open Drain

Quasi-Bidirectional Output Configuration

The default port output configuration for standard P87LPC764 I/O ports is the quasi-bidirectional output that is common on the 80C51 and most of its derivatives. This output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin is pulled low, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

One of these pull-ups, called the “very weak” pull-up, is turned on whenever the port latch for the pin contains a logic 1. The very weak pull-up sources a very small current that will pull the pin high if it is left floating.

A second pull-up, called the “weak” pull-up, is turned on when the port latch for the pin contains a logic 1 and the pin itself is also at a logic 1 level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting a 1. If a pin that has a logic 1 on it is pulled low by an external device, the weak pull-up turns off, and only the very weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to overpower the weak pull-up and take the voltage on the port pin below its input threshold.

The third pull-up is referred to as the “strong” pull-up. This pull-up is used to speed up low-to-high transitions on a quasi-bidirectional port pin when the port latch changes from a logic 0 to a logic 1. When this occurs, the strong pull-up turns on for a brief time, two CPU clocks, in order to pull the port pin high quickly. Then it turns off again.

The quasi-bidirectional port configuration is shown in Figure 10.

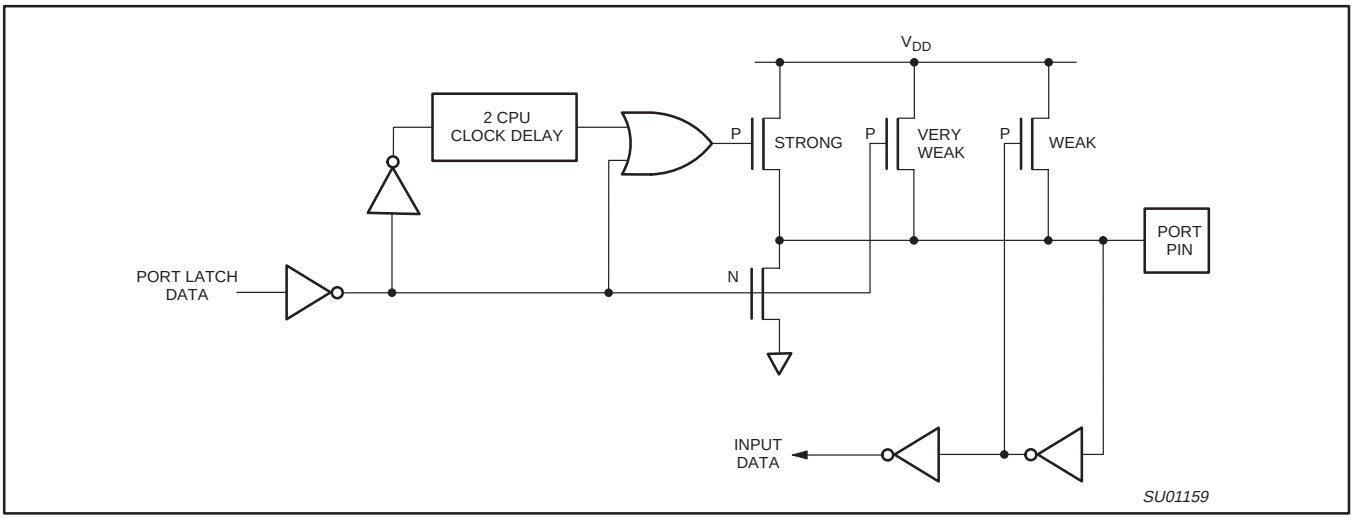


Figure 10. Quasi-Bidirectional Output

P2M1 Address: A4h Reset Value: 00h

Not Bit Addressable

7	6	5	4	3	2	1	0
P2S	P1S	P0S	ENCLK	T1OE	T0OE	(P2M1.1)	(P2M1.0)

BIT	SYMBOL	FUNCTION
P2M1.7	P2S	When P2S = 1, this bit enables Schmitt trigger inputs on Port 2.
P2M1.6	P1S	When P1S = 1, this bit enables Schmitt trigger inputs on Port 1.
P2M1.5	P0S	When P0S = 1, this bit enables Schmitt trigger inputs on Port 0.
P2M1.4	ENCLK	When ENCLK is set and the 87LPC764 is configured to use the on-chip RC oscillator, a clock output is enabled on the X2 pin (P2.0). Refer to the Oscillator section for details.
P2M1.3	T1OE	When set, the P0.7 pin is toggled whenever Timer 1 overflows. The output frequency is therefore one half of the Timer 1 overflow rate. Refer to the Timer/Counters section for details.
P2M1.2	T0OE	When set, the P1.2 pin is toggled whenever Timer 0 overflows. The output frequency is therefore one half of the Timer 0 overflow rate. Refer to the Timer/Counterssection for details.
P2M1.1, P2M1.0	—	These bits, along with the matching bits in the P2M2 register, control the output configuration of P2.1 and P2.0 respectively, as shown in Table 4.

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Figure 13. Port 2 Mode Register 1 (P2M1)

Keyboard Interrupt (KBI)

The Keyboard Interrupt function is intended primarily to allow a single interrupt to be generated when any key is pressed on a keyboard or keypad connected to specific pins of the P87LPC764, as shown in Figure 14. This interrupt may be used to wake up the CPU from Idle or Power Down modes. This feature is particularly useful in handheld, battery powered systems that need to carefully manage power consumption yet also need to be convenient to use.

The P87LPC764 allows any or all pins of port 0 to be enabled to cause this interrupt. Port pins are enabled by the setting of bits in the KBI register, as shown in Figure 15. The Keyboard Interrupt Flag (KBF) in the AUXR1 register is set when any enabled pin is pulled low while the KBI interrupt function is active. An interrupt will generated if it has been enabled. Note that the KBF bit must be cleared by software.

Due to human time scales and the mechanical delay associated with keyswitch closures, the KBI feature will typically allow the interrupt service routine to poll port 0 in order to determine which key was pressed, even if the processor has to wake up from Power Down mode. Refer to the section on Power Reduction Modes for details.

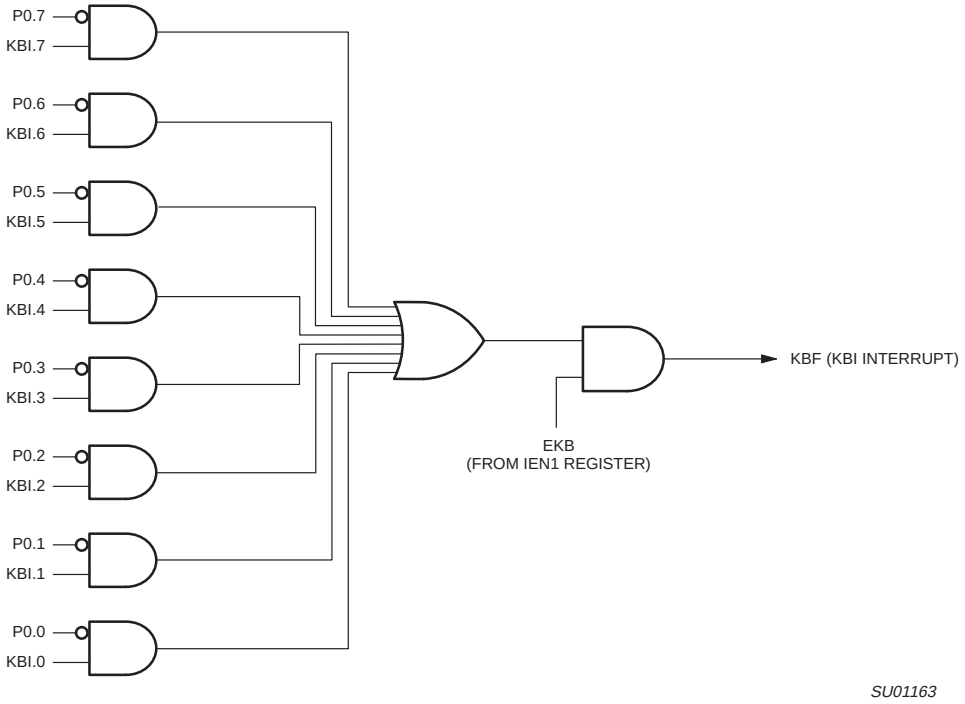

Figure 14. Keyboard Interrupt

KBI Address: 86h Reset Value: 00h

Not Bit Addressable

7	6	5	4	3	2	1	0
KBI.7	KBI.6	KBI.5	KBI.4	KBI.3	KBI.2	KBI.1	KBI.0

BIT	SYMBOL	FUNCTION
KBI.7	KBI.7	When set, enables P0.7 as a cause of a Keyboard Interrupt.
KBI.6	KBI.6	When set, enables P0.6 as a cause of a Keyboard Interrupt.
KBI.5	KBI.5	When set, enables P0.5 as a cause of a Keyboard Interrupt.
KBI.4	KBI.4	When set, enables P0.4 as a cause of a Keyboard Interrupt.
KBI.3	KBI.3	When set, enables P0.3 as a cause of a Keyboard Interrupt.
KBI.2	KBI.2	When set, enables P0.2 as a cause of a Keyboard Interrupt.
KBI.1	KBI.1	When set, enables P0.1 as a cause of a Keyboard Interrupt.
KBI.0	KBI.0	When set, enables P0.0 as a cause of a Keyboard Interrupt.

Note: the Keyboard Interrupt must be enabled in order for the settings of the KBI register to be effective. The interrupt flag (KBF) is located at bit 7 of AUXR1.

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Figure 15. Keyboard Interrupt Register (KBI)

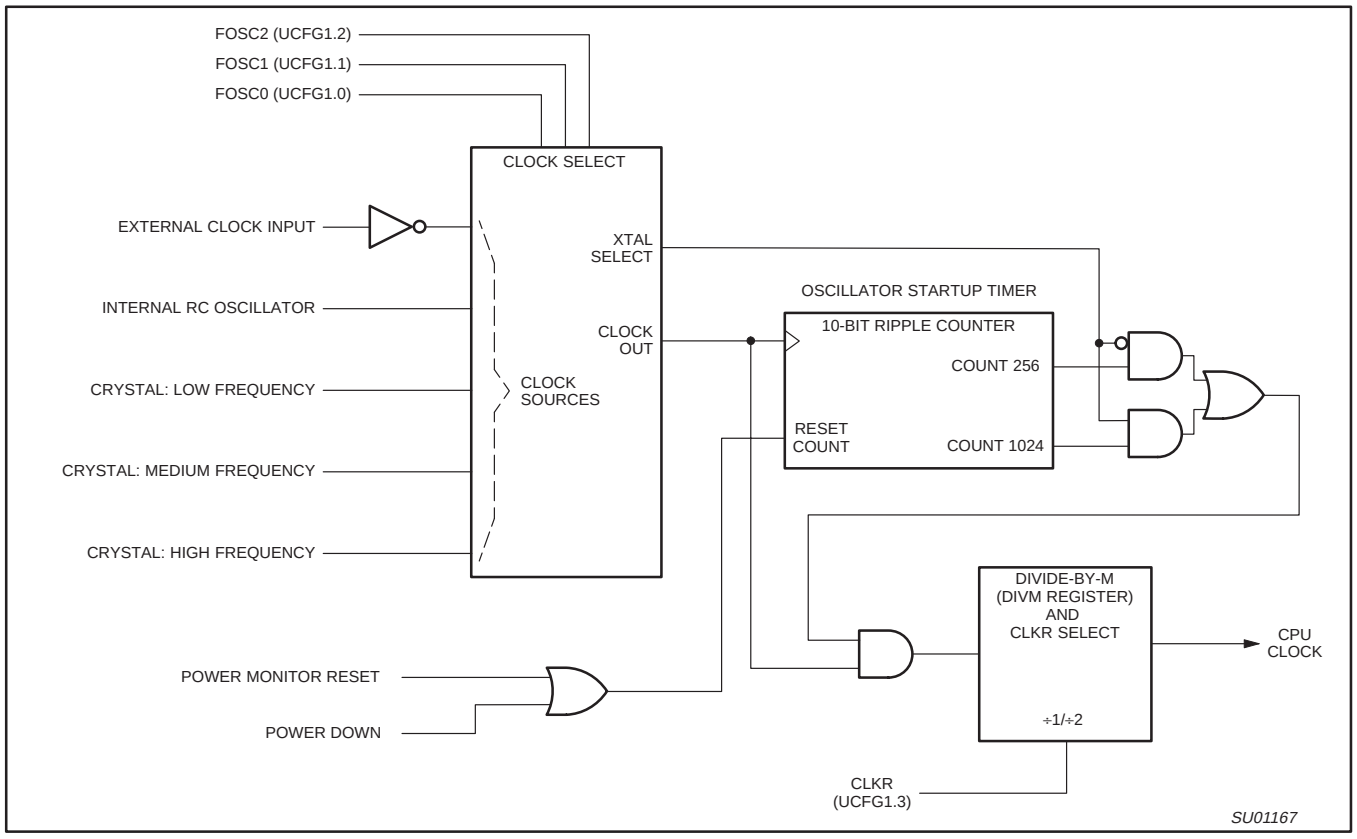


Figure 18. Block Diagram of Oscillator Control

CPU Clock Modification: CLKR and DIVM

For backward compatibility, the CLKR configuration bit allows setting the P87LPC764 instruction and peripheral timing to match standard 80C51 timing by dividing the CPU clock by two. Default timing for the P87LPC764 is 6 CPU clocks per machine cycle while standard 80C51 timing is 12 clocks per machine cycle. This division also applies to peripheral timing, allowing 80C51 code that is oscillator frequency and/or timer rate dependent. The CLKR bit is located in the EPROM configuration register UCFG1, described under EPROM Characteristics

In addition to this, the CPU clock may be divided down from the oscillator rate by a programmable divider, under program control. This function is controlled by the DIVM register. If the DIVM register is set to zero (the default value), the CPU will be clocked by either the unmodified oscillator rate, or that rate divided by two, as determined by the previously described CLKR function.

When the DIVM register is set to some value N (between 1 and 255), the CPU clock is divided by 2 * (N + 1). Clock division values from 4 through 512 are thus possible. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption, in a manner similar to Idle mode. By dividing the clock, the CPU can retain the ability to respond to events other than those that can cause interrupts (i.e. events that allow exiting the Idle mode) by executing its normal program at a lower rate. This can allow bypassing the oscillator startup time in cases where Power Down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

Power Monitoring Functions

The P87LPC764 incorporates power monitoring functions designed to prevent incorrect operation during initial power up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-On Detect and Brownout Detect.

Brownout Detection

The Brownout Detect function allows preventing the processor from failing in an unpredictable manner if the power supply voltage drops below a certain level. The default operation is for a brownout detection to cause a processor reset, however it may alternatively be configured to generate an interrupt by setting the BOI bit in the AUXR1 register (AUXR1.5).

The P87LPC764 allows selection of two Brownout levels: 2.5 V or 3.8 V. When V_{DD} drops below the selected voltage, the brownout detector triggers and remains active until V_{DD} is returns to a level above the Brownout Detect voltage. When Brownout Detect causes a processor reset, that reset remains active as long as V_{DD} remains below the Brownout Detect voltage. When Brownout Detect generates an interrupt, that interrupt occurs once as V_{DD} crosses from above to below the Brownout Detect voltage. For the interrupt to be processed, the interrupt system and the BOI interrupt must both be enabled (via the EA and EBO bits in IEN0).

When Brownout Detect is activated, the BOF flag in the PCON register is set so that the cause of processor reset may be determined by software. This flag will remain set until cleared by software.

Timer/Counters

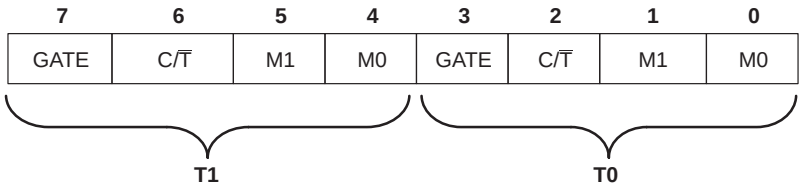
The P87LPC764 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. Both can be configured to operate either as timers or event counters (see Figure 22). An option to automatically toggle the T0 and/or T1 pins upon timer overflow has been added.

In the “Timer” function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of 6 CPU clock periods, the count rate is 1/6 of the CPU clock frequency. Refer to the section Enhanced CPU for a description of the CPU clock.

In the “Counter” function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once during every machine cycle. When the samples of the pin state show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (12 CPU clocks) to recognize a 1-to-0 transition, the maximum count rate is 1/6 of the CPU clock frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

The “Timer” or “Counter” function is selected by control bits C/$\overline{T}$ in the Special Function Register TMOD. In addition to the “Timer” or “Counter” selection, Timer 0 and Timer 1 have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timers/Counters. Mode 3 is different. The four operating modes are described in the following text.

TMOD Address: 89h Reset Value: 00h
Not Bit Addressable



BIT	SYMBOL	FUNCTION
TMOD.7	GATE	Gating control for Timer 1. When set, Timer/Counter is enabled only while the $\overline{INT1}$ pin is high and the TR1 control pin is set. When cleared, Timer 1 is enabled when the TR1 control bit is set.
TMOD.6	C/$\overline{T}$	Timer or Counter Selector for Timer 1. Cleared for Timer operation (input from internal system clock.) Set for Counter operation (input from T1 input pin).
TMOD.5, 4	M1, M0	Mode Select for Timer 1 (see table below).
TMOD.3	GATE	Gating control for Timer 0. When set, Timer/Counter is enabled only while the $\overline{INT0}$ pin is high and the TR0 control pin is set. When cleared, Timer 0 is enabled when the TR0 control bit is set.
TMOD.2	C/$\overline{T}$	Timer or Counter Selector for Timer 0. Cleared for Timer operation (input from internal system clock.) Set for Counter operation (input from T0 input pin).
TMOD.1, 0	M1, M0	Mode Select for Timer 0 (see table below).
	M1, M0	Timer Mode
	0 0	8048 Timer “TLn” serves as 5-bit prescaler.
	0 1	16-bit Timer/Counter “THn” and “TLn” are cascaded; there is no prescaler.
	1 0	8-bit auto-reload Timer/Counter. THn holds a value which is loaded into TLn when it overflows.
	1 1	Timer 0 is a dual 8-bit Timer/Counter in this mode. TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only, controlled by the Timer 1 control bits (see text). Timer 1 in this mode is stopped.

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Figure 22. Timer/Counter Mode Control Register (TMOD)

Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. Figure 24 shows Mode 0 operation.

In this mode, the Timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the Timer interrupt flag TFn. The count input is enabled to the Timer when TRn = 1 and either GATE = 0 or $\overline{INTn}$ = 1. (Setting GATE = 1 allows the Timer to be controlled by external input $\overline{INTn}$, to facilitate pulse width measurements). TRn is a control bit in the Special Function Register TCON (Figure 23). The GATE bit is in the TMOD register.

The 13-bit register consists of all 8 bits of THn and the lower 5 bits of TLn. The upper 3 bits of TLn are indeterminate and should be ignored. Setting the run flag (TRn) does not clear the registers.

Mode 0 operation is the same for Timer 0 and Timer 1. See Figure 24. There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

TCON Address: 88h Reset Value: 00h

Bit Addressable

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

BIT	SYMBOL	FUNCTION
TCON.7	TF1	Timer 1 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when the interrupt is processed, or by software.
TCON.6	TR1	Timer 1 Run control bit. Set/cleared by software to turn Timer/Counter 1 on/off.
TCON.5	TF0	Timer 0 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when the processor vectors to the interrupt routine, or by software.
TCON.4	TR0	Timer 0 Run control bit. Set/cleared by software to turn Timer/Counter 0 on/off.
TCON.3	IE1	Interrupt 1 Edge flag. Set by hardware when external interrupt 1 edge is detected. Cleared by hardware when the interrupt is processed, or by software.
TCON.2	IT1	Interrupt 1 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.
TCON.1	IE0	Interrupt 0 Edge flag. Set by hardware when external interrupt 0 edge is detected. Cleared by hardware when the interrupt is processed, or by software.
TCON.0	IT0	Interrupt 0 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.

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Figure 23. Timer/Counter Control Register (TCON)

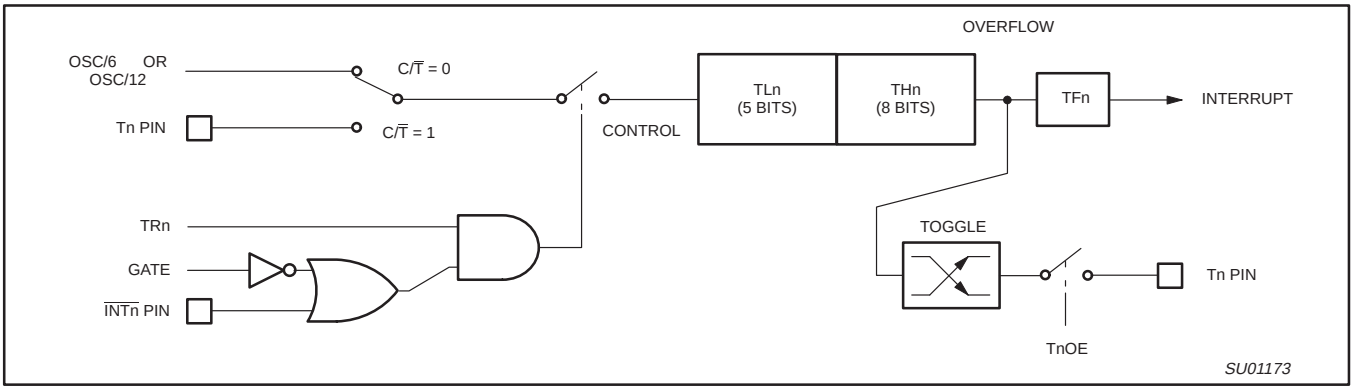

Figure 24. Timer/Counter 0 or 1 in Mode 0 (13-Bit Counter)

Mode 1
Mode 1 is the same as Mode 0, except that all 16 bits of the timer register (THn and TLn) are used. See Figure 25

Mode 2
Mode 2 configures the Timer register as an 8-bit Counter (TL1) with automatic reload, as shown in Figure 26. Overflow from TLn not only sets TFn, but also reloads TLn with the contents of THn, which must be preset by software. The reload leaves THn unchanged. Mode 2 operation is the same for Timer 0 and Timer 1.

Mode 3
When Timer 1 is in Mode 3 it is stopped. The effect is the same as setting TR1 = 0.

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate 8-bit counters. The logic for Mode 3 on Timer 0 is shown in Figure 27. TL0 uses the Timer 0 control bits: C/$\overline{T}$, GATE, TR0 and pin $\overline{INT0}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the “Timer 1” interrupt.

Mode 3 is provided for applications that require an extra 8-bit timer. With Timer 0 in Mode 3, an P87LPC764 can look like it has three Timer/Counters. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it into and out of its own Mode 3. It can still be used by the serial port as a baud rate generator, or in any application not requiring an interrupt.

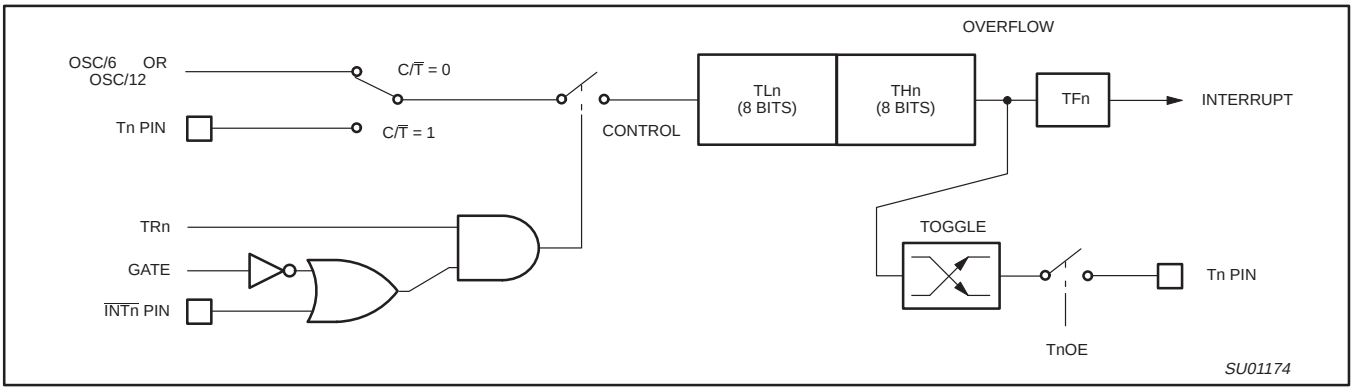

Figure 25. Timer/Counter 0 or 1 in Mode 1 (16-Bit Counter)

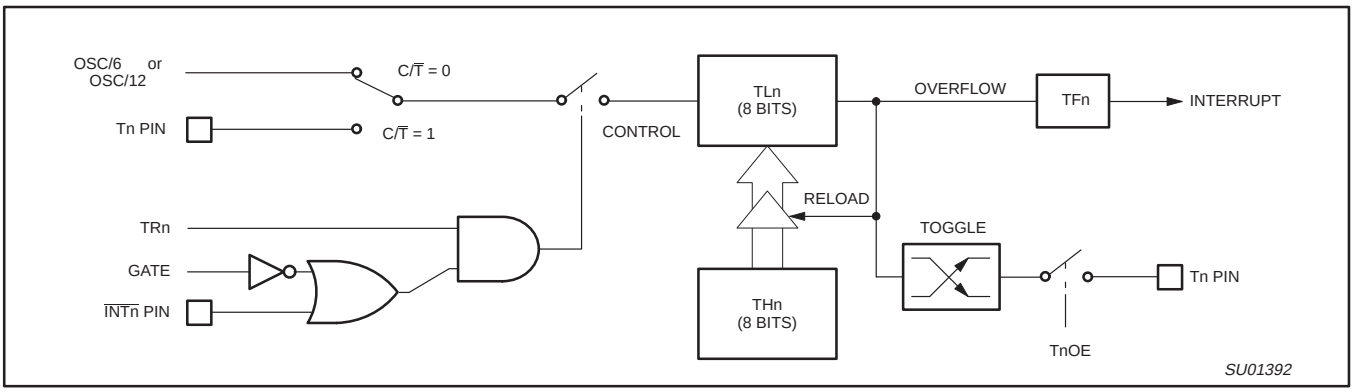

Figure 26. Timer/Counter 0 or 1 in Mode 2 (8-Bit Auto-Reload)

Serial Port Control Register (SCON)
The serial port control and status register is the Special Function Register SCON, shown in Figure 28. This register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

The Framing Error bit (FE) allows detection of missing stop bits in the received data stream. The FE bit shares the bit position SCON.7 with the SM0 bit. Which bit appears in SCON at any particular time is determined by the SMOD0 bit in the PCON register. If SMOD0 = 0, SCON.7 is the SM0 bit. If SMOD0 = 1, SCON.7 is the FE bit. Once set, the FE bit remains set until it is cleared by software. This allows detection of framing errors for a group of characters without the need for monitoring it for every character individually.

SCON Address: 98h Reset Value: 00h

Bit Addressable

7	6	5	4	3	2	1	0
SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

BIT	SYMBOL	FUNCTION
SCON.7	FE	Framing Error. This bit is set by the UART receiver when an invalid stop bit is detected. Must be cleared by software. The SMOD0 bit in the PCON register must be 1 for this bit to be accessible. See SM0 bit below.
SCON.7	SM0	With SM1, defines the serial port mode. The SMOD0 bit in the PCON register must be 0 for this bit to be accessible. See FE bit above.
SCON. 6	SM1	With SM0, defines the serial port mode (see table below).

SM0, SM1	UART Mode	Baud Rate
0 0	0: shift register	CPU clock/6
0 1	1: 8-bit UART	Variable (see text)
1 0	2: 9-bit UART	CPU clock/32 or CPU clock/16
1 1	3: 9-bit UART	Variable (see text)

SCON.5	SM2	Enables the multiprocessor communication feature in Modes 2 and 3. In Mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In Mode 1, if SM2=1 then RI will not be activated if a valid stop bit was not received. In Mode 0, SM2 should be 0.
SCON.4	REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
SCON.3	TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
SCON.2	RB8	In Modes 2 and 3, is the 9th data bit that was received. In Mode 1, it SM2=0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
SCON.1	TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
SCON.0	RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

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Figure 28. Serial Port Control Register (SCON)

Table 10. Baud Rates, Timer Values, and CPU Clock Frequencies for SMOD1 = 1

Timer Count	Baud Rate						
	2400	4800	9600	19.2k	38.4k	57.6k	115.2k
–1	0.2304	0.4608	0.9216	* 1.8432	* 3.6864	5.5296	* 11.0592
–2	0.4608	0.9216	* 1.8432	* 3.6864	* 7.3728	* 11.0592	–
–3	0.6912	1.3824	2.7648	5.5296	* 11.0592	16.5888	–
–4	0.9216	* 1.8432	* 3.6864	* 7.3728	* 14.7456	–	–
–5	1.1520	2.3040	4.6080	9.2160	* 18.4320	–	–
–6	1.3824	2.7648	5.5296	* 11.0592	–	–	–
–7	1.6128	3.2256	6.4512	12.9024	–	–	–
–8	* 1.8432	* 3.6864	* 7.3728	* 14.7456	–	–	–
–9	2.0736	4.1472	8.2944	16.5888	–	–	–
–10	2.3040	4.6080	9.2160	* 18.4320	–	–	–
–11	2.5344	5.0688	10.1376	–	–	–	–
–12	2.7648	5.5296	* 11.0592	–	–	–	–
–13	2.9952	5.9904	11.9808	–	–	–	–
–14	3.2256	6.4512	12.9024	–	–	–	–
–15	3.4560	6.9120	13.8240	–	–	–	–
–16	* 3.6864	* 7.3728	* 14.7456	–	–	–	–
–17	3.9168	7.8336	15.6672	–	–	–	–
–18	4.1472	8.2944	16.5888	–	–	–	–
–19	4.3776	8.7552	17.5104	–	–	–	–
–20	4.6080	9.2160	* 18.4320	–	–	–	–
–21	4.8384	9.6768	19.3536	–	–	–	–

NOTES TO TABLES 9 AND 10:

1. Tables 6 and 7 apply to UART modes 1 and 3 (variable rate modes), and show CPU clock rates in MHz for standard baud rates from 2400 to 115.2k baud.
2. Table 6 shows timer settings and CPU clock rates with the SMOD1 bit in the PCON register = 0 (the default after reset), while Table 7 reflects the SMOD1 bit = 1.
3. The tables show all potential CPU clock frequencies up to 20 MHz that may be used for baud rates from 9600 baud to 115.2k baud. Other CPU clock frequencies that would give only lower baud rates are not shown.
4. Table entries marked with an asterisk (*) indicate standard crystal and ceramic resonator frequencies that may be obtained from many sources without special ordering.

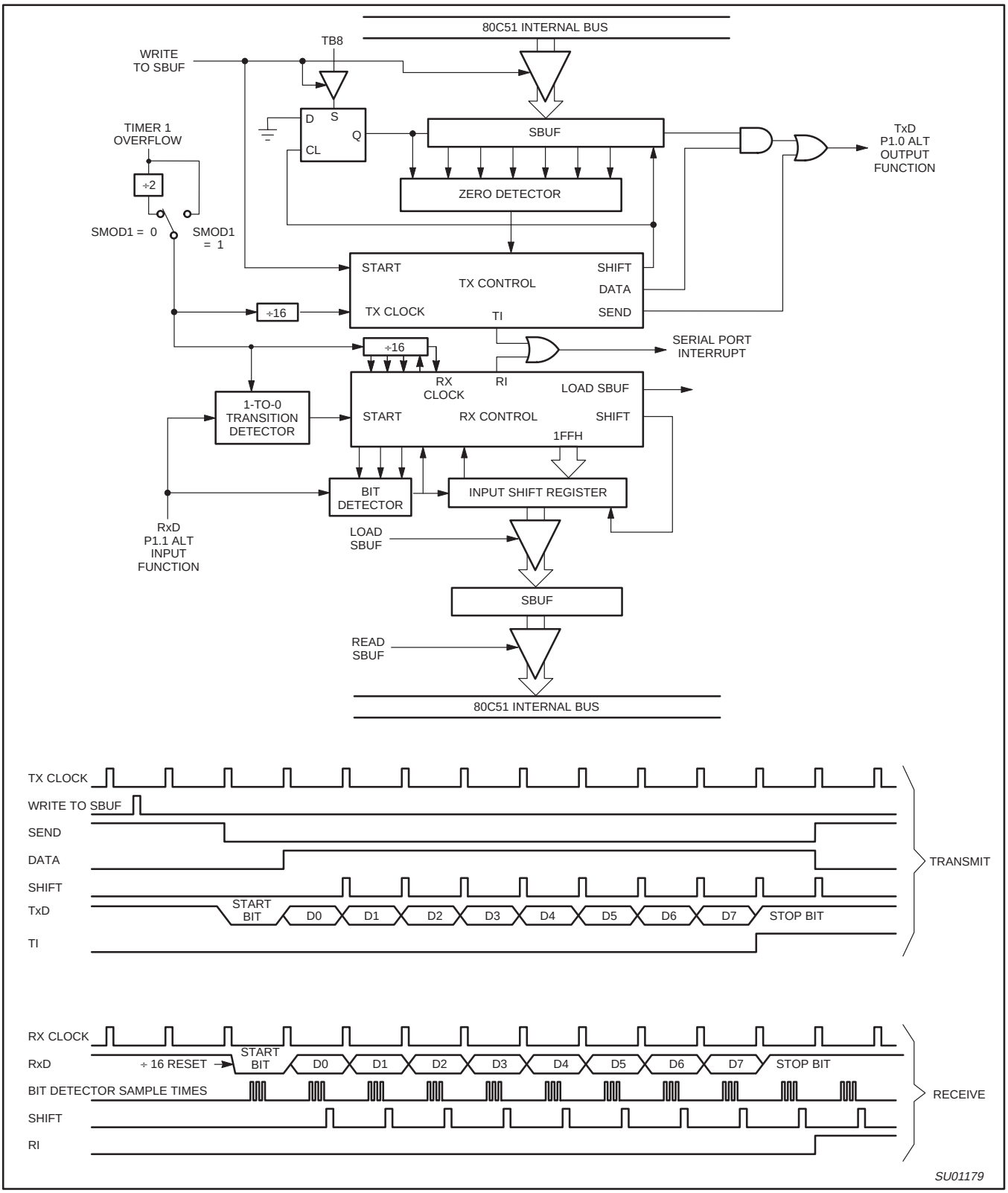

Figure 30. Serial Port Mode 1

More About UART Modes 2 and 3

Eleven bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8) can be assigned the value of 0 or 1. On receive, the 9the data bit goes into RB8 in SCON. The baud rate is programmable to either 1/16 or 1/32 of the CPU clock frequency in Mode 2. Mode 3 may have a variable baud rate generated from Timer 1.

Figures 31 and 32 show a functional diagram of the serial port in Modes 2 and 3. The receive portion is exactly the same as in Mode 1. The transmit portion differs from Mode 1 only in the 9th bit of the transmit shift register.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads TB8 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SBUF” signal.)

The transmission begins with activation of SEND, which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that. The first shift clocks a 1 (the stop bit) into the 9th bit position of the shift register. Thereafter, only zeros are clocked in. Thus, as data bits shift out to the right, zeros are clocked in from the left. When TB8 is at the output position of the shift register, then the stop bit is just to the left of TB8, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 11th divide-by-16 rollover after “write to SBUF.”

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written to the input shift register.

At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of R–D. The value accepted is the value that was seen in at least 2 of the 3 samples. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in Modes 2 and 3 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI.

The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated. 1. RI = 0, and 2. Either SM2 = 0, or the received 9th data bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF. One bit time later, whether the above conditions were met or not, the unit goes back to looking for a 1-to-0 transition at the RxD input.

Multiprocessor Communications

UART modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received or transmitted. When data is received, the 9th bit is stored in RB8. The UART can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. One way to use this feature in multiprocessor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that follow. The slaves that weren’t being addressed leave their SM2 bits set and go on about their business, ignoring the subsequent data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit, although this is better done with the Framing Error flag. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

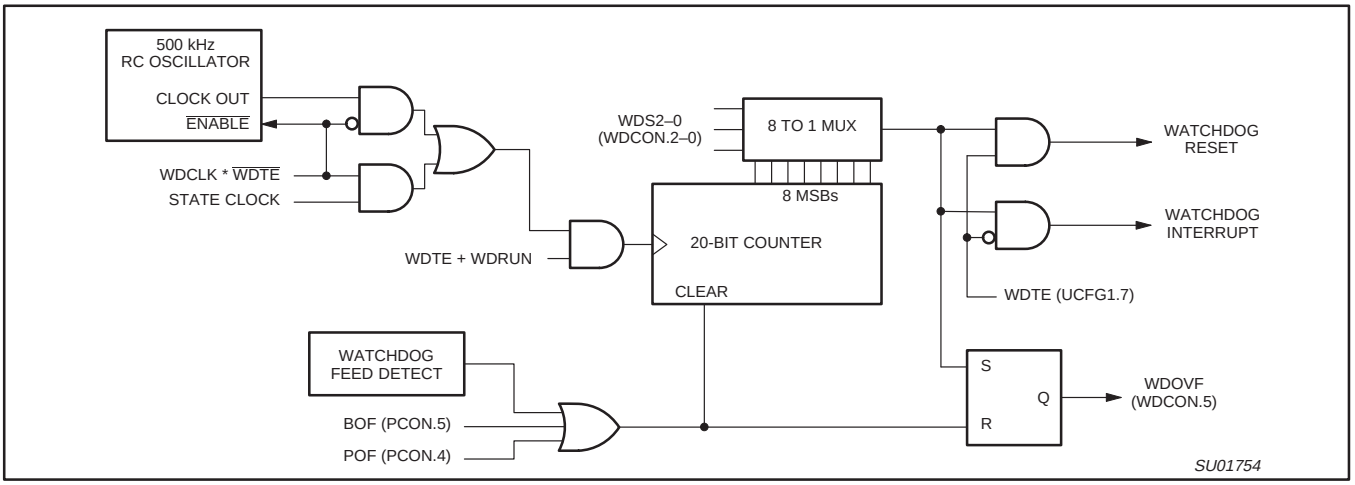

Figure 33. Block Diagram of the Watchdog Timer

WDCON Address: A7h

Not Bit Addressable

Reset Value:
- 30h for a watchdog reset.
- 10h for other rest sources if the watchdog is enabled via the WDTE configuration bit.
- 00h for other reset sources if the watchdog is disabled via the WDTE configuration bit.

7	6	5	4	3	2	1	0
—	—	WDOVF	WDRUN	WDCLK	WDS2	WDS1	WDS0

BIT	SYMBOL	FUNCTION
WDCON.7, 6	—	Reserved for future use. Should not be set to 1 by user programs.
WDCON.5	WDOVF	Watchdog timer overflow flag. Set when a watchdog reset or timer overflow occurs. Cleared when the watchdog is fed.
WDCON.4	WDRUN	Watchdog run control. The watchdog timer is started when WDRUN = 1 and stopped when WDRUN = 0. This bit is forced to 1 (watchdog running) if the WDTE configuration bit = 1.
WDCON.3	WDCLK	Watchdog clock select. The watchdog timer is clocked by CPU clock/6 when WDCLK = 1 and by the watchdog RC oscillator when WDCLK = 0. This bit is forced to 0 (using the watchdog RC oscillator) if the WDTE configuration bit = 1.
WDCON.2–0	WDS2–0	Watchdog rate select.

WDS2–0	Timeout Clocks	Minimum Time	Nominal Time	Maximum Time
0 0 0	8,192	10 ms	25 ms	40 ms
0 0 1	16,384	20 ms	50 ms	80 ms
0 1 0	32,768	41 ms	100 ms	160 ms
0 1 1	65,536	82 ms	200 ms	320 ms
1 0 0	131,072	165 ms	400 ms	640 ms
1 0 1	262,144	330 ms	800 ms	1280 ms
1 1 0	524,288	660 ms	1.60 sec	2.60 sec
1 1 1	1,048,576	1.3 sec	3.20 sec	5.30 sec

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Figure 34. Watchdog Timer Control Register (WDCON)

DC ELECTRICAL CHARACTERISTICS (FOR P87LPC764BD, BN, BDH, FN, FD, FDH, BD/01, BDH/01)

V_{DD} = 2.7 V to 6.0 V unless otherwise specified; T_{amb} = 0°C to +70°C or –40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
I_{DD}	Power supply current, operating	5.0 V, 20 MHz[11]		15	25	mA
		3.0 V, 10 MHz[11]		4	7	mA
I_{ID}	Power supply current, Idle mode	5.0 V, 20 MHz[11]		6	10	mA
		3.0 V, 10 MHz[11]		2	4	mA
I_{PD}	Power supply current, Power Down mode	5.0 V[11]		1	10	µA
		3.0 V[11]		1	5	µA
V_{RAM}	RAM keep-alive voltage		1.5			V
V_{IL}	Input low voltage (TTL input)	4.0 V < V_{DD} < 6.0 V	–0.5		0.2 V_{DD}–0.1	V
		2.7 V < V_{DD} < 4.0 V	–0.5		0.7	V
V_{IL1}	Negative going threshold (Schmitt input)		–0.5		0.3 V_{DD}	V
V_{IH}	Input high voltage (TTL input)		0.2 V_{DD}+0.9		V_{DD}+0.5	V
V_{IH1}	Positive going threshold (Schmitt input)		0.7 V_{DD}		V_{DD}+0.5	V
HYS	Hysteresis voltage			0.2 V_{DD}		V
V_{OL}	Output low voltage all ports[5, 9]	I_{OL} = 3.2 mA, V_{DD} = 2.7 V			0.4	V
V_{OL1}	Output low voltage all ports[5, 9]	I_{OL} = 20 mA, V_{DD} = 2.7 V			1.0	V
V_{OH}	Output high voltage, all ports[3]	I_{OH} = –20 µA, V_{DD} = 2.7 V	V_{DD}–0.7			V
		I_{OH} = –30 µA, V_{DD} = 4.5 V	V_{DD}–0.7			V
V_{OH1}	Output high voltage, all ports[4]	I_{OH} = –1.0 mA, V_{DD} = 2.7 V	V_{DD}–0.7			V
C_{IO}	Input/Output pin capacitance[10]				15	pF
I_{IL}	Logical 0 input current, all ports[8]	V_{IN} = 0.4 V			–50	µA
I_{LI}	Input leakage current, all ports[7]	V_{IN} = V_{IL} or V_{IH}			±2	µA
I_{TL}	Logical 1 to 0 transition current, all ports[3, 6]	V_{IN} = 1.5 V at V_{DD} = 3.0 V	–30		–250	µA
		V_{IN} = 2.0 V at V_{DD} = 5.5 V	–150		–650	µA
R_{RST}	Internal reset pull-up resistor[14]		40		225	kΩ
V_{BOLOW}	Brownout trip voltage with BOV = 1[12]		2.35		2.69	V
V_{BOHI}	Brownout trip voltage with BOV = 0		3.45		3.99	V
V_{REF}	Reference voltage		1.11	1.26	1.41	V
t_C (V_{REF})	Temperature coefficient			tbd		ppm/°C
SS	Supply sensitivity			tbd		%/V

NOTES:

1. Typical ratings are not guaranteed. The values listed are at room temperature, 5 V.
2. See other Figures for details.
   Active mode: $I_{CC(MAX)}$ = tbd
   Idle mode: $I_{CC(MAX)}$ = tbd
3. Ports in quasi-bidirectional mode with weak pull-up (applies to all port pins with pull-ups). Does not apply to open drain pins.
4. Ports in PUSH-PULL mode. Does not apply to open drain pins.
5. In all output modes except high impedance mode.
6. Port pins source a transition current when used in quasi-bidirectional mode and externally driven from 1 to 0. This current is highest when V_{IN} is approximately 2 V.
7. Measured with port in high impedance mode. Parameter is guaranteed but not tested at cold temperature.
8. Measured with port in quasi-bidirectional mode.
9. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 20 mA
   Maximum total I_{OL} for all outputs: 80 mA
   Maximum total I_{OH} for all outputs: 5 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
10. Pin capacitance is characterized but not tested.
11. The I_{DD}, I_{ID}, and I_{PD} specifications are measured using an external clock with the following functions disabled: comparators, brownout detect, and watchdog timer. For V_{DD} = 3 V, LPEP = 1. Refer to the appropriate figures on the following pages for additional current drawn by each of these functions and detailed graphs for other frequency and voltage combinations.
12. Devices initially operating at V_{DD} = 2.7V or above and at f_{OSC} = 10 MHz or less are guaranteed to continue to execute instructions correctly at the brownout trip point. Initial power-on operation below V_{DD} = 2.7 V is not guaranteed.
13. Devices initially operating at V_{DD} = 4.0 V or above and at f_{OSC} = 20 MHz or less are guaranteed to continue to execute instructions correctly at the brownout trip point. Initial power-on operation below V_{DD} = 4.0 V and F_{OSC} > 10 MHz is not guaranteed.
14. This internal resistor is disconnected if P1.5 is used as a general purpose input pin instead of the reset pin.

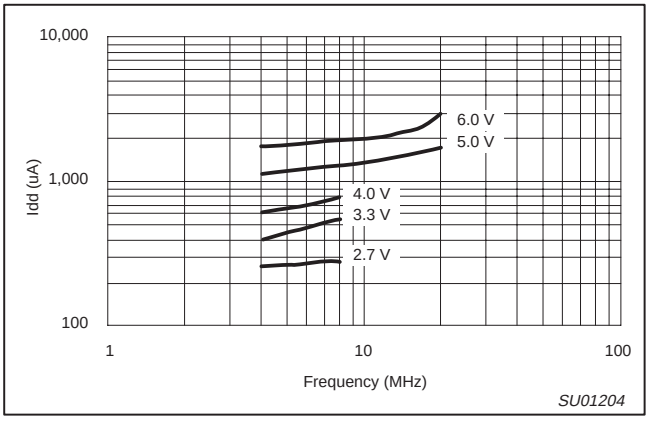

Figure 42. Typical Idd versus frequency (high frequency oscillator, 25°C)

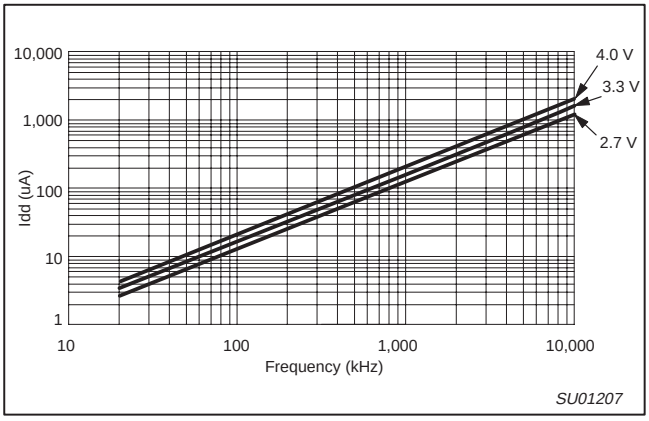

Figure 45. Typical Idle Idd versus frequency (external clock, 25°C, LPEP=1)

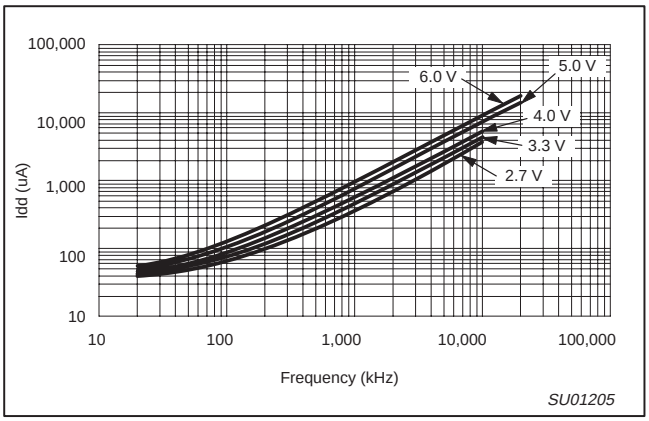

Figure 43. Typical Active Idd versus frequency (external clock, 25°C, LPEP=0)

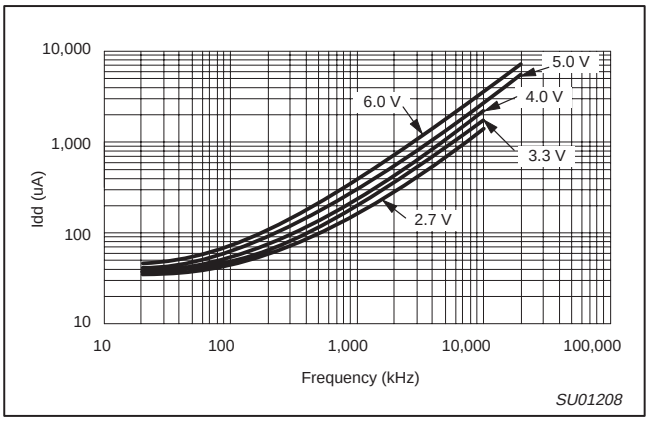

Figure 46. Typical Idle Idd versus frequency (external clock, 25°C, LPEP=0)

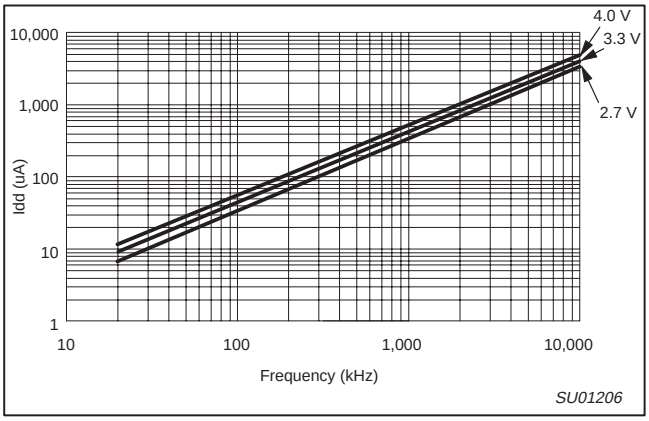

Figure 44. Typical Active Idd versus frequency (external clock, 25°C, LPEP=1)