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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p87lpc764bdh-518

Internal Reference Voltage
An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as V_{ref}, is 1.28 V ±10%.

Comparator Interrupt
Each comparator has an interrupt flag CMFn contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The interrupt will be generated when the corresponding enable bit ECn in the IEN1 register is set and the interrupt system is enabled via the EA bit in the IEN0 register.

Comparators and Power Reduction Modes
Either or both comparators may remain enabled when Power Down or Idle mode is activated. The comparators will continue to function in the power reduction mode. If a comparator interrupt is enabled, a change of the comparator output state will generate an interrupt and wake up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in power down mode. The reason is that with the oscillator stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power Down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue.

Comparator Configuration Example
The code shown in Figure 5 is an example of initializing one comparator. Comparator 1 is configured to use the CIN1A and CMPREF inputs, outputs the comparator result to the CMP1 pin, and generates an interrupt when the comparator output changes.

The interrupt routine used for the comparator must clear the interrupt flag (CMF1 in this case) before returning.

```
CmpInit:
    mov     PT0AD,#30h      ; Disable digital inputs on pins that are used
                            ;   for analog functions: CIN1A, CMPREF.
    anl     P0M2,#0cfh      ; Disable digital outputs on pins that are used
    orl     P0M1,#30h       ;   for analog functions: CIN1A, CMPREF.
    mov     CMP1,#24h       ; Turn on comparator 1 and set up for:
                            ;   – Positive input on CIN1A.
                            ;   – Negative input from CMPREF pin.
                            ;   – Output to CMP1 pin enabled.
    call    delay10us       ; The comparator has to start up for at
                            ;   least 10 microseconds before use.
    anl     CMP1,#0feh      ; Clear comparator 1 interrupt flag.
    setb    EC1             ; Enable the comparator 1 interrupt. The
                            ;   priority is left at the current value.
    setb    EA              ; Enable the interrupt system (if needed).
    ret                     ; Return to caller.
```

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Figure 5.

I2CON Address: D8h Reset Value: 81h

Bit Addressable[1]

	7	6	5	4	3	2	1	0
READ	RDAT	ATN	DRDY	ARL	STR	STP	MASTER	—
WRITE	CXA	IDLE	CDR	CARL	CSTR	CSTP	XSTR	XSTP

BIT	SYMBOL	FUNCTION
I2CON.7	RDAT	Read: the most recently received data bit.
"	CXA	Write: clears the transmit active flag.
I2CON.6	ATN	Read: ATN = 1 if any of the flags DRDY, ARL, STR, or STP = 1.
"	IDLE	Write: in the I^2C slave mode, writing a 1 to this bit causes the I^2C hardware to ignore the bus until it is needed again.
I2CON.5	DRDY	Read: Data Ready flag, set when there is a rising edge on SCL.
"	CDR	Write: writing a 1 to this bit clears the DRDY flag.
I2CON.4	ARL	Read: Arbitration Loss flag, set when arbitration is lost while in the transmit mode.
"	CARL	Write: writing a 1 to this bit clears the CARL flag.
I2CON.3	STR	Read: Start flag, set when a start condition is detected at a master or non-idle slave.
"	CSTR	Write: writing a 1 to this bit clears the STR flag.
I2CON.2	STP	Read: Stop flag, set when a stop condition is detected at a master or non-idle slave.
"	CSTP	Write: writing a 1 to this bit clears the STP flag.
I2CON.1	MASTER	Read: indicates whether this device is currently as bus master.
"	XSTR	Write: writing a 1 to this bit causes a repeated start condition to be generated.
I2CON.0	—	Read: undefined.
"	XSTP	Write: writing a 1 to this bit causes a stop condition to be generated.

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Figure 6. I^2C Control Register (I2CON)

I2DAT Address: D9h Reset Value: xxh

Not Bit Addressable

	7	6	5	4	3	2	1	0
READ	RDAT	—	—	—	—	—	—	—
WRITE	XDAT	—	—	—	—	—	—	—

BIT	SYMBOL	FUNCTION
I2DAT.7	RDAT	Read: the most recently received data bit, captured from SDA at every rising edge of SCL. Reading I2DAT also clears DRDY and the Transmit Active state.
"	XDAT	Write: sets the data for the next transmitted bit. Writing I2DAT also clears DRDY and sets the Transmit Active state.
I2DAT.6–0	–	Unused.

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Figure 7. I^2C Data Register (I2DAT)

Checking ATN and DRDY

When a program detects ATN = 1, it should next check DRDY. If DRDY = 1, then if it receives the last bit, it should capture the data from RDAT (in I2DAT or I2CON). Next, if the next bit is to be sent, it should be written to I2DAT. One way or another, it should clear DRDY and then return to monitoring ATN. Note that if any of ARL, STR, or STP is set, clearing DRDY will not release SCL to high, so that the I^2C will not go on to the next bit. If a program detects ATN = 1, and DRDY = 0, it should go on to examine ARL, STR, and STP.

I2CFG Address: C8h Reset Value: 00h

Bit Addressable

7	6	5	4	3	2	1	0
SLAVEN	MASTRQ	CLRTI	TIRUN	—	—	CT1	CT0

BIT	SYMBOL	FUNCTION
I2CFG.7	SLAVEN	Slave Enable. Writing a 1 this bit enables the slave functions of the I^2C subsystem. If SLAVEN and MASTRQ are 0, the I^2C hardware is disabled. This bit is cleared to 0 by reset and by an I^2C time-out.
I2CFG.6	MASTRQ	Master Request. Writing a 1 to this bit requests mastership of the I^2C bus. If a transmission is in progress when this bit is changed from 0 to 1, action is delayed until a stop condition is detected. A start condition is sent and DRDY is set (thus making ATN = 1 and generating an I^2C interrupt). When a master wishes to release mastership status of the I^2C, it writes a 1 to XSTP in I2CON. MASTRQ is cleared by an I^2C time-out.
I2CFG.5	CLRTI	Writing a 1 to this bit clears the Timer I overflow flag. This bit position always reads as a 0.
I2CFG.4	TIRUN	Writing a 1 to this bit lets Timer I run; a zero stops and clears it. Together with SLAVEN, MASTRQ, and MASTER, this bit determines operational modes as shown in Table 1.
I2CFG.2, 3	—	Reserved for future use. Should not be set to 1 by user programs.
I2CFG.1, 0	CT1, CT0	These two bits are programmed as a function of the CPU clock rate, to optimize the MIN HI and LO time of SCL when this device is a master on the I^2C. The time value determined by these bits controls both of these parameters, and also the timing for stop and start conditions.

SU01474

Figure 8. I^2C Configuration Register (I2CFG)

Regarding Software Response Time

Because the P87LPC764 can run at 20 MHz, and because the I^2C interface is optimized for high-speed operation, it is quite likely that an I^2C service routine will sometimes respond to DRDY (which is set at a rising edge of SCL) and write I2DAT before SCL has gone low again. If XDAT were applied directly to SDA, this situation would produce an I^2C protocol violation. The programmer need not worry about this possibility because XDAT is applied to SDA only when SCL is low.

Conversely, a program that includes an I^2C service routine may take a long time to respond to DRDY. Typically, an I^2C routine operates on a flag-polling basis during a message, with interrupts from other peripheral functions enabled. If an interrupt occurs, it will delay the response of the I^2C service routine. The programmer need not worry about this very much either, because the I^2C hardware stretches the SCL low time until the service routine responds. The only constraint on the response is that it must not exceed the Timer I time-out.

Values to be used in the CT1 and CT0 bits are shown in Table 2. To allow the I^2C bus to run at the maximum rate for a particular oscillator frequency, compare the actual oscillator rate to the f OSC max column in the table. The value for CT1 and CT0 is found in the first line of the table where CPU clock max is greater than or equal to the actual frequency.

Table 2 also shows the machine cycle count for various settings of CT1/CT0. This allows calculation of the actual minimum high and low times for SCL as follows:

$$\text{SCL min high/low time (in microseconds)} = \frac{6 * \text{Min Time Count}}{\text{CPU clock (in MHz)}}$$

For instance, at an 8 MHz frequency, with CT1/CT0 set to 1 0, the minimum SCL high and low times will be 5.25 μs.

Table 2 also shows the Timer I timeout period (given in machine cycles) for each CT1/CT0 combination. The timeout period varies because of the way in which minimum SCL high and low times are measured. When the I^2C interface is operating, Timer I is pre-loaded at every SCL transition with a value dependent upon CT1/CT0. The pre-load value is chosen such that a minimum SCL high or low time has elapsed when Timer I reaches a count of 008 (the actual value pre-loaded into Timer I is 8 minus the machine cycle count).

External Interrupt Inputs

The P87LPC764 has two individual interrupt inputs as well as the Keyboard Interrupt function. The latter is described separately elsewhere in this section. The two interrupt inputs are identical to those present on the standard 80C51 microcontroller.

The external sources can be programmed to be level-activated or transition-activated by setting or clearing bit IT1 or IT0 in Register TCON. If ITn = 0, external interrupt n is triggered by a detected low at the $\overline{INTn}$ pin. If ITn = 1, external interrupt n is edge triggered. In this mode if successive samples of the $\overline{INTn}$ pin show a high in one cycle and a low in the next cycle, interrupt request flag IEn in TCON is set, causing an interrupt request.

Since the external interrupt pins are sampled once each machine cycle, an input high or low should hold for at least 6 CPU Clocks to ensure proper sampling. If the external interrupt is transition-activated, the external source has to hold the request pin high for at least one machine cycle, and then hold it low for at least one machine cycle. This is to ensure that the transition is seen and that interrupt request flag IEn is set. IEn is automatically cleared by the CPU when the service routine is called.

If the external interrupt is level-activated, the external source must hold the request active until the requested interrupt is actually generated. If the external interrupt is still asserted when the interrupt service routine is completed another interrupt will be generated. It is not necessary to clear the interrupt flag IEn when the interrupt is level sensitive, it simply tracks the input pin level.

If an external interrupt is enabled when the P87LPC764 is put into Power Down or Idle mode, the interrupt will cause the processor to wake up and resume operation. Refer to the section on Power Reduction Modes for details.

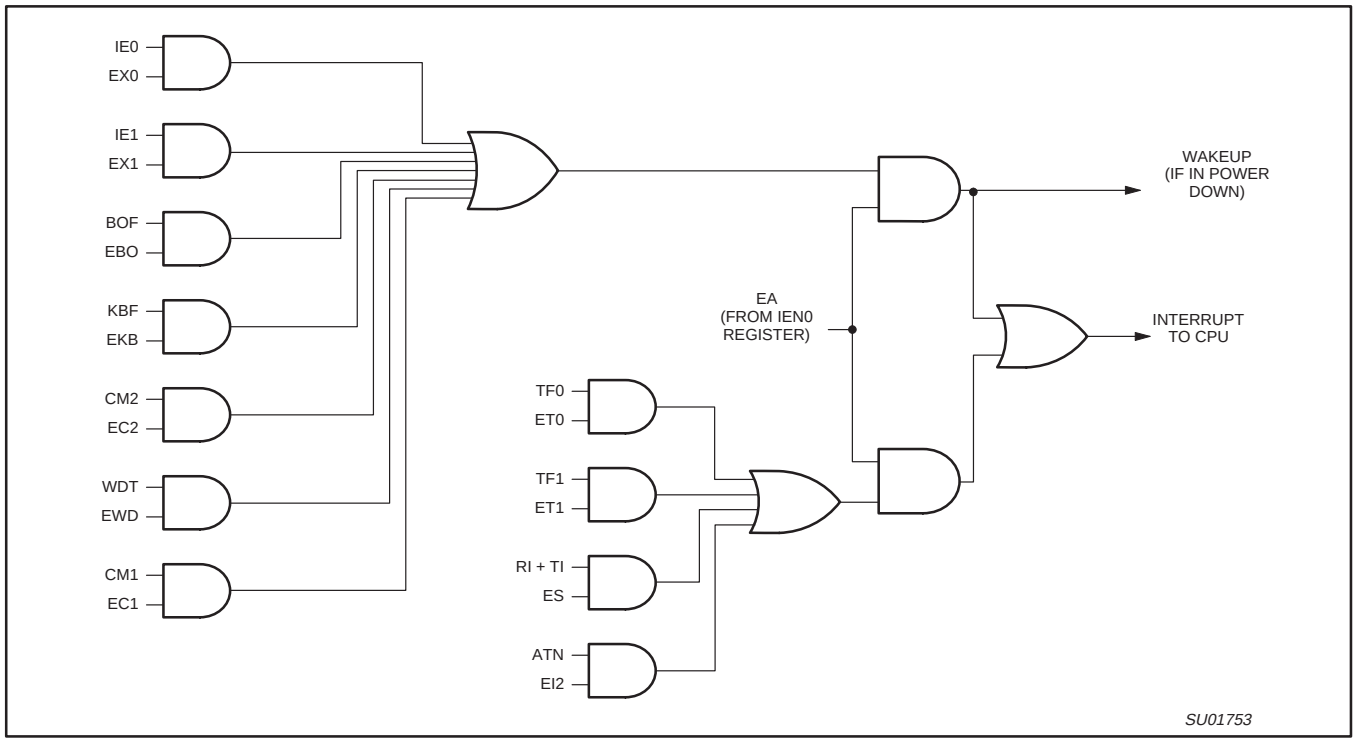


Figure 9. Interrupt Sources, Interrupt Enables, and Power Down Wakeup Sources

Open Drain Output Configuration

The open drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}. The pull-down for this mode is the same as for the quasi-bidirectional mode.

The open drain port configuration is shown in Figure 11.

Push-Pull Output Configuration

The push-pull output configuration has the same pull-down structure as both the open drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output.

The push-pull port configuration is shown in Figure 12.

The three port pins that cannot be configured are P1.2, P1.3, and P1.5. The port pins P1.2 and P1.3 are permanently configured as open drain outputs. They may be used as inputs by writing ones to their respective port latches. P1.5 may be used as a Schmitt trigger input if the P87LPC764 has been configured for an internal reset and is not using the external reset input function $\overline{RST}$.

Additionally, port pins P2.0 and P2.1 are disabled for both input and output if one of the crystal oscillator options is chosen. Those options are described in the Oscillator section.

The value of port pins at reset is determined by the PRHI bit in the UCFG1 register. Ports may be configured to reset high or low as needed for the application. When port pins are driven high at reset, they are in quasi-bidirectional mode and therefore do not source large amounts of current.

Every output on the P87LPC764 may potentially be used as a 20 mA sink LED drive output. However, there is a maximum total output current for all ports which must not be exceeded.

All ports pins of the P87LPC764 have slew rate controlled outputs. This is to limit noise generated by quickly switching output signals. The slew rate is factory set to approximately 10 ns rise and fall times.

The bits in the P2M1 register that are not used to control configuration of P2.1 and P2.0 are used for other purposes. These bits can enable Schmitt trigger inputs on each I/O port, enable toggle outputs from Timer 0 and Timer 1, and enable a clock output if either the internal RC oscillator or external clock input is being used. The last two functions are described in the Timer/Counters and Oscillator sections respectively. The enable bits for all of these functions are shown in Figure 13.

Each I/O port of the P87LPC764 may be selected to use TTL level inputs or Schmitt inputs with hysteresis. A single configuration bit determines this selection for the entire port. Port pins P1.2, P1.3, and P1.5 always have a Schmitt trigger input.

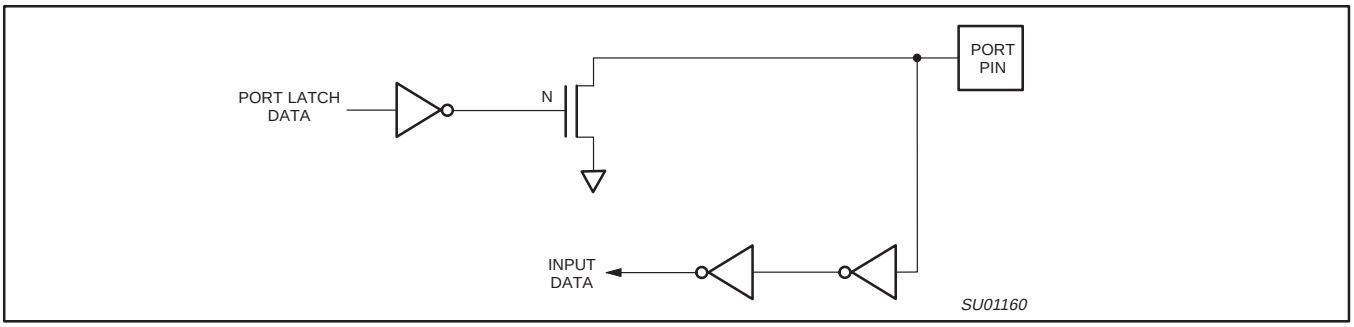


Figure 11. Open Drain Output

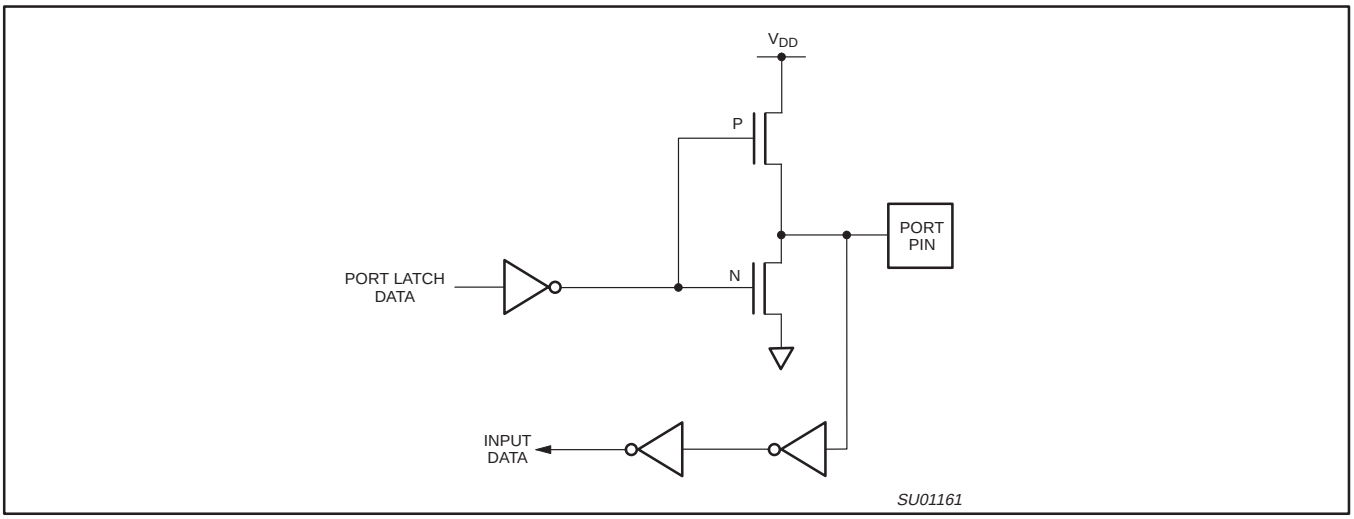


Figure 12. Push-Pull Output

Oscillator

The P87LPC764 provides several user selectable oscillator options, allowing optimization for a range of needs from high precision to lowest possible cost. These are configured when the EPROM is programmed. Basic oscillator types that are supported include: low, medium, and high speed crystals, covering a range from 20 kHz to 20 MHz; ceramic resonators; and on-chip RC oscillator.

Low Frequency Oscillator Option

This option supports an external crystal in the range of 20 kHz to 100 kHz.

Table 5 shows capacitor values that may be used with a quartz crystal in this mode.

Table 5. Recommended oscillator capacitors for use with the low frequency oscillator option

Oscillator Frequency	V_{DD} = 2.7 to 4.5 V			V_{DD} = 4.5 to 6.0 V		
	Lower Limit	Optimal Value	Upper Limit	Lower Limit	Optimal Value	Upper Limit
20 kHz	15 pF	15 pF	33 pF	33 pF	33 pF	47 pF
32 kHz	15 pF	15 pF	33 pF	33 pF	33 pF	47 pF
100 kHz	15 pF	15 pF	33 pF	15 pF	15 pF	33 pF

Medium Frequency Oscillator Option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

Table 6 shows capacitor values that may be used with a quartz crystal in this mode.

Table 6. Recommended oscillator capacitors for use with the medium frequency oscillator option

Oscillator Frequency	V_{DD} = 2.7 to 4.5 V			V_{DD} = 4.5 to 6.0 V		
	Lower Limit	Optimal Value	Upper Limit	Lower Limit	Optimal Value	Upper Limit
100 kHz	33 pF	33 pF	47 pF	33 pF	33 pF	47 pF
1 MHz	15 pF	15 pF	33 pF	15 pF	22 pF	47 pF
4 MHz	15 pF	15 pF	33 pF	15 pF	15 pF	33 pF

High Frequency Oscillator Option

This option supports an external crystal in the range of 4 to 20 MHz. Ceramic resonators are also supported in this configuration.

Table 7 shows capacitor values that may be used with a quartz crystal in this mode.

Table 7. Recommended oscillator capacitors for use with the high frequency oscillator option

Oscillator Frequency	V_{DD} = 2.7 to 4.5 V			V_{DD} = 4.5 to 6.0 V		
	Lower Limit	Optimal Value	Upper Limit	Lower Limit	Optimal Value	Upper Limit
4 MHz	15 pF	33 pF	47 pF	15 pF	33 pF	68 pF
8 MHz	15 pF	15 pF	33 pF	15 pF	33 pF	47 pF
16 MHz	–	–	–	15 pF	15 pF	33 pF
20 MHz	–	–	–	15 pF	15 pF	33 pF

On-Chip RC Oscillator Option

The on-chip RC oscillator option has a typical frequency of 6 MHz and can be divided down for slower operation through the use of the DIVM register. For on-chip oscillator tolerance see AC Electrical Characteristics table. A clock output on the X2/P2.0 pin may be enabled when the on-chip RC oscillator is used.

External Clock Input Option

In this configuration, the processor clock is input from an external source driving the X1/P2.1 pin. The rate may be from 0 Hz up to 20 MHz when V_{DD} is above 4.5 V and up to 10 MHz when V_{DD} is below 4.5 V. When the external clock input mode is used, the X2/P2.0 pin may be used as a standard port pin. A clock output on the X2/P2.0 pin may be enabled when the external clock input is used.

Clock Output

The P87LPC764 supports a clock output function when either the on-chip RC oscillator or external clock input options are selected. This allows external devices to synchronize to the P87LPC764. When enabled, via the ENCLK bit in the P2M1 register, the clock output appears on the X2/CLKOUT pin whenever the on-chip oscillator is running, including in Idle mode. The frequency of the clock output is 1/6 of the CPU clock rate. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power. The clock output may also be enabled when the external clock input option is selected.

Table 8. Sources of Wakeup from Power Down Mode

Wakeup Source	Conditions
External Interrupt 0 or 1	The corresponding interrupt must be enabled.
Keyboard Interrupt	The keyboard interrupt feature must be enabled and properly set up. The corresponding interrupt must be enabled.
Comparator 1 or 2	The comparator(s) must be enabled and properly set up. The corresponding interrupt must be enabled.
Watchdog Timer Reset	The watchdog timer must be enabled via the WDTE bit in the UCFG1 EPROM configuration byte.
Watchdog Timer Interrupt	The WDTE bit in the UCFG1 EPROM configuration byte must not be set. The corresponding interrupt must be enabled.
Brownout Detect Reset	The BOD bit in AUXR1 must not be set (brownout detect not disabled). The BOI bit in AUXR1 must not be set (brownout interrupt disabled).
Brownout Detect Interrupt	The BOD bit in AUXR1 must not be set (brownout detect not disabled). The BOI bit in AUXR1 must be set (brownout interrupt enabled). The corresponding interrupt must be enabled.
Reset Input	The external reset input must be enabled.

Low Voltage EPROM Operation
The EPROM array contains some analog circuits that are not required when V_{DD} is less than 4 V, but are required for a V_{DD} greater than 4 V. The LPEP bit (AUXR.4), when set by software, will power down these analog circuits resulting in a reduced supply current. LPEP is cleared only by power-on reset, so it may be set ONLY for applications that always operate with V_{DD} less than 4 V.

Reset

The P87LPC764 has an integrated power-on reset circuit which always provides a reset when power is initially applied to the device. It is recommended to use the internal reset whenever possible to save external components and to be able to use pin P1.5 as a general-purpose input pin.

The P87LPC764 can additionally be configured to use P1.5 as an external active-low reset pin $\overline{RST}$ by programming the RPD bit in the User Configuration Register UCFG1 to 0. The internal reset is still active on power-up of the device. While the signal on the $\overline{RST}$ pin is low, the P87LPC764 is held in reset until the signal goes high.

The watchdog timer on the LPC764 can act as an oscillator fail detect because it uses an independent, fully on-chip oscillator.

UCFG1 is described in the System Configuration Bytes section of this datasheet.

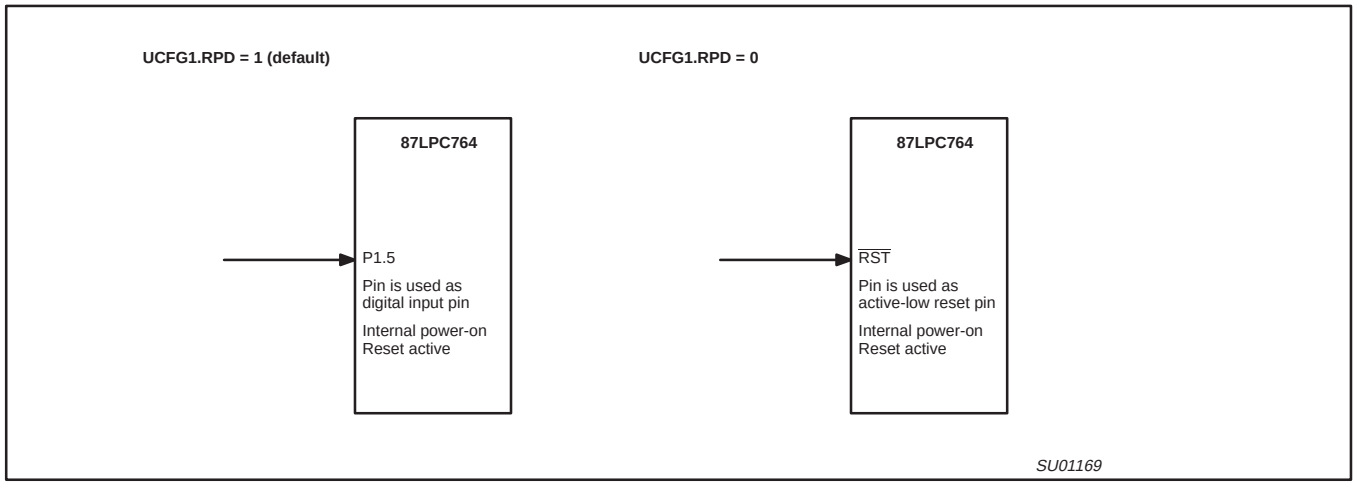


Figure 20. Using pin P1.5 as general purpose input pin or as low-active reset pin

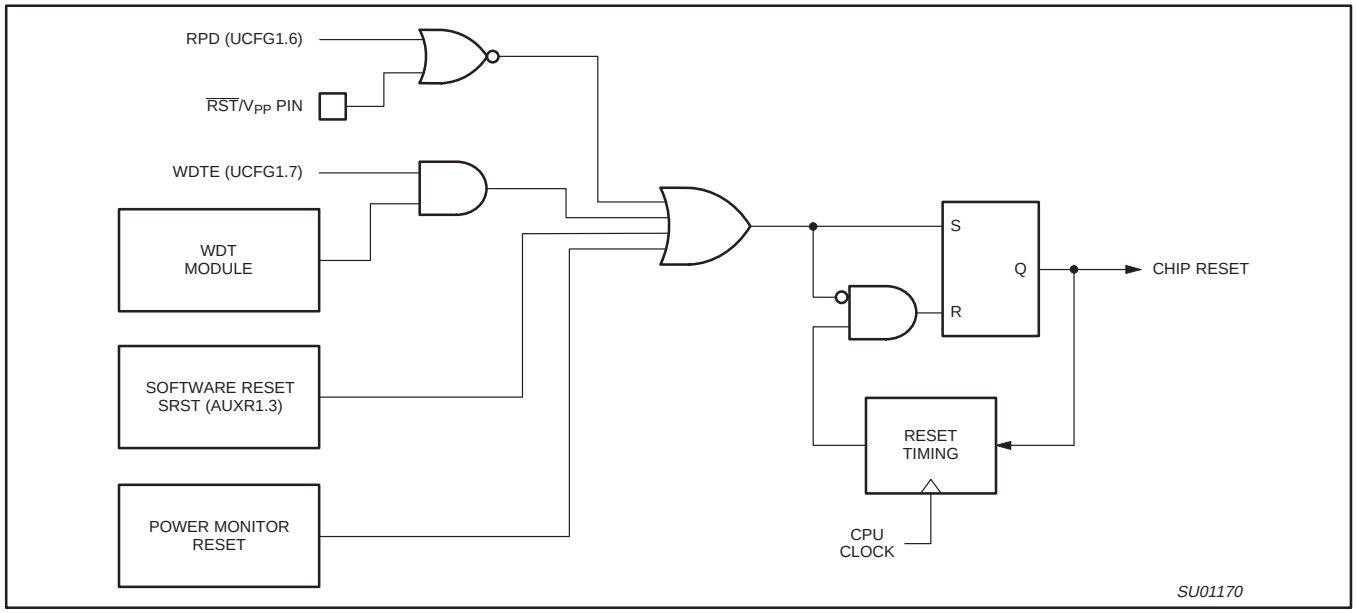


Figure 21. Block Diagram Showing Reset Sources

Timer/Counters

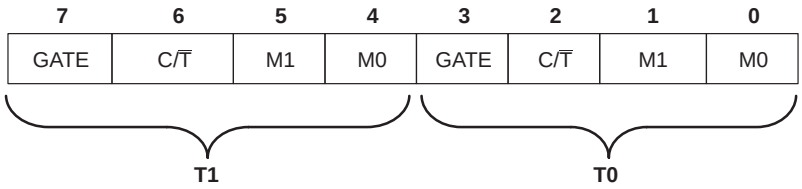
The P87LPC764 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. Both can be configured to operate either as timers or event counters (see Figure 22). An option to automatically toggle the T0 and/or T1 pins upon timer overflow has been added.

In the “Timer” function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of 6 CPU clock periods, the count rate is 1/6 of the CPU clock frequency. Refer to the section Enhanced CPU for a description of the CPU clock.

In the “Counter” function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once during every machine cycle. When the samples of the pin state show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (12 CPU clocks) to recognize a 1-to-0 transition, the maximum count rate is 1/6 of the CPU clock frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

The “Timer” or “Counter” function is selected by control bits C/$\overline{T}$ in the Special Function Register TMOD. In addition to the “Timer” or “Counter” selection, Timer 0 and Timer 1 have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timers/Counters. Mode 3 is different. The four operating modes are described in the following text.

TMOD Address: 89h Reset Value: 00h
Not Bit Addressable



BIT	SYMBOL	FUNCTION
TMOD.7	GATE	Gating control for Timer 1. When set, Timer/Counter is enabled only while the $\overline{INT1}$ pin is high and the TR1 control pin is set. When cleared, Timer 1 is enabled when the TR1 control bit is set.
TMOD.6	C/$\overline{T}$	Timer or Counter Selector for Timer 1. Cleared for Timer operation (input from internal system clock.) Set for Counter operation (input from T1 input pin).
TMOD.5, 4	M1, M0	Mode Select for Timer 1 (see table below).
TMOD.3	GATE	Gating control for Timer 0. When set, Timer/Counter is enabled only while the $\overline{INT0}$ pin is high and the TR0 control pin is set. When cleared, Timer 0 is enabled when the TR0 control bit is set.
TMOD.2	C/$\overline{T}$	Timer or Counter Selector for Timer 0. Cleared for Timer operation (input from internal system clock.) Set for Counter operation (input from T0 input pin).
TMOD.1, 0	M1, M0	Mode Select for Timer 0 (see table below).
	M1, M0	Timer Mode
	0 0	8048 Timer “TLn” serves as 5-bit prescaler.
	0 1	16-bit Timer/Counter “THn” and “TLn” are cascaded; there is no prescaler.
	1 0	8-bit auto-reload Timer/Counter. THn holds a value which is loaded into TLn when it overflows.
	1 1	Timer 0 is a dual 8-bit Timer/Counter in this mode. TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only, controlled by the Timer 1 control bits (see text). Timer 1 in this mode is stopped.

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Figure 22. Timer/Counter Mode Control Register (TMOD)

Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. Figure 24 shows Mode 0 operation.

In this mode, the Timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the Timer interrupt flag TFn. The count input is enabled to the Timer when TRn = 1 and either GATE = 0 or $\overline{INTn}$ = 1. (Setting GATE = 1 allows the Timer to be controlled by external input $\overline{INTn}$, to facilitate pulse width measurements). TRn is a control bit in the Special Function Register TCON (Figure 23). The GATE bit is in the TMOD register.

The 13-bit register consists of all 8 bits of THn and the lower 5 bits of TLn. The upper 3 bits of TLn are indeterminate and should be ignored. Setting the run flag (TRn) does not clear the registers.

Mode 0 operation is the same for Timer 0 and Timer 1. See Figure 24. There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

TCON Address: 88h Reset Value: 00h

Bit Addressable

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

BIT	SYMBOL	FUNCTION
TCON.7	TF1	Timer 1 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when the interrupt is processed, or by software.
TCON.6	TR1	Timer 1 Run control bit. Set/cleared by software to turn Timer/Counter 1 on/off.
TCON.5	TF0	Timer 0 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when the processor vectors to the interrupt routine, or by software.
TCON.4	TR0	Timer 0 Run control bit. Set/cleared by software to turn Timer/Counter 0 on/off.
TCON.3	IE1	Interrupt 1 Edge flag. Set by hardware when external interrupt 1 edge is detected. Cleared by hardware when the interrupt is processed, or by software.
TCON.2	IT1	Interrupt 1 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.
TCON.1	IE0	Interrupt 0 Edge flag. Set by hardware when external interrupt 0 edge is detected. Cleared by hardware when the interrupt is processed, or by software.
TCON.0	IT0	Interrupt 0 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.

SU01172

Figure 23. Timer/Counter Control Register (TCON)

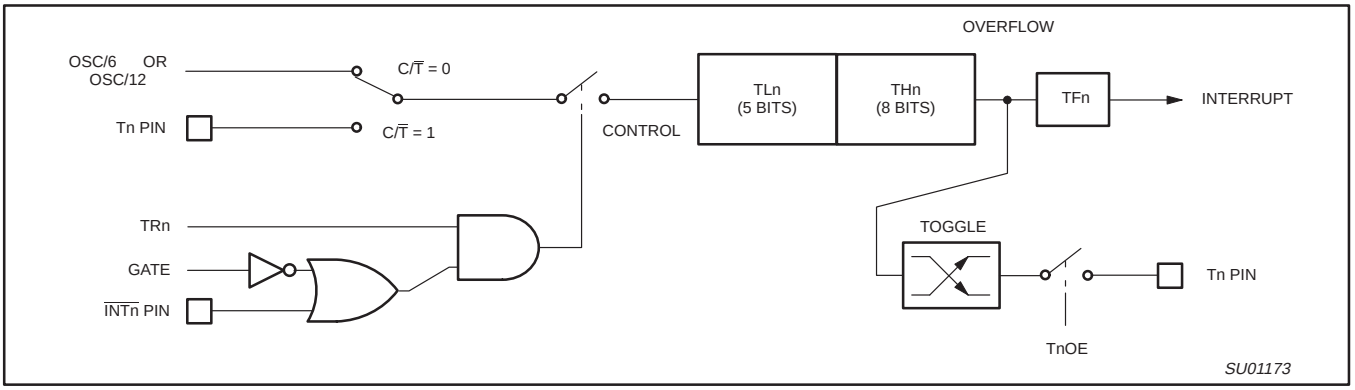

Figure 24. Timer/Counter 0 or 1 in Mode 0 (13-Bit Counter)

Table 10. Baud Rates, Timer Values, and CPU Clock Frequencies for SMOD1 = 1

Timer Count	Baud Rate						
	2400	4800	9600	19.2k	38.4k	57.6k	115.2k
–1	0.2304	0.4608	0.9216	* 1.8432	* 3.6864	5.5296	* 11.0592
–2	0.4608	0.9216	* 1.8432	* 3.6864	* 7.3728	* 11.0592	–
–3	0.6912	1.3824	2.7648	5.5296	* 11.0592	16.5888	–
–4	0.9216	* 1.8432	* 3.6864	* 7.3728	* 14.7456	–	–
–5	1.1520	2.3040	4.6080	9.2160	* 18.4320	–	–
–6	1.3824	2.7648	5.5296	* 11.0592	–	–	–
–7	1.6128	3.2256	6.4512	12.9024	–	–	–
–8	* 1.8432	* 3.6864	* 7.3728	* 14.7456	–	–	–
–9	2.0736	4.1472	8.2944	16.5888	–	–	–
–10	2.3040	4.6080	9.2160	* 18.4320	–	–	–
–11	2.5344	5.0688	10.1376	–	–	–	–
–12	2.7648	5.5296	* 11.0592	–	–	–	–
–13	2.9952	5.9904	11.9808	–	–	–	–
–14	3.2256	6.4512	12.9024	–	–	–	–
–15	3.4560	6.9120	13.8240	–	–	–	–
–16	* 3.6864	* 7.3728	* 14.7456	–	–	–	–
–17	3.9168	7.8336	15.6672	–	–	–	–
–18	4.1472	8.2944	16.5888	–	–	–	–
–19	4.3776	8.7552	17.5104	–	–	–	–
–20	4.6080	9.2160	* 18.4320	–	–	–	–
–21	4.8384	9.6768	19.3536	–	–	–	–

NOTES TO TABLES 9 AND 10:

1. Tables 6 and 7 apply to UART modes 1 and 3 (variable rate modes), and show CPU clock rates in MHz for standard baud rates from 2400 to 115.2k baud.
2. Table 6 shows timer settings and CPU clock rates with the SMOD1 bit in the PCON register = 0 (the default after reset), while Table 7 reflects the SMOD1 bit = 1.
3. The tables show all potential CPU clock frequencies up to 20 MHz that may be used for baud rates from 9600 baud to 115.2k baud. Other CPU clock frequencies that would give only lower baud rates are not shown.
4. Table entries marked with an asterisk (*) indicate standard crystal and ceramic resonator frequencies that may be obtained from many sources without special ordering.

More About UART Mode 0

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/6 the CPU clock frequency. Figure 29 shows a simplified functional diagram of the serial port in Mode 0, and associated timing.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal at S6P2 also loads a 1 into the 9th position of the transmit shift register and tells the TX Control block to commence a transmission. The internal timing is such that one full machine cycle will elapse between “write to SBUF” and activation of SEND.

SEND enables the output of the shift register to the alternate output function line of P1.1 and also enable SHIFT CLOCK to the alternate output function line of P1.0. SHIFT CLOCK is low during S3, S4, and S5 of every machine cycle, and high during S6, S1, and S2. At S6P2 of every machine cycle in which SEND is active, the contents of the transmit shift are shifted to the right one position.

As data bits shift out to the right, zeros come in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position, is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control block to do one last shift and then deactivate SEND and set T1. Both of these actions occur at S1P1 of the 10th machine cycle after “write to SBUF.” Reception is initiated by the condition REN = 1 and R1 = 0. At S6P2 of the next machine cycle, the RX Control unit writes the bits 11111110 t o the receive shift register, and in the next clock phase activates RECEIVE.

RECEIVE enable SHIFT CLOCK to the alternate output function line of P1.0. SHIFT CLOCK makes transitions at S3P1 and S6P1 of every machine cycle. At S6P2 of every machine cycle in which RECEIVE is active, the contents of the receive shift register are shifted to the left one position. The value that comes in from the right is the value that was sampled at the P1.1 pin at S5P2 of the same machine cycle.

As data bits come in from the right, 1s shift out to the left. When the 0 that was initially loaded into the rightmost position arrives at the leftmost position in the shift register, it flags the RX Control block to do one last shift and load SBUF. At S1P1 of the 10th machine cycle after the write to SCON that cleared RI, RECEIVE is cleared as RI is set.

More About UART Mode 1

Ten bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in SCON. In the P87LPC764 the baud rate is determined by the Timer 1 overflow rate. Figure 30 shows a simplified functional diagram of the serial port in Mode 1, and associated timings for transmit receive.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads a 1 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission actually commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SBUF” signal.)

The transmission begins with activation of SEND which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that.

As data bits shift out to the right, zeros are clocked in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 10th divide-by-16 rollover after “write to SBUF.”

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written into the input shift register. Resetting the divide-by-16 counter aligns its rollovers with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RxD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in mode 1 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated.: 1. R1 = 0, and 2. Either SM2 = 0, or the received stop bit = 1.

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated. At this time, whether the above conditions are met or not, the unit goes back to looking for a 1-to-0 transition in RxD.

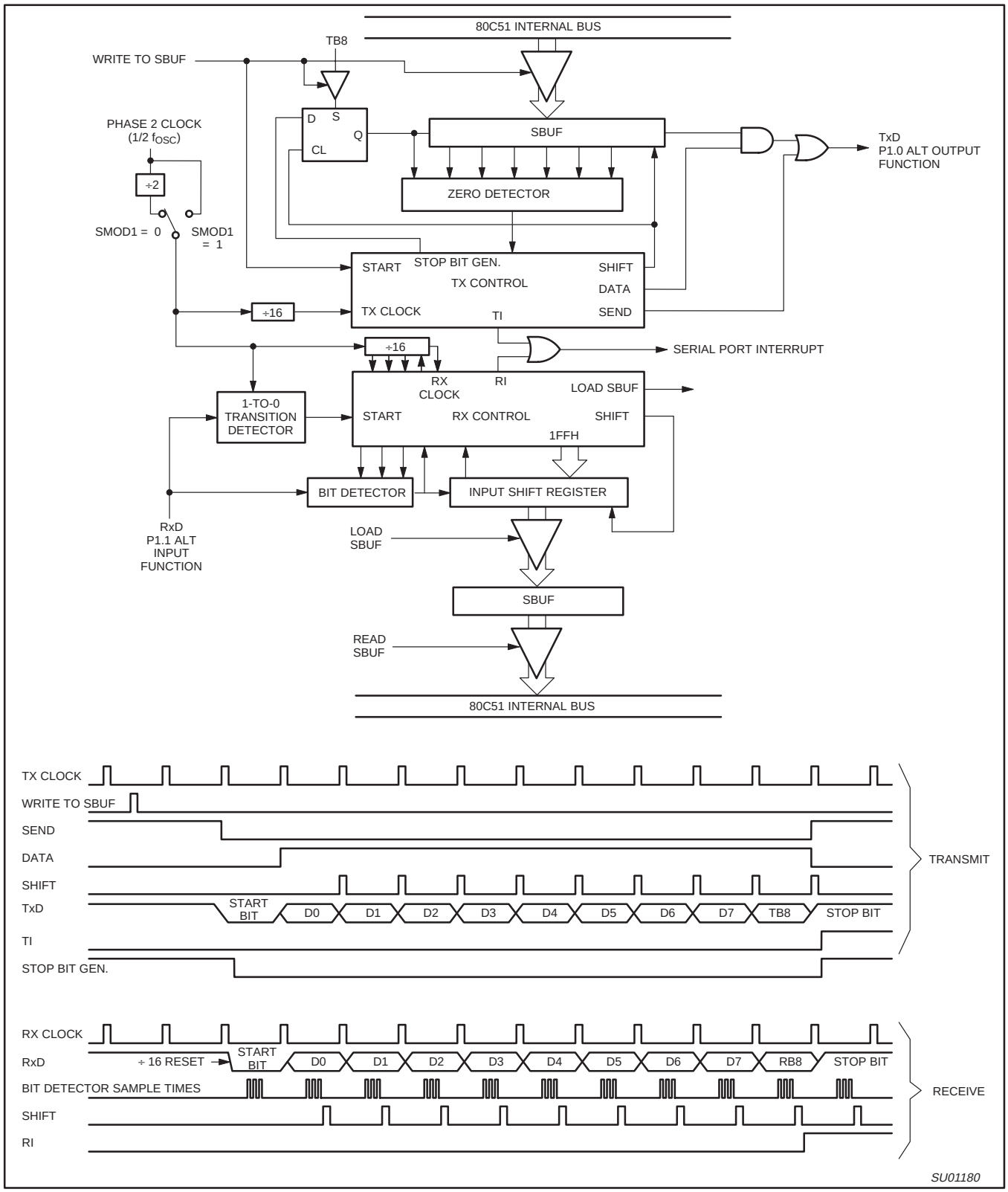

Figure 31. Serial Port Mode 2

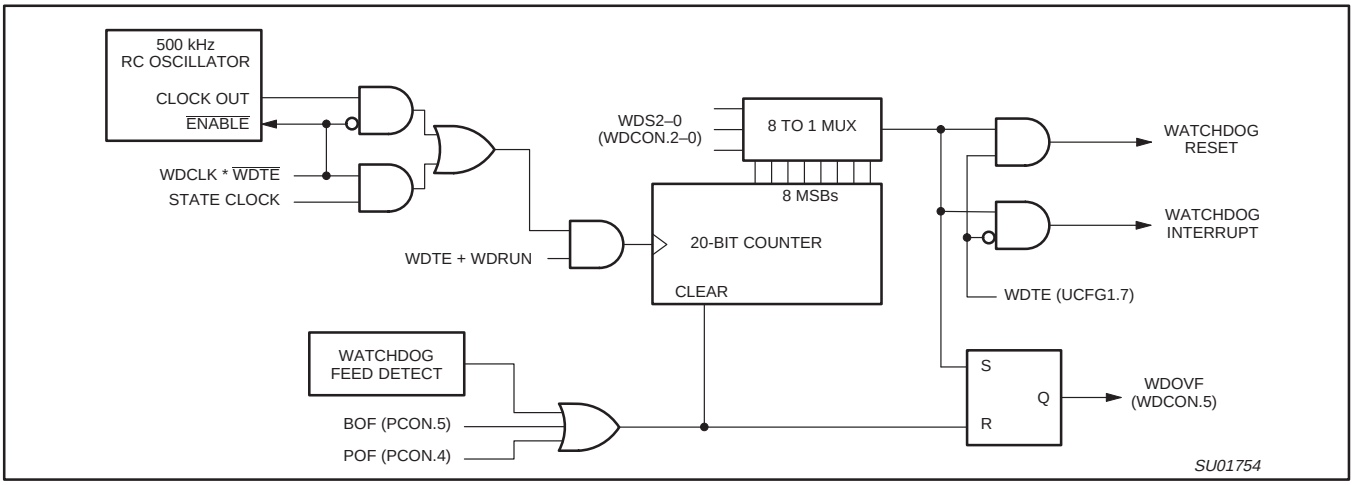

Figure 33. Block Diagram of the Watchdog Timer

WDCON Address: A7h

Not Bit Addressable

Reset Value:
- 30h for a watchdog reset.
- 10h for other rest sources if the watchdog is enabled via the WDTE configuration bit.
- 00h for other reset sources if the watchdog is disabled via the WDTE configuration bit.

7	6	5	4	3	2	1	0
—	—	WDOVF	WDRUN	WDCLK	WDS2	WDS1	WDS0

BIT	SYMBOL	FUNCTION
WDCON.7, 6	—	Reserved for future use. Should not be set to 1 by user programs.
WDCON.5	WDOVF	Watchdog timer overflow flag. Set when a watchdog reset or timer overflow occurs. Cleared when the watchdog is fed.
WDCON.4	WDRUN	Watchdog run control. The watchdog timer is started when WDRUN = 1 and stopped when WDRUN = 0. This bit is forced to 1 (watchdog running) if the WDTE configuration bit = 1.
WDCON.3	WDCLK	Watchdog clock select. The watchdog timer is clocked by CPU clock/6 when WDCLK = 1 and by the watchdog RC oscillator when WDCLK = 0. This bit is forced to 0 (using the watchdog RC oscillator) if the WDTE configuration bit = 1.
WDCON.2–0	WDS2–0	Watchdog rate select.

WDS2–0	Timeout Clocks	Minimum Time	Nominal Time	Maximum Time
0 0 0	8,192	10 ms	25 ms	40 ms
0 0 1	16,384	20 ms	50 ms	80 ms
0 1 0	32,768	41 ms	100 ms	160 ms
0 1 1	65,536	82 ms	200 ms	320 ms
1 0 0	131,072	165 ms	400 ms	640 ms
1 0 1	262,144	330 ms	800 ms	1280 ms
1 1 0	524,288	660 ms	1.60 sec	2.60 sec
1 1 1	1,048,576	1.3 sec	3.20 sec	5.30 sec

SU01476

Figure 34. Watchdog Timer Control Register (WDCON)

DC ELECTRICAL CHARACTERISTICS (FOR P87LPC764BD, BN, BDH, FN, FD, FDH, BD/01, BDH/01)

V_{DD} = 2.7 V to 6.0 V unless otherwise specified; T_{amb} = 0°C to +70°C or –40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
I_{DD}	Power supply current, operating	5.0 V, 20 MHz[11]		15	25	mA
		3.0 V, 10 MHz[11]		4	7	mA
I_{ID}	Power supply current, Idle mode	5.0 V, 20 MHz[11]		6	10	mA
		3.0 V, 10 MHz[11]		2	4	mA
I_{PD}	Power supply current, Power Down mode	5.0 V[11]		1	10	µA
		3.0 V[11]		1	5	µA
V_{RAM}	RAM keep-alive voltage		1.5			V
V_{IL}	Input low voltage (TTL input)	4.0 V < V_{DD} < 6.0 V	–0.5		0.2 V_{DD}–0.1	V
		2.7 V < V_{DD} < 4.0 V	–0.5		0.7	V
V_{IL1}	Negative going threshold (Schmitt input)		–0.5		0.3 V_{DD}	V
V_{IH}	Input high voltage (TTL input)		0.2 V_{DD}+0.9		V_{DD}+0.5	V
V_{IH1}	Positive going threshold (Schmitt input)		0.7 V_{DD}		V_{DD}+0.5	V
HYS	Hysteresis voltage			0.2 V_{DD}		V
V_{OL}	Output low voltage all ports[5, 9]	I_{OL} = 3.2 mA, V_{DD} = 2.7 V			0.4	V
V_{OL1}	Output low voltage all ports[5, 9]	I_{OL} = 20 mA, V_{DD} = 2.7 V			1.0	V
V_{OH}	Output high voltage, all ports[3]	I_{OH} = –20 µA, V_{DD} = 2.7 V	V_{DD}–0.7			V
		I_{OH} = –30 µA, V_{DD} = 4.5 V	V_{DD}–0.7			V
V_{OH1}	Output high voltage, all ports[4]	I_{OH} = –1.0 mA, V_{DD} = 2.7 V	V_{DD}–0.7			V
C_{IO}	Input/Output pin capacitance[10]				15	pF
I_{IL}	Logical 0 input current, all ports[8]	V_{IN} = 0.4 V			–50	µA
I_{LI}	Input leakage current, all ports[7]	V_{IN} = V_{IL} or V_{IH}			±2	µA
I_{TL}	Logical 1 to 0 transition current, all ports[3, 6]	V_{IN} = 1.5 V at V_{DD} = 3.0 V	–30		–250	µA
		V_{IN} = 2.0 V at V_{DD} = 5.5 V	–150		–650	µA
R_{RST}	Internal reset pull-up resistor[14]		40		225	kΩ
V_{BOLOW}	Brownout trip voltage with BOV = 1[12]		2.35		2.69	V
V_{BOHI}	Brownout trip voltage with BOV = 0		3.45		3.99	V
V_{REF}	Reference voltage		1.11	1.26	1.41	V
t_C (V_{REF})	Temperature coefficient			tbd		ppm/°C
SS	Supply sensitivity			tbd		%/V

NOTES:

1. Typical ratings are not guaranteed. The values listed are at room temperature, 5 V.
2. See other Figures for details.
   Active mode: $I_{CC(MAX)}$ = tbd
   Idle mode: $I_{CC(MAX)}$ = tbd
3. Ports in quasi-bidirectional mode with weak pull-up (applies to all port pins with pull-ups). Does not apply to open drain pins.
4. Ports in PUSH-PULL mode. Does not apply to open drain pins.
5. In all output modes except high impedance mode.
6. Port pins source a transition current when used in quasi-bidirectional mode and externally driven from 1 to 0. This current is highest when V_{IN} is approximately 2 V.
7. Measured with port in high impedance mode. Parameter is guaranteed but not tested at cold temperature.
8. Measured with port in quasi-bidirectional mode.
9. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 20 mA
   Maximum total I_{OL} for all outputs: 80 mA
   Maximum total I_{OH} for all outputs: 5 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
10. Pin capacitance is characterized but not tested.
11. The I_{DD}, I_{ID}, and I_{PD} specifications are measured using an external clock with the following functions disabled: comparators, brownout detect, and watchdog timer. For V_{DD} = 3 V, LPEP = 1. Refer to the appropriate figures on the following pages for additional current drawn by each of these functions and detailed graphs for other frequency and voltage combinations.
12. Devices initially operating at V_{DD} = 2.7V or above and at f_{OSC} = 10 MHz or less are guaranteed to continue to execute instructions correctly at the brownout trip point. Initial power-on operation below V_{DD} = 2.7 V is not guaranteed.
13. Devices initially operating at V_{DD} = 4.0 V or above and at f_{OSC} = 20 MHz or less are guaranteed to continue to execute instructions correctly at the brownout trip point. Initial power-on operation below V_{DD} = 4.0 V and F_{OSC} > 10 MHz is not guaranteed.
14. This internal resistor is disconnected if P1.5 is used as a general purpose input pin instead of the reset pin.

AC ELECTRICAL CHARACTERISTICS (FOR P87LPC764BD, BDH, BN, FN, FD, FDH)

T_{amb} = 0 °C to +70 °C or –40°C to +85°C, V_{DD} = 2.7 V to 6.0 V unless otherwise specified; V_{SS} = 0 V[1,2,3]

SYMBOL	FIGURE	PARAMETER		LIMITS		UNIT
				MIN	MAX	
External Clock						
f_{osc}	39	Oscillator frequency (V_{DD} = 4.0 V to 6.0 V)		0	20	MHz
f_{osc}	39	Oscillator frequency (V_{DD} = 2.7 V to 6.0 V)		0	10	MHz
t_C	39	Clock period and CPU timing cycle		$1/f_{osc}$	–	ns
$f_{osc(tol)}$		On-chip RC oscillator tolerance. Applies to P87LPC764BDH[5]		10	10	%
$f_{osc(tol)}$		On-chip RC oscillator tolerance, all other devices		25	25	%
t_{CLCX}	39	Clock low-time[4]	f_{OSC} = 20 MHz	20	–	ns
t_{CLCX}	39		f_{OSC} = 10 MHz	40	–	ns
t_{CHCX}	39	Clock high-time[4]	f_{OSC} = 20 MHz	20	–	ns
t_{CHCX}	39		f_{OSC} = 10 MHz	40	–	ns
Shift Register						
t_{XLXL}	38	Serial port clock cycle time		$6t_C$	–	ns
t_{QVXH}	38	Output data setup to clock rising edge		$5t_C$ – 133	–	ns
t_{XHQX}	38	Output data hold after clock rising edge		$1t_C$ – 80	–	ns
t_{XHDV}	38	Input data setup to clock rising edge		–	$5t_C$ – 133	ns
t_{XHDX}	38	Input data hold after clock rising edge		0	–	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for all outputs = 80 pF.
3. Parts are guaranteed to operate down to 0 Hz.
4. Applies only to an external clock source, not when a crystal is connected to the X1 and X2 pins.
5. For availability of other devices with this specification, please contact Philips sales office.

AC ELECTRICAL CHARACTERISTICS (FOR P87LPC764HDH)

V_{DD} = 4.5 V to 5.5 V; T_{amb} = –40°C to +125°C; V_{SS} = 0 V[1,2,3]

SYMBOL	FIGURE	PARAMETER		LIMITS		UNIT
				MIN	MAX	
External Clock						
f_{osc}	39			0	16	MHz
t_C	39	Clock period and CPU timing cycle		$1/f_{osc}$		ns
$f_{osc(tol)}$		on-chip RC oscillator tolerance		–10	+10	%
t_{CHCX}	39	Clock high-time[4]	f_{OSC} = 16 MHz	25		ns
t_{CLCX}	39	Clock low-time[4]	f_{OSC} = 16 MHz	25		ns
Shift Register						
t_{XLXL}	38	Serial port clock cycle time		$6t_C$		ns
t_{QVXH}	38	Output data setup to clock rising edge		$5t_C$ – 133		ns
t_{XHQX}	38	Output data hold after clock rising edge		$1t_C$ – 80		ns
t_{XHDV}	38	Input data setup to clock rising edge			$5t_C$ – 133	ns
t_{XHDX}	38	Input data hold after clock rising edge		0		ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for all outputs = 80 pF.
3. Parts are guaranteed to operate down to 0 Hz.
4. Applies only to an external clock source, not when a crystal is connected to the X1 and X2 pins.
5. For availability of other devices with this specification, please contact Philips sales office.

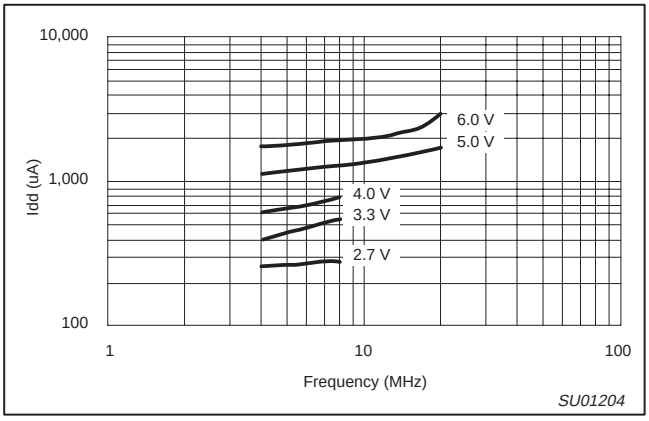

Figure 42. Typical Idd versus frequency (high frequency oscillator, 25°C)

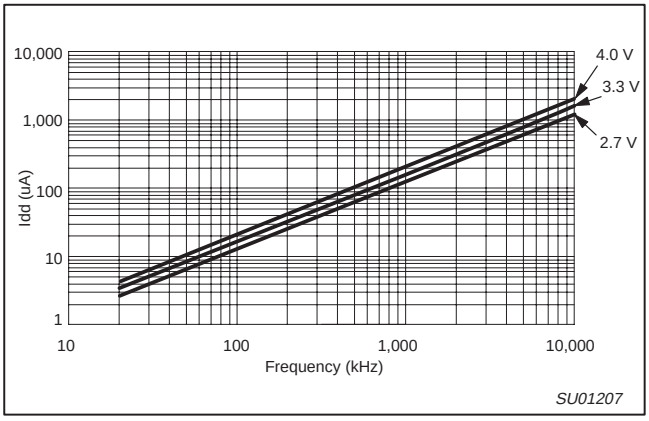

Figure 45. Typical Idle Idd versus frequency (external clock, 25°C, LPEP=1)

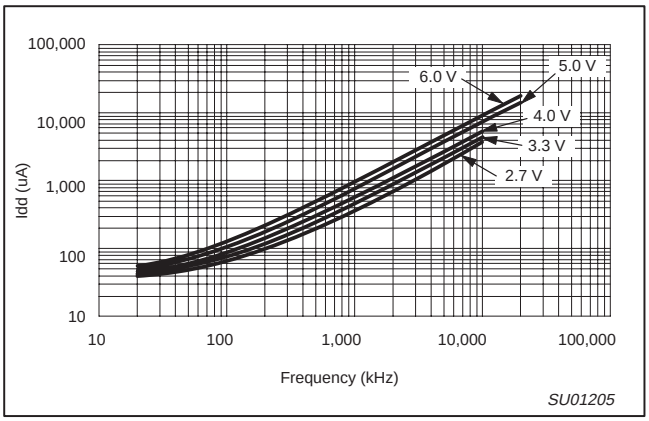

Figure 43. Typical Active Idd versus frequency (external clock, 25°C, LPEP=0)

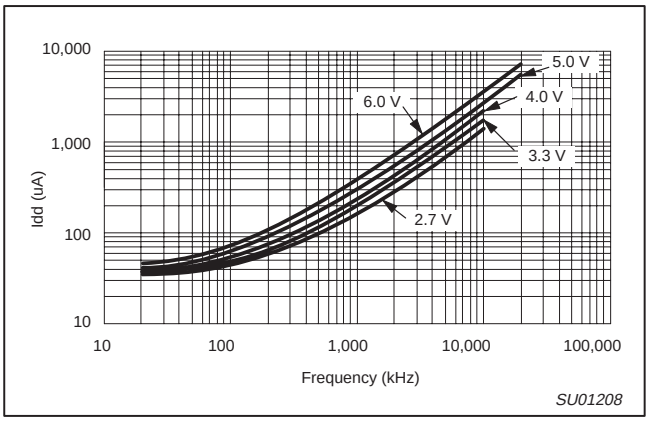

Figure 46. Typical Idle Idd versus frequency (external clock, 25°C, LPEP=0)

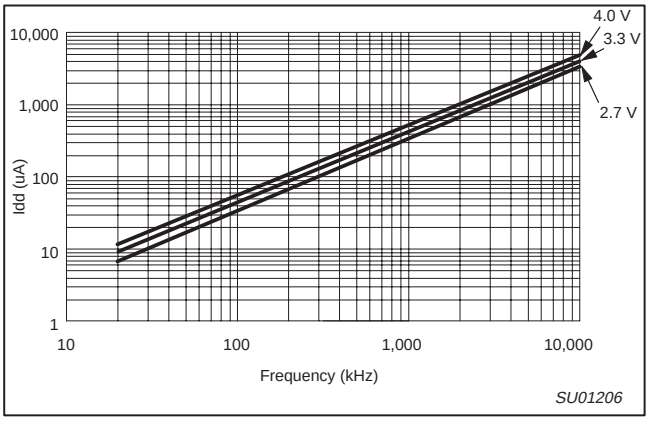

Figure 44. Typical Active Idd versus frequency (external clock, 25°C, LPEP=1)

REVISION HISTORY

Rev	Date	Description
_11	20030903	**Product data (9397 750 11121); ECN 853-2401 30269** Modifications: ● Added BD/01, BDH/01 and HDH part types
_10	20011026	**Preliminary data (9397 750 09017); previous release**

Low power, low price, low pin count (20 pin) microcontroller with 4 kbyte OTP

P87LPC764

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Date of release: 09-03

Document order number: 9397 750 11121

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