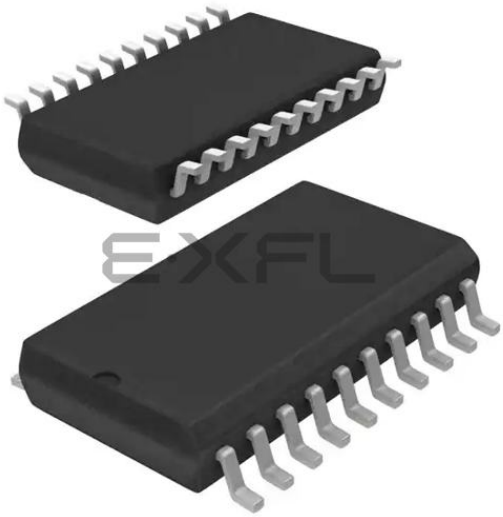

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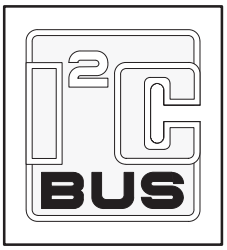
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p87lpc764fd-512

Low power, low price, low pin count (20 pin) microcontroller with 4 kbyte OTP

P87LPC764



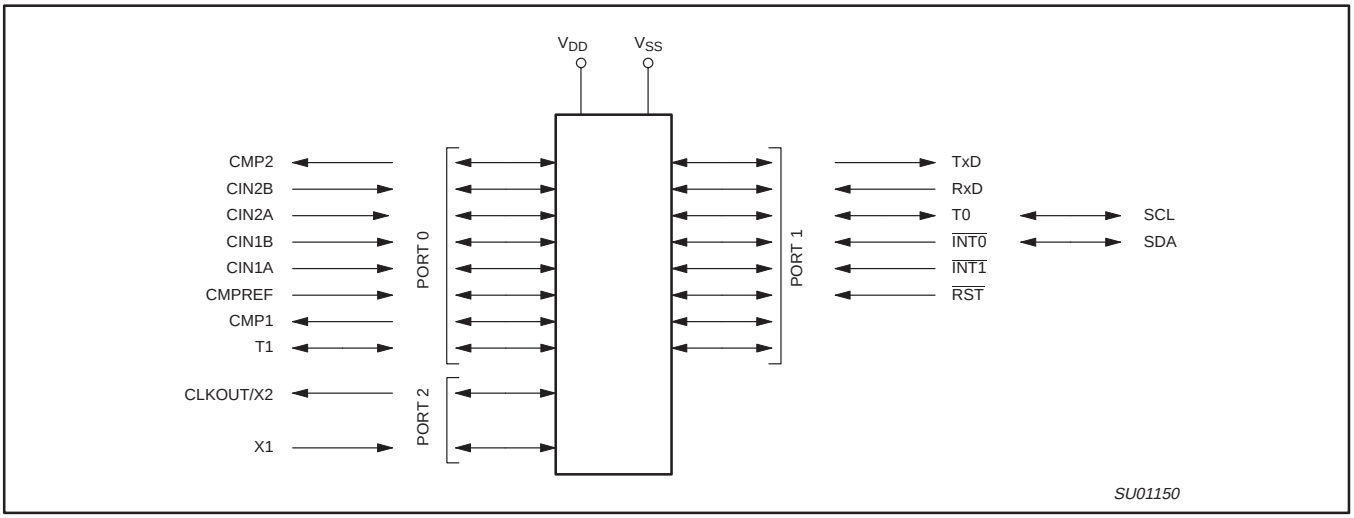
GENERAL DESCRIPTION

The P87LPC764 is a 20-pin single-chip microcontroller designed for low pin count applications demanding high-integration, low cost solutions over a wide range of performance requirements. A member of the Philips low pin count family, the P87LPC764 offers programmable oscillator configurations for high and low speed crystals or RC operation, wide operating voltage range, programmable port output configurations, selectable Schmitt trigger inputs, LED drive outputs, and a built-in watchdog timer. The P87LPC764 is based on an accelerated 80C51 processor architecture that executes instructions at twice the rate of standard 80C51 devices.

FEATURES

- An accelerated 80C51 CPU provides instruction cycle times of 300–600 ns for all instructions except multiply and divide when executing at 20 MHz. Execution at up to 20 MHz when V_{DD} = 4.5 V to 6.0 V, 10 MHz when V_{DD} = 2.7 V to 6.0 V.
- 4.5 V to 5.5 V for P87LPC764HDH.
- 2.7 V to 6.0 V operating range for digital functions.
- 4 kbytes EPROM code memory.
- 128 byte RAM data memory.
- 32 byte customer code EPROM allows serialization of devices, storage of setup parameters, etc.
- Two 16-bit counter/timers. Each timer may be configured to toggle a port output upon timer overflow.
- Two analog comparators.
- Full duplex UART.
- I^2C communication port.
- Eight keypad interrupt inputs, plus two additional external interrupt inputs.
- Four interrupt priority levels.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog timeout time is selectable from 8 values.
- Active low reset. On-chip power-on reset allows operation with no external reset components.
- Low voltage reset. One of two preset low voltage levels may be selected to allow a graceful system shutdown when power fails. May optionally be configured as an interrupt.
- Oscillator Fail Detect. The watchdog timer has a separate fully on-chip oscillator, allowing it to perform an oscillator fail detect function.
- Configurable on-chip oscillator with frequency range and RC oscillator options (selected by user programmed EPROM bits). The RC oscillator option allows operation with no external oscillator components.
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- Selectable Schmitt trigger port inputs.
- LED drive capability (20 mA) on all port pins.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- 15 I/O pins minimum. Up to 18 I/O pins using on-chip oscillator and reset options.
- Only power and ground connections are required to operate the P87LPC764 when fully on-chip oscillator and reset options are selected.
- Serial EPROM programming allows simple in-circuit production coding. Two EPROM security bits prevent reading of sensitive application programs.
- Idle and Power Down reduced power modes. Improved wakeup from Power Down mode (a low interrupt input starts execution). Typical Power Down current is 1 μA.
- 20-pin DIP, SO, and TSSOP packages.

LOGIC SYMBOL



SPECIAL FUNCTION REGISTERS

Name	Description	SFR Address	Bit Functions and Addresses MSB							LSB	Reset Value
			E7	E6	E5	E4	E3	E2	E1	E0	
ACC*	Accumulator	E0h									00h
AUXR1#	Auxiliary Function Register	A2h	KBF	BOD	BOI	LPEP	SRST	0	–	DPS	02h[1]
			F7	F6	F5	F4	F3	F2	F1	F0	
B*	B register	F0h									00h
CMP1#	Comparator 1 control register	ACh	–	–	CE1	CP1	CN1	OE1	CO1	CMF1	00h[1]
CMP2#	Comparator 2 control register	ADh	–	–	CE2	CP2	CN2	OE2	CO2	CMF2	00h[1]
DIVM#	CPU clock divide-by-M control	95h									00h
DPTR:	Data pointer (2 bytes)										
DPH	Data pointer high byte	83h									00h
DPL	Data pointer low byte	82h									00h
			CF	CE	CD	CC	CB	CA	C9	C8	
I2CFG#*	I^2C configuration register	C8h/RD	SLAVEN	MASTRQ	0	TIRUN	–	–	CT1	CT0	00h[1]
		C8h/WR	SLAVEN	MASTRQ	CLRTI	TIRUN	–	–	CT1	CT0	
			DF	DE	DD	DC	DB	DA	D9	D8	
I2CON#*	I^2C control register	D8h/RD	RDAT	ATN	DRDY	ARL	STR	STP	MASTER	–	80h[1]
		D8h/WR	CXA	IDLE	CDR	CARL	CSTR	CSTP	XSTR	XSTP	
I2DAT#	I^2C data register	D9h/RD	RDAT	0	0	0	0	0	0	0	80h
		D9h/WR	XDAT	x	x	x	x	x	x	x	
			AF	AE	AD	AC	AB	AA	A9	A8	
IEN0*	Interrupt enable 0	A8h	EA	EWD	EBO	ES	ET1	EX1	ET0	EX0	00h
			EF	EE	ED	EC	EB	EA	E9	E8	
IEN1#*	Interrupt enable 1	E8h	ETI	–	EC1	–	–	EC2	EKB	EI2	00h[1]
			BF	BE	BD	BC	BB	BA	B9	B8	
IP0*	Interrupt priority 0	B8h	–	PWD	PBO	PS	PT1	PX1	PT0	PX0	00h[1]
IP0H#	Interrupt priority 0 high byte	B7h	–	PWDH	PBOH	PSH	PT1H	PX1H	PT0H	PX0H	00h[1]
			FF	FE	FD	FC	FB	FA	F9	F8	
IP1*	Interrupt priority 1	F8h	PTI	–	PC1	–	–	PC2	PKB	PI2	00h[1]
IP1H#	Interrupt priority 1 high byte	F7h	PTIH	–	PC1H	–	–	PC2H	PKBH	PI2H	00h[1]
KBI#	Keyboard Interrupt	86h									00h
			87	86	85	84	83	82	81	80	
P0*	Port 0	80h	T1	CMP1	CMPREF	CIN1A	CIN1B	CIN2A	CIN2B	CMP2	Note 2
			97	96	95	94	93	92	91	90	
P1*	Port 1	90h	(P1.7)	(P1.6)	$\overline{RST}$	$\overline{INT1}$	$\overline{INT0}$	T0	RxD	TxD	Note 2
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0h	–	–	–	–	–	–	X1	X2	Note 2
P0M1#	Port 0 output mode 1	84h	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	00h
P0M2#	Port 0 output mode 2	85h	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00H
P1M1#	Port 1 output mode 1	91h	(P1M1.7)	(P1M1.6)	–	(P1M1.4)	–	–	(P1M1.1)	(P1M1.0)	00h[1]
P1M2#	Port 1 output mode 2	92h	(P1M2.7)	(P1M2.6)	–	(P1M2.4)	–	–	(P1M2.1)	(P1M2.0)	00h[1]
P2M1#	Port 2 output mode 1	A4h	P2S	P1S	P0S	ENCLK	T1OE	T0OE	(P2M1.1)	(P2M1.0)	00h
P2M2#	Port 2 output mode 2	A5h	–	–	–	–	–	–	(P2M2.1)	(P2M2.0)	00h[1]
PCON	Power control register	87h	SMOD1	SMOD0	BOF	POF	GF1	GF0	PD	IDL	Note 3

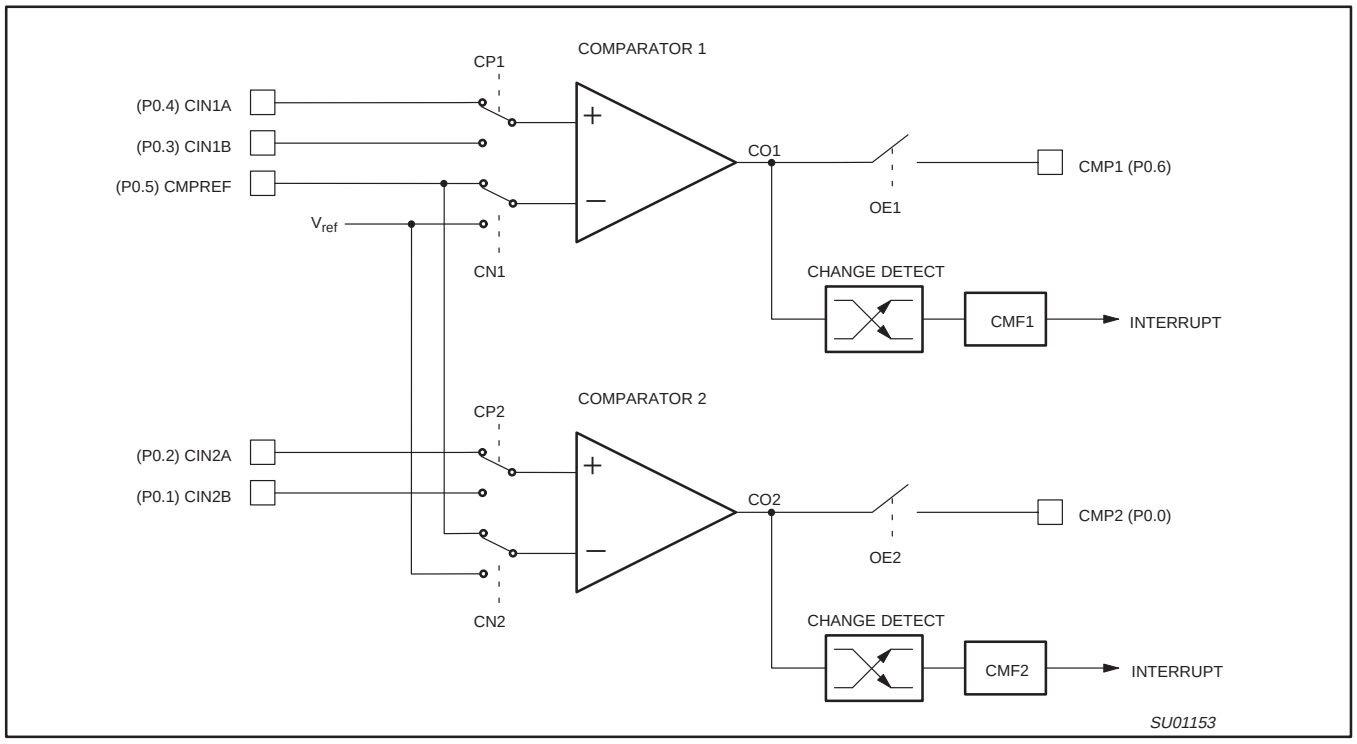


Figure 3. Comparator Input and Output Connections

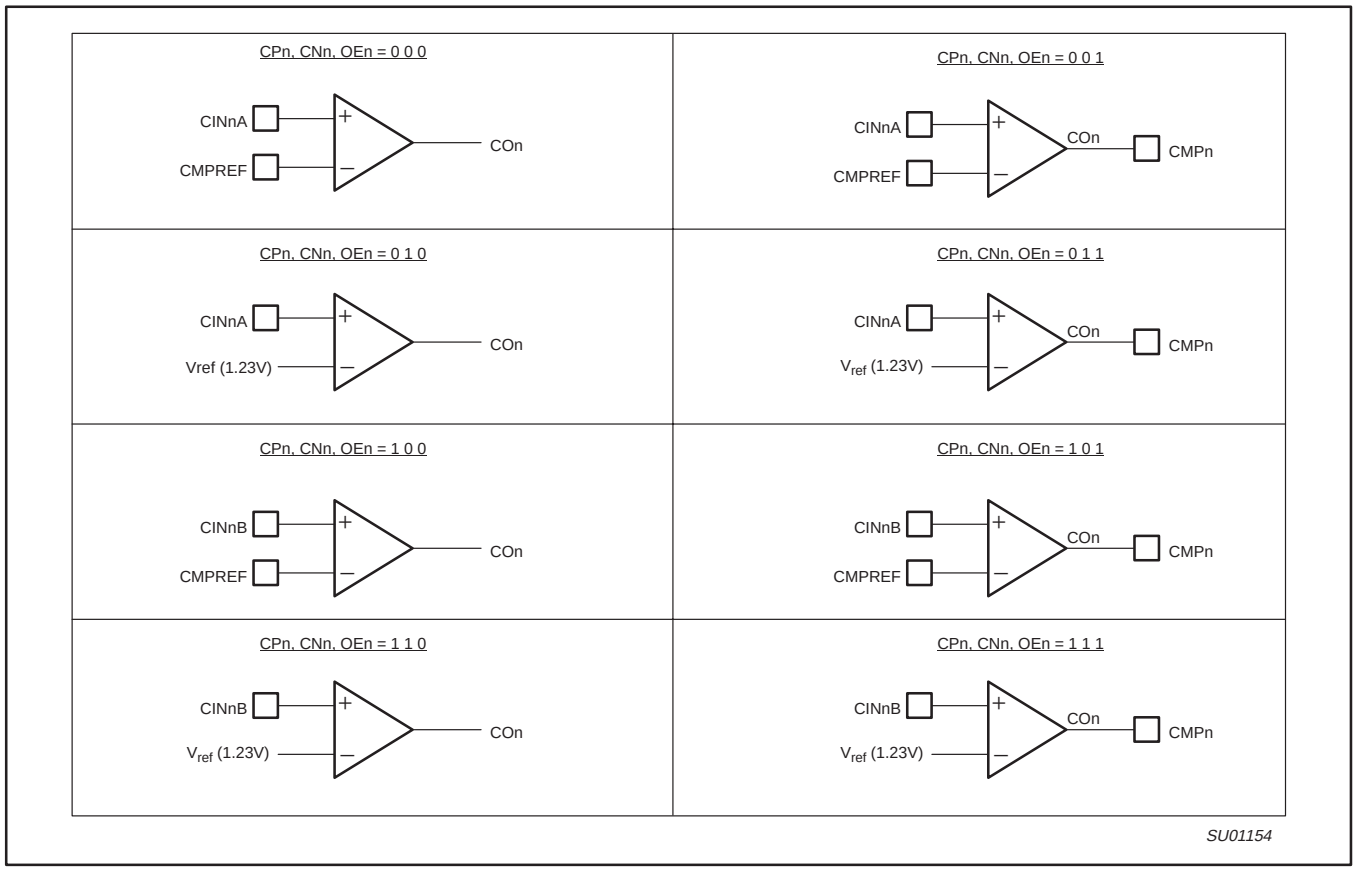


Figure 4. Comparator Configurations

Internal Reference Voltage
An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as V_{ref}, is 1.28 V ±10%.

Comparator Interrupt
Each comparator has an interrupt flag CMFn contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The interrupt will be generated when the corresponding enable bit ECn in the IEN1 register is set and the interrupt system is enabled via the EA bit in the IEN0 register.

Comparators and Power Reduction Modes
Either or both comparators may remain enabled when Power Down or Idle mode is activated. The comparators will continue to function in the power reduction mode. If a comparator interrupt is enabled, a change of the comparator output state will generate an interrupt and wake up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in power down mode. The reason is that with the oscillator stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power Down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue.

Comparator Configuration Example
The code shown in Figure 5 is an example of initializing one comparator. Comparator 1 is configured to use the CIN1A and CMPREF inputs, outputs the comparator result to the CMP1 pin, and generates an interrupt when the comparator output changes.

The interrupt routine used for the comparator must clear the interrupt flag (CMF1 in this case) before returning.

```
CmpInit:
    mov     PT0AD,#30h      ; Disable digital inputs on pins that are used
                            ;   for analog functions: CIN1A, CMPREF.
    anl     P0M2,#0cfh      ; Disable digital outputs on pins that are used
    orl     P0M1,#30h       ;   for analog functions: CIN1A, CMPREF.
    mov     CMP1,#24h       ; Turn on comparator 1 and set up for:
                            ;   – Positive input on CIN1A.
                            ;   – Negative input from CMPREF pin.
                            ;   – Output to CMP1 pin enabled.
    call    delay10us       ; The comparator has to start up for at
                            ;   least 10 microseconds before use.
    anl     CMP1,#0feh      ; Clear comparator 1 interrupt flag.
    setb    EC1             ; Enable the comparator 1 interrupt. The
                            ;   priority is left at the current value.
    setb    EA              ; Enable the interrupt system (if needed).
    ret                     ; Return to caller.
```

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Figure 5.

ARL "Arbitration Loss" is 1 when transmit Active was set, but this device lost arbitration to another transmitter. Transmit Active is cleared when ARL is 1. There are four separate cases in which ARL is set.

1. If the program sent a 1 or repeated start, but another device sent a 0, or a stop, so that SDA is 0 at the rising edge of SCL. (If the other device sent a stop, the setting of ARL will be followed shortly by STP being set.)

2. If the program sent a 1, but another device sent a repeated start, and it drove SDA low before SCL could be driven low. (This type of ARL is always accompanied by STR = 1.)

3. In master mode, if the program sent a repeated start, but another device sent a 1, and it drove SCL low before this device could drive SDA low.

4. In master mode, if the program sent stop, but it could not be sent because another device sent a 0.

STR "STaRt" is set to a 1 when an I^2C start condition is detected at a non-idle slave or at a master. (STR is not set when an idle slave becomes active due to a start bit; the slave has nothing useful to do until the rising edge of SCL sets DRDY.)

STP "SToP" is set to 1 when an I^2C stop condition is detected at a non-idle slave or at a master. (STP is not set for a stop condition at an idle slave.)

MASTER "MASTER" is 1 if this device is currently a master on the I^2C. MASTER is set when MASTRQ is 1 and the bus is not busy (i.e., if a start bit hasn't been received since reset or a "Timer I" time-out, or if a stop has been received since the last start). MASTER is cleared when ARL is set, or after the software writes MASTRQ = 0 and then XSTP = 1.

Writing I2CON

Typically, for each bit in an I^2C message, a service routine waits for ATN = 1. Based on DRDY, ARL, STR, and STP, and on the current bit position in the message, it may then write I2CON with one or more of the following bits, or it may read or write the I2DAT register.

CXA Writing a 1 to "Clear Xmit Active" clears the Transmit Active state. (Reading the I2DAT register also does this.)

Regarding Transmit Active

Transmit Active is set by writing the I2DAT register, or by writing I2CON with XSTR = 1 or XSTP = 1. The I^2C interface will only drive the SDA line low when Transmit Active is set, and the ARL bit will only be set to 1 when Transmit Active is set. Transmit Active is cleared by reading the I2DAT register, or by writing I2CON with CXA = 1. Transmit Active is automatically cleared when ARL is 1.

IDLE Writing 1 to "IDLE" causes a slave's I^2C hardware to ignore the I^2C until the next start condition (but if MASTRQ is 1, then a stop condition will cause this device to become a master).

CDR Writing a 1 to "Clear Data Ready" clears DRDY. (Reading or writing the I2DAT register also does this.)

CARL Writing a 1 to "Clear Arbitration Loss" clears the ARL bit.

CSTR Writing a 1 to "Clear STaRt" clears the STR bit.

CSTP Writing a 1 to "Clear SToP" clears the STP bit. Note that if one or more of DRDY, ARL, STR, or STP is 1, the low time of SCL is stretched until the service routine responds by clearing them.

XSTR Writing 1s to "Xmit repeated STaRt" and CDR tells the I^2C hardware to send a repeated start condition. This should only be at a master. Note that XSTR need not and should not be used to send an "initial" (non-repeated) start; it is sent automatically by the I^2C hardware. Writing XSTR = 1 includes the effect of writing I2DAT with XDAT = 1; it sets Transmit Active and releases SDA to high during the SCL low time. After SCL goes high, the I^2C hardware waits for the suitable minimum time and then drives SDA low to make the start condition.

XSTP Writing 1s to "Xmit SToP" and CDR tells the I^2C hardware to send a stop condition. This should only be done at a master. If there are no more messages to initiate, the service routine should clear the MASTRQ bit in I2CFG to 0 before writing XSTP with 1. Writing XSTP = 1 includes the effect of writing I2DAT with XDAT = 0; it sets Transmit Active and drives SDA low during the SCL low time. After SCL goes high, the I^2C hardware waits for the suitable minimum time and then releases SDA to high to make the stop condition.

External Interrupt Inputs

The P87LPC764 has two individual interrupt inputs as well as the Keyboard Interrupt function. The latter is described separately elsewhere in this section. The two interrupt inputs are identical to those present on the standard 80C51 microcontroller.

The external sources can be programmed to be level-activated or transition-activated by setting or clearing bit IT1 or IT0 in Register TCON. If ITn = 0, external interrupt n is triggered by a detected low at the $\overline{INTn}$ pin. If ITn = 1, external interrupt n is edge triggered. In this mode if successive samples of the $\overline{INTn}$ pin show a high in one cycle and a low in the next cycle, interrupt request flag IEn in TCON is set, causing an interrupt request.

Since the external interrupt pins are sampled once each machine cycle, an input high or low should hold for at least 6 CPU Clocks to ensure proper sampling. If the external interrupt is transition-activated, the external source has to hold the request pin high for at least one machine cycle, and then hold it low for at least one machine cycle. This is to ensure that the transition is seen and that interrupt request flag IEn is set. IEn is automatically cleared by the CPU when the service routine is called.

If the external interrupt is level-activated, the external source must hold the request active until the requested interrupt is actually generated. If the external interrupt is still asserted when the interrupt service routine is completed another interrupt will be generated. It is not necessary to clear the interrupt flag IEn when the interrupt is level sensitive, it simply tracks the input pin level.

If an external interrupt is enabled when the P87LPC764 is put into Power Down or Idle mode, the interrupt will cause the processor to wake up and resume operation. Refer to the section on Power Reduction Modes for details.

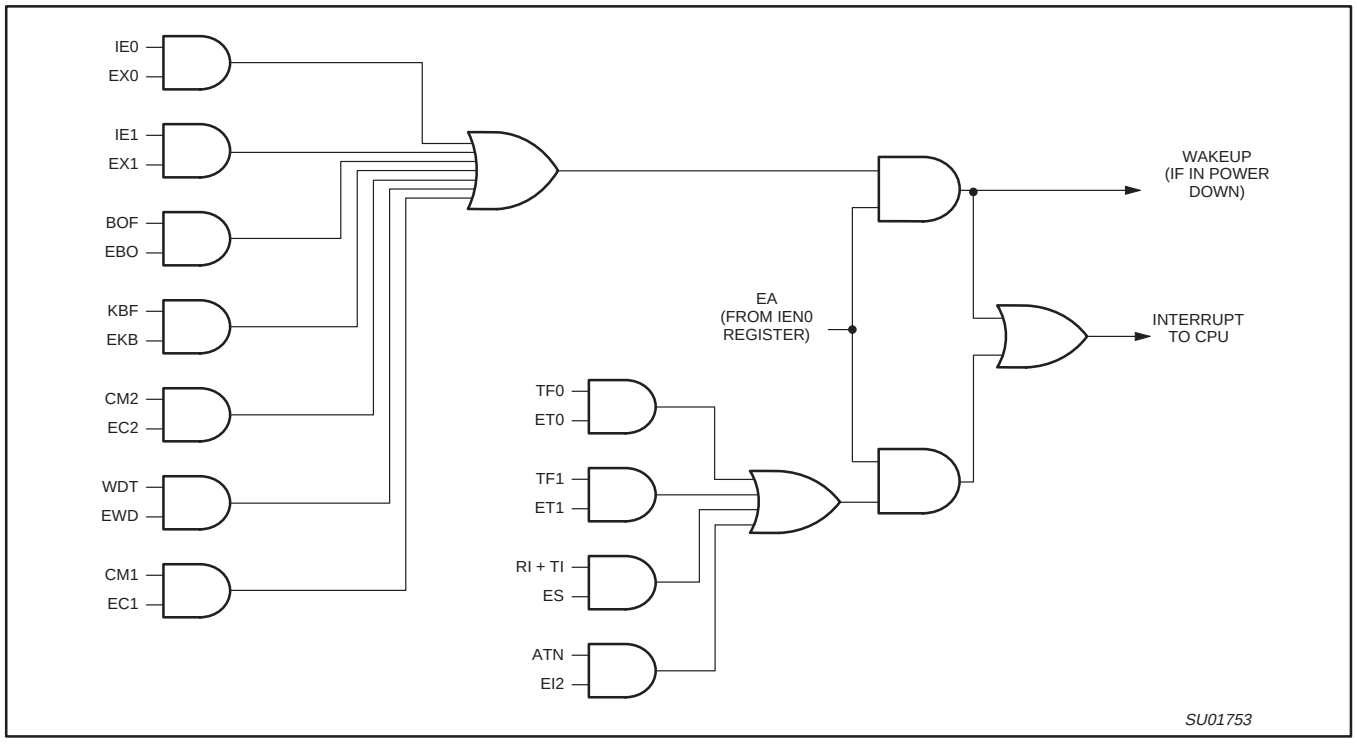

Figure 9. Interrupt Sources, Interrupt Enables, and Power Down Wakeup Sources

P2M1 Address: A4h Reset Value: 00h

Not Bit Addressable

7	6	5	4	3	2	1	0
P2S	P1S	P0S	ENCLK	T1OE	T0OE	(P2M1.1)	(P2M1.0)

BIT	SYMBOL	FUNCTION
P2M1.7	P2S	When P2S = 1, this bit enables Schmitt trigger inputs on Port 2.
P2M1.6	P1S	When P1S = 1, this bit enables Schmitt trigger inputs on Port 1.
P2M1.5	P0S	When P0S = 1, this bit enables Schmitt trigger inputs on Port 0.
P2M1.4	ENCLK	When ENCLK is set and the 87LPC764 is configured to use the on-chip RC oscillator, a clock output is enabled on the X2 pin (P2.0). Refer to the Oscillator section for details.
P2M1.3	T1OE	When set, the P0.7 pin is toggled whenever Timer 1 overflows. The output frequency is therefore one half of the Timer 1 overflow rate. Refer to the Timer/Counters section for details.
P2M1.2	T0OE	When set, the P1.2 pin is toggled whenever Timer 0 overflows. The output frequency is therefore one half of the Timer 0 overflow rate. Refer to the Timer/Counterssection for details.
P2M1.1, P2M1.0	—	These bits, along with the matching bits in the P2M2 register, control the output configuration of P2.1 and P2.0 respectively, as shown in Table 4.

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Figure 13. Port 2 Mode Register 1 (P2M1)

Keyboard Interrupt (KBI)

The Keyboard Interrupt function is intended primarily to allow a single interrupt to be generated when any key is pressed on a keyboard or keypad connected to specific pins of the P87LPC764, as shown in Figure 14. This interrupt may be used to wake up the CPU from Idle or Power Down modes. This feature is particularly useful in handheld, battery powered systems that need to carefully manage power consumption yet also need to be convenient to use.

The P87LPC764 allows any or all pins of port 0 to be enabled to cause this interrupt. Port pins are enabled by the setting of bits in the KBI register, as shown in Figure 15. The Keyboard Interrupt Flag (KBF) in the AUXR1 register is set when any enabled pin is pulled low while the KBI interrupt function is active. An interrupt will generated if it has been enabled. Note that the KBF bit must be cleared by software.

Due to human time scales and the mechanical delay associated with keyswitch closures, the KBI feature will typically allow the interrupt service routine to poll port 0 in order to determine which key was pressed, even if the processor has to wake up from Power Down mode. Refer to the section on Power Reduction Modes for details.

Oscillator

The P87LPC764 provides several user selectable oscillator options, allowing optimization for a range of needs from high precision to lowest possible cost. These are configured when the EPROM is programmed. Basic oscillator types that are supported include: low, medium, and high speed crystals, covering a range from 20 kHz to 20 MHz; ceramic resonators; and on-chip RC oscillator.

Low Frequency Oscillator Option

This option supports an external crystal in the range of 20 kHz to 100 kHz.

Table 5 shows capacitor values that may be used with a quartz crystal in this mode.

Table 5. Recommended oscillator capacitors for use with the low frequency oscillator option

Oscillator Frequency	V_{DD} = 2.7 to 4.5 V			V_{DD} = 4.5 to 6.0 V		
	Lower Limit	Optimal Value	Upper Limit	Lower Limit	Optimal Value	Upper Limit
20 kHz	15 pF	15 pF	33 pF	33 pF	33 pF	47 pF
32 kHz	15 pF	15 pF	33 pF	33 pF	33 pF	47 pF
100 kHz	15 pF	15 pF	33 pF	15 pF	15 pF	33 pF

Medium Frequency Oscillator Option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

Table 6 shows capacitor values that may be used with a quartz crystal in this mode.

Table 6. Recommended oscillator capacitors for use with the medium frequency oscillator option

Oscillator Frequency	V_{DD} = 2.7 to 4.5 V			V_{DD} = 4.5 to 6.0 V		
	Lower Limit	Optimal Value	Upper Limit	Lower Limit	Optimal Value	Upper Limit
100 kHz	33 pF	33 pF	47 pF	33 pF	33 pF	47 pF
1 MHz	15 pF	15 pF	33 pF	15 pF	22 pF	47 pF
4 MHz	15 pF	15 pF	33 pF	15 pF	15 pF	33 pF

High Frequency Oscillator Option

This option supports an external crystal in the range of 4 to 20 MHz. Ceramic resonators are also supported in this configuration.

Table 7 shows capacitor values that may be used with a quartz crystal in this mode.

Table 7. Recommended oscillator capacitors for use with the high frequency oscillator option

Oscillator Frequency	V_{DD} = 2.7 to 4.5 V			V_{DD} = 4.5 to 6.0 V		
	Lower Limit	Optimal Value	Upper Limit	Lower Limit	Optimal Value	Upper Limit
4 MHz	15 pF	33 pF	47 pF	15 pF	33 pF	68 pF
8 MHz	15 pF	15 pF	33 pF	15 pF	33 pF	47 pF
16 MHz	–	–	–	15 pF	15 pF	33 pF
20 MHz	–	–	–	15 pF	15 pF	33 pF

On-Chip RC Oscillator Option

The on-chip RC oscillator option has a typical frequency of 6 MHz and can be divided down for slower operation through the use of the DIVM register. For on-chip oscillator tolerance see AC Electrical Characteristics table. A clock output on the X2/P2.0 pin may be enabled when the on-chip RC oscillator is used.

External Clock Input Option

In this configuration, the processor clock is input from an external source driving the X1/P2.1 pin. The rate may be from 0 Hz up to 20 MHz when V_{DD} is above 4.5 V and up to 10 MHz when V_{DD} is below 4.5 V. When the external clock input mode is used, the X2/P2.0 pin may be used as a standard port pin. A clock output on the X2/P2.0 pin may be enabled when the external clock input is used.

Clock Output

The P87LPC764 supports a clock output function when either the on-chip RC oscillator or external clock input options are selected. This allows external devices to synchronize to the P87LPC764. When enabled, via the ENCLK bit in the P2M1 register, the clock output appears on the X2/CLKOUT pin whenever the on-chip oscillator is running, including in Idle mode. The frequency of the clock output is 1/6 of the CPU clock rate. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power. The clock output may also be enabled when the external clock input option is selected.

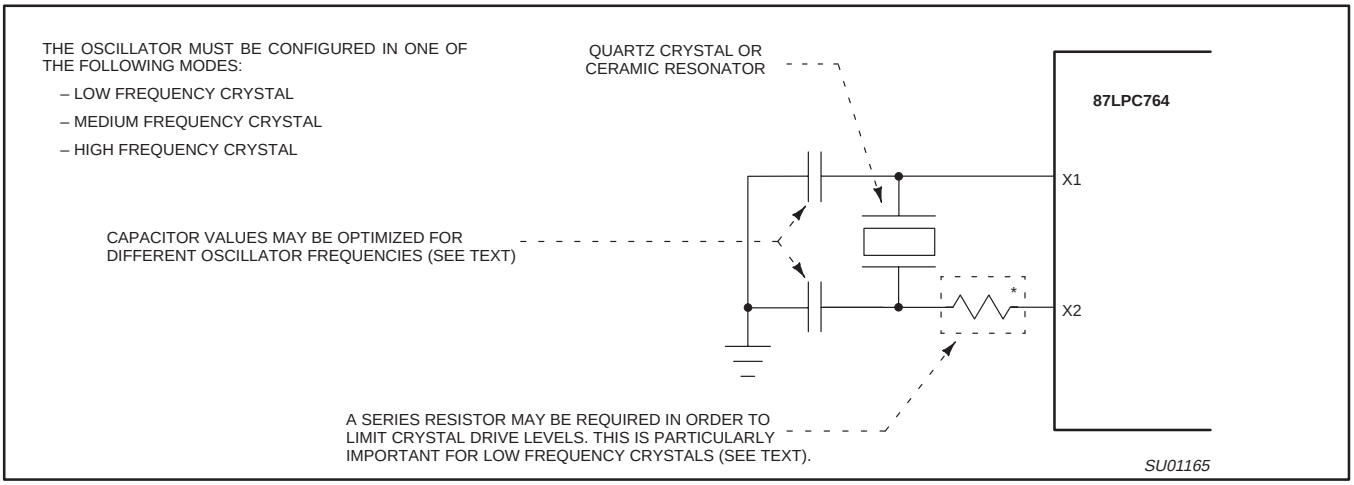

Figure 16. Using the Crystal Oscillator

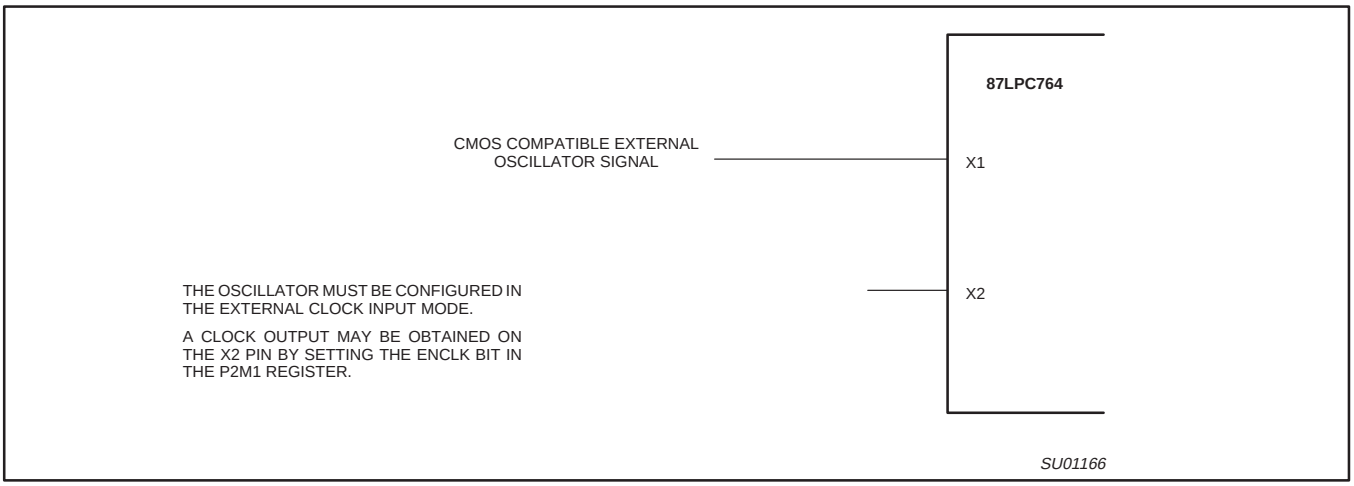

Figure 17. Using an External Clock Input

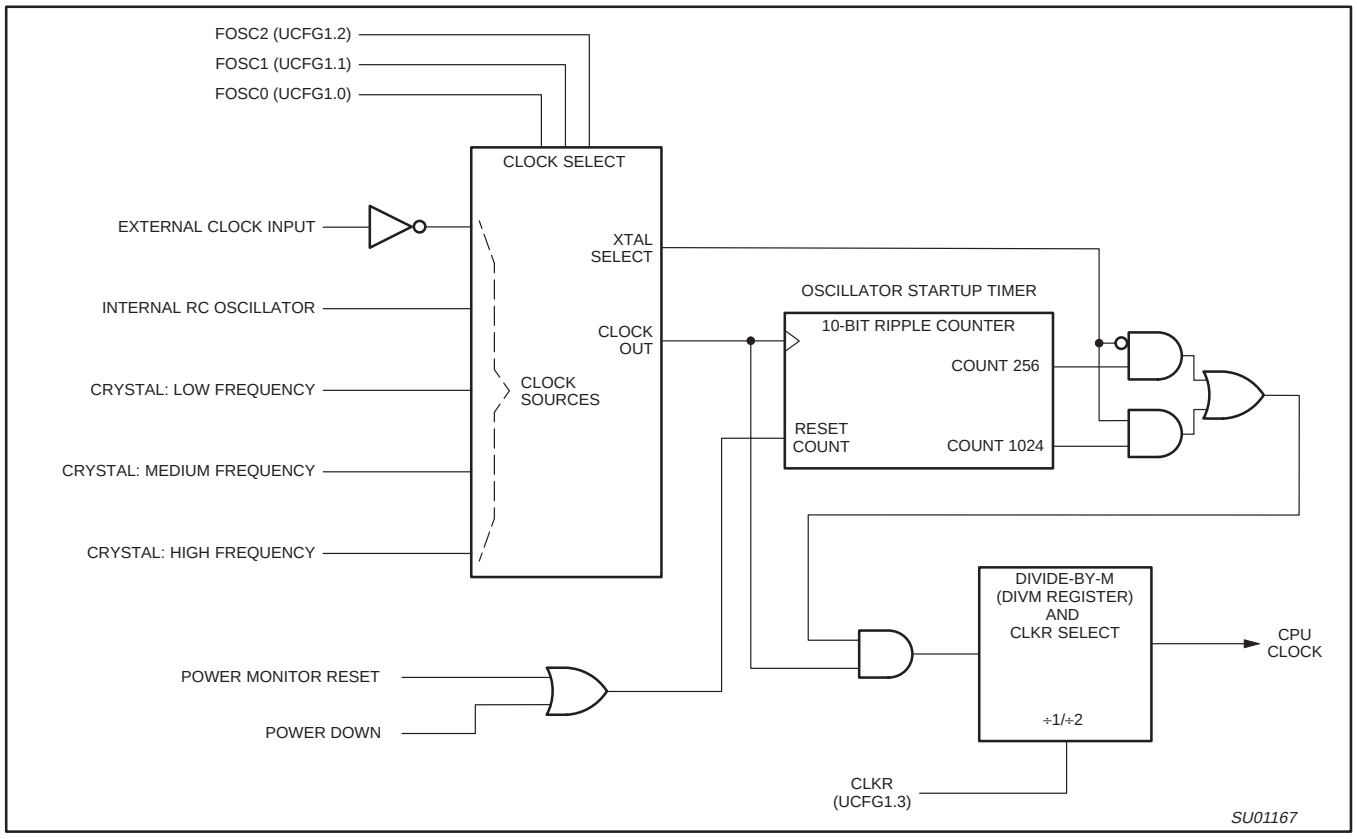

Figure 18. Block Diagram of Oscillator Control

CPU Clock Modification: CLKR and DIVM

For backward compatibility, the CLKR configuration bit allows setting the P87LPC764 instruction and peripheral timing to match standard 80C51 timing by dividing the CPU clock by two. Default timing for the P87LPC764 is 6 CPU clocks per machine cycle while standard 80C51 timing is 12 clocks per machine cycle. This division also applies to peripheral timing, allowing 80C51 code that is oscillator frequency and/or timer rate dependent. The CLKR bit is located in the EPROM configuration register UCFG1, described under EPROM Characteristics

In addition to this, the CPU clock may be divided down from the oscillator rate by a programmable divider, under program control. This function is controlled by the DIVM register. If the DIVM register is set to zero (the default value), the CPU will be clocked by either the unmodified oscillator rate, or that rate divided by two, as determined by the previously described CLKR function.

When the DIVM register is set to some value N (between 1 and 255), the CPU clock is divided by 2 * (N + 1). Clock division values from 4 through 512 are thus possible. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption, in a manner similar to Idle mode. By dividing the clock, the CPU can retain the ability to respond to events other than those that can cause interrupts (i.e. events that allow exiting the Idle mode) by executing its normal program at a lower rate. This can allow bypassing the oscillator startup time in cases where Power Down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

Power Monitoring Functions

The P87LPC764 incorporates power monitoring functions designed to prevent incorrect operation during initial power up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-On Detect and Brownout Detect.

Brownout Detection

The Brownout Detect function allows preventing the processor from failing in an unpredictable manner if the power supply voltage drops below a certain level. The default operation is for a brownout detection to cause a processor reset, however it may alternatively be configured to generate an interrupt by setting the BOI bit in the AUXR1 register (AUXR1.5).

The P87LPC764 allows selection of two Brownout levels: 2.5 V or 3.8 V. When V_{DD} drops below the selected voltage, the brownout detector triggers and remains active until V_{DD} is returns to a level above the Brownout Detect voltage. When Brownout Detect causes a processor reset, that reset remains active as long as V_{DD} remains below the Brownout Detect voltage. When Brownout Detect generates an interrupt, that interrupt occurs once as V_{DD} crosses from above to below the Brownout Detect voltage. For the interrupt to be processed, the interrupt system and the BOI interrupt must both be enabled (via the EA and EBO bits in IEN0).

When Brownout Detect is activated, the BOF flag in the PCON register is set so that the cause of processor reset may be determined by software. This flag will remain set until cleared by software.

For correct activation of Brownout Detect, the V_{DD} fall time must be no faster than 50 mV/µs. When V_{DD} is restored, is should not rise faster than 2 mV/µs in order to insure a proper reset.

The brownout voltage (2.5 V or 3.8 V) is selected via the BOV bit in the EPROM configuration register UCFG1. When unprogrammed (BOV = 1), the brownout detect voltage is 2.5 V. When programmed (BOV = 0), the brownout detect voltage is 3.8 V.

If the Brownout Detect function is not required in an application, it may be disabled, thus saving power. Brownout Detect is disabled by setting the control bit BOD in the AUXR1 register (AUXR1.6).

Power On Detection

The Power On Detect has a function similar to the Brownout Detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where Brownout Detect can work. When this feature is activated, the POF flag in the PCON register is set to indicate an initial power up condition. The POF flag will remain set until cleared by software.

Power Reduction Modes

The P87LPC764 supports Idle and Power Down modes of power reduction.

Idle Mode

The Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or Reset may terminate Idle mode. Idle mode is entered by setting the IDL bit in the PCON register (see Figure 19).

Power Down Mode

The Power Down mode stops the oscillator in order to absolutely minimize power consumption. Power Down mode is entered by setting the PD bit in the PCON register (see Figure 19).

The processor can be made to exit Power Down mode via Reset or one of the interrupt sources shown in Table 5. This will occur if the interrupt is enabled and its priority is higher than any interrupt currently in progress.

In Power Down mode, the power supply voltage may be reduced to the RAM keep-alive voltage V_{RAM}. This retains the RAM contents at the point where Power Down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{RAM}, therefore it is recommended to wake up the processor via Reset in this case. V_{DD} must be raised to within the operating range before the Power Down mode is exited. Since the watchdog timer has a separate oscillator, it may reset the processor upon overflow if it is running during Power Down.

Note that if the Brownout Detect reset is enabled, the processor will be put into reset as soon as V_{DD} drops below the brownout voltage. If Brownout Detect is configured as an interrupt and is enabled, it will wake up the processor from Power Down mode when V_{DD} drops below the brownout voltage.

When the processor wakes up from Power Down mode, it will start the oscillator immediately and begin execution when the oscillator is stable. Oscillator stability is determined by counting 1024 CPU clocks after start-up when one of the crystal oscillator configurations is used, or 256 clocks after start-up for the internal RC or external clock input configurations.

Some chip functions continue to operate and draw power during Power Down mode, increasing the total power used during Power Down. These include the Brownout Detect, Watchdog Timer, and Comparators.

PCON Address: 87h

Not Bit Addressable

Reset Value:
- 30h for a Power On reset
- 20h for a Brownout reset
- 00h for other reset sources

7	6	5	4	3	2	1	0
SMOD1	SMOD0	BOF	POF	GF1	GF0	PD	IDL

BIT	SYMBOL	FUNCTION
PCON.7	SMOD1	When set, this bit doubles the UART baud rate for modes 1, 2, and 3.
PCON.6	SMOD0	This bit selects the function of bit 7 of the SCON SFR. When 0, SCON.7 is the SM0 bit. When 1, SCON.7 is the FE (Framing Error) flag. See Figure 28 for additional information.
PCON.5	BOF	Brown Out Flag. Set automatically when a brownout reset or interrupt has occurred. Also set at power on. Cleared by software. Refer to the Power Monitoring Functions section for additional information.
PCON.4	POF	Power On Flag. Set automatically when a power-on reset has occurred. Cleared by software. Refer to the Power Monitoring Functions section for additional information.
PCON.3	GF1	General purpose flag 1. May be read or written by user software, but has no effect on operation.
PCON.2	GF0	General purpose flag 0. May be read or written by user software, but has no effect on operation.
PCON.1	PD	Power Down control bit. Setting this bit activates Power Down mode operation. Cleared when the Power Down mode is terminated (see text).
PCON.0	IDL	Idle mode control bit. Setting this bit activates Idle mode operation. Cleared when the Idle mode is terminated (see text).

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Figure 19. Power Control Register (PCON)

Table 10. Baud Rates, Timer Values, and CPU Clock Frequencies for SMOD1 = 1

Timer Count	Baud Rate						
	2400	4800	9600	19.2k	38.4k	57.6k	115.2k
–1	0.2304	0.4608	0.9216	* 1.8432	* 3.6864	5.5296	* 11.0592
–2	0.4608	0.9216	* 1.8432	* 3.6864	* 7.3728	* 11.0592	–
–3	0.6912	1.3824	2.7648	5.5296	* 11.0592	16.5888	–
–4	0.9216	* 1.8432	* 3.6864	* 7.3728	* 14.7456	–	–
–5	1.1520	2.3040	4.6080	9.2160	* 18.4320	–	–
–6	1.3824	2.7648	5.5296	* 11.0592	–	–	–
–7	1.6128	3.2256	6.4512	12.9024	–	–	–
–8	* 1.8432	* 3.6864	* 7.3728	* 14.7456	–	–	–
–9	2.0736	4.1472	8.2944	16.5888	–	–	–
–10	2.3040	4.6080	9.2160	* 18.4320	–	–	–
–11	2.5344	5.0688	10.1376	–	–	–	–
–12	2.7648	5.5296	* 11.0592	–	–	–	–
–13	2.9952	5.9904	11.9808	–	–	–	–
–14	3.2256	6.4512	12.9024	–	–	–	–
–15	3.4560	6.9120	13.8240	–	–	–	–
–16	* 3.6864	* 7.3728	* 14.7456	–	–	–	–
–17	3.9168	7.8336	15.6672	–	–	–	–
–18	4.1472	8.2944	16.5888	–	–	–	–
–19	4.3776	8.7552	17.5104	–	–	–	–
–20	4.6080	9.2160	* 18.4320	–	–	–	–
–21	4.8384	9.6768	19.3536	–	–	–	–

NOTES TO TABLES 9 AND 10:

1. Tables 6 and 7 apply to UART modes 1 and 3 (variable rate modes), and show CPU clock rates in MHz for standard baud rates from 2400 to 115.2k baud.
2. Table 6 shows timer settings and CPU clock rates with the SMOD1 bit in the PCON register = 0 (the default after reset), while Table 7 reflects the SMOD1 bit = 1.
3. The tables show all potential CPU clock frequencies up to 20 MHz that may be used for baud rates from 9600 baud to 115.2k baud. Other CPU clock frequencies that would give only lower baud rates are not shown.
4. Table entries marked with an asterisk (*) indicate standard crystal and ceramic resonator frequencies that may be obtained from many sources without special ordering.

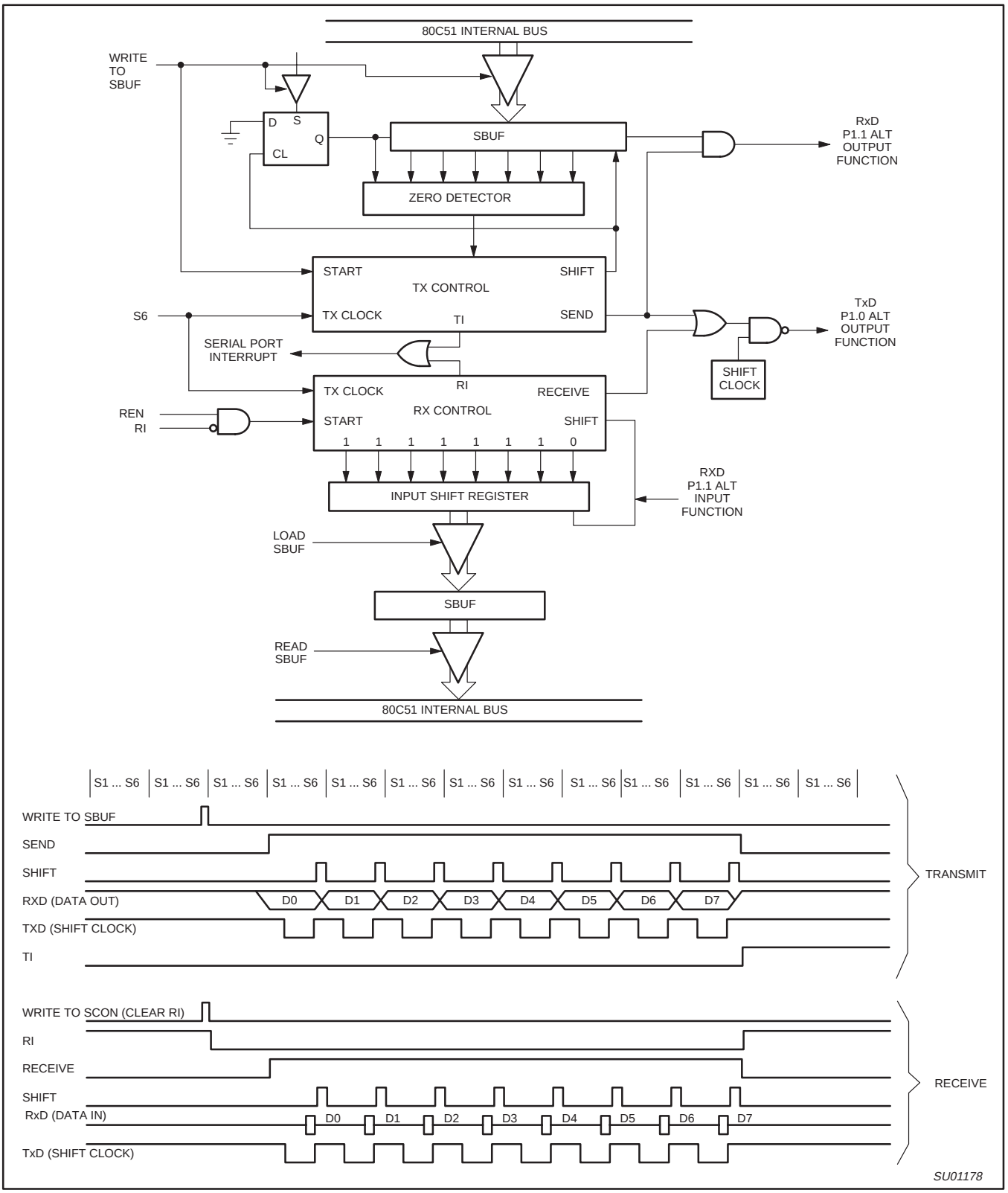

Figure 29. Serial Port Mode 0

EPROM Characteristics

Programming of the EPROM on the P87LPC764 is accomplished with a serial programming method. Commands, addresses, and data are transmitted to and from the device on two pins after programming mode is entered. Serial programming allows easy implementation of In-System Programming of the P87LPC764 in an application board. Details of In-System Programming can be found in application note AN466.

The P87LPC764 contains three signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes designate the device as an P87LPC764 manufactured by Philips. The signature bytes may be read by the user program at addresses FC30h, FC31h and FC60h with the MOVC instruction, using the DPTR register for addressing.

A special user data area is also available for access via the MOVC instruction at addresses FCE0h through FCFFh. This “customer code” space is programmed in the same manner as the main code EPROM and may be used to store a serial number, manufacturing date, or other application information.

32-Byte Customer Code Space

A small supplemental EPROM space is reserved for use by the customer in order to identify code revisions, store checksums, add a serial number to each device, or any other desired use. This area exists in the code memory space from addresses FCE0h through FCFFh. Code execution from this space is not supported, but it may be read as data through the use of the MOVC instruction with the appropriate addresses. The memory may be programmed at the same time as the rest of the code memory and UCFG bytes are programmed.

System Configuration Bytes

A number of user configurable features of the P87LPC764 must be defined at power up and therefore cannot be set by the program after start of execution. Those features are configured through the use of two EPROM bytes that are programmed in the same manner as the EPROM program space. The contents of the two configuration bytes, UCFG1 and UCFG2, are shown in Figures 36 and 37. The values of these bytes may be read by the program through the use of the MOVX instruction at the addresses shown in the figure.

UCFG1 Address: FD00h Unprogrammed Value: FFh

7	6	5	4	3	2	1	0
WDTE	RPD	PRHI	BOV	CLKR	FOSC2	FOSC1	FOSC0

BIT	SYMBOL	FUNCTION
UCFG1.7	WDTE	Watchdog timer enable. When programmed (0), disables the watchdog timer. The timer may still be used to generate an interrupt.
UCFG1.6	RPD	Reset pin disable. When 1 disables the reset function of pin P1.5, allowing it to be used as an input only port pin.
UCFG1.5	PRHI	Port reset high. When 1, ports reset to a high state. When 0, ports reset to a low state.
UCFG1.4	BOV	Brownout voltage select. When 1, the brownout detect voltage is 2.5V. When 0, the brownout detect voltage is 3.8V. This is described in the Power Monitoring Functions section.
UCFG1.3	CLKR	Clock rate select. When 0, the CPU clock rate is divided by 2. This results in machine cycles taking 12 CPU clocks to complete as in the standard 80C51. For full backward compatibility, this division applies to peripheral timing as well.
UCFG1.2–0	FOSC2–FSOC0	CPU oscillator type select. See Oscillator section for additional information. Combinations other than those shown below should not be used. They are reserved for future use.
	FOSC2–FOSC0	Oscillator Configuration
	1 1 1	External clock input on X1 (default setting for an unprogrammed part).
	0 1 1	Internal RC oscillator, 6 MHz. For tolerance, see AC Electrical Characteristics table.
	0 1 0	Low frequency crystal, 20 kHz to 100 kHz.
	0 0 1	Medium frequency crystal or resonator, 100 kHz to 4 MHz.
	0 0 0	High frequency crystal or resonator, 4 MHz to 20 MHz.

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Figure 36. EPROM System Configuration Byte 1 (UCFG1)

UCFG2 Address: FD01h Unprogrammed Value: FFh

7	6	5	4	3	2	1	0
SB2	SB1	—	—	—	—	—	—

BIT	SYMBOL	FUNCTION
UCFG2.7, 6	SB2, SB1	EPROM security bits. See table entitled, “EPROM Security Bits” for details.
UCFG2.5–0	—	Reserved for future use.

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Figure 37. EPROM System Configuration Byte 2 (UCFG2)

Security Bits
When neither of the security bits are programmed, the code in the EPROM can be verified. When only security bit 1 is programmed, all further programming of the EPROM is disabled. At that point, only security bit 2 may still be programmed. When both security bits are programmed, EPROM verify is also disabled.

Table 11. EPROM Security Bits

SB2	SB1	Protection Description
1	1	Both security bits unprogrammed. No program security features enabled. EPROM is programmable and verifiable.
1	0	Only security bit 1 programmed. Further EPROM programming is disabled. Security bit 2 may still be programmed.
0	1	Only security bit 2 programmed. This combination is not supported.
0	0	Both security bits programmed. All EPROM verification and programming are disabled.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Operating temperature under bias	–55 to +125	°C
Storage temperature range	–65 to +150	°C
Voltage on $\overline{RST}/V_{PP}$ pin to V_{SS}	0 to +11.0	V
Voltage on any other pin to V_{SS}	–0.5 to V_{DD}+0.5V	V
Maximum I_{OL} per I/O pin	20	mA
Power dissipation (based on package heat transfer, not device power consumption)	1.5	W

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification are not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.

DC ELECTRICAL CHARACTERISTICS (FOR P87LPC764BD, BN, BDH, FN, FD, FDH, BD/01, BDH/01)

V_{DD} = 2.7 V to 6.0 V unless otherwise specified; T_{amb} = 0°C to +70°C or –40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
I_{DD}	Power supply current, operating	5.0 V, 20 MHz[11]		15	25	mA
		3.0 V, 10 MHz[11]		4	7	mA
I_{ID}	Power supply current, Idle mode	5.0 V, 20 MHz[11]		6	10	mA
		3.0 V, 10 MHz[11]		2	4	mA
I_{PD}	Power supply current, Power Down mode	5.0 V[11]		1	10	µA
		3.0 V[11]		1	5	µA
V_{RAM}	RAM keep-alive voltage		1.5			V
V_{IL}	Input low voltage (TTL input)	4.0 V < V_{DD} < 6.0 V	–0.5		0.2 V_{DD}–0.1	V
		2.7 V < V_{DD} < 4.0 V	–0.5		0.7	V
V_{IL1}	Negative going threshold (Schmitt input)		–0.5		0.3 V_{DD}	V
V_{IH}	Input high voltage (TTL input)		0.2 V_{DD}+0.9		V_{DD}+0.5	V
V_{IH1}	Positive going threshold (Schmitt input)		0.7 V_{DD}		V_{DD}+0.5	V
HYS	Hysteresis voltage			0.2 V_{DD}		V
V_{OL}	Output low voltage all ports[5, 9]	I_{OL} = 3.2 mA, V_{DD} = 2.7 V			0.4	V
V_{OL1}	Output low voltage all ports[5, 9]	I_{OL} = 20 mA, V_{DD} = 2.7 V			1.0	V
V_{OH}	Output high voltage, all ports[3]	I_{OH} = –20 µA, V_{DD} = 2.7 V	V_{DD}–0.7			V
		I_{OH} = –30 µA, V_{DD} = 4.5 V	V_{DD}–0.7			V
V_{OH1}	Output high voltage, all ports[4]	I_{OH} = –1.0 mA, V_{DD} = 2.7 V	V_{DD}–0.7			V
C_{IO}	Input/Output pin capacitance[10]				15	pF
I_{IL}	Logical 0 input current, all ports[8]	V_{IN} = 0.4 V			–50	µA
I_{LI}	Input leakage current, all ports[7]	V_{IN} = V_{IL} or V_{IH}			±2	µA
I_{TL}	Logical 1 to 0 transition current, all ports[3, 6]	V_{IN} = 1.5 V at V_{DD} = 3.0 V	–30		–250	µA
		V_{IN} = 2.0 V at V_{DD} = 5.5 V	–150		–650	µA
R_{RST}	Internal reset pull-up resistor[14]		40		225	kΩ
V_{BOLOW}	Brownout trip voltage with BOV = 1[12]		2.35		2.69	V
V_{BOHI}	Brownout trip voltage with BOV = 0		3.45		3.99	V
V_{REF}	Reference voltage		1.11	1.26	1.41	V
t_C (V_{REF})	Temperature coefficient			tbd		ppm/°C
SS	Supply sensitivity			tbd		%/V

NOTES:

1. Typical ratings are not guaranteed. The values listed are at room temperature, 5 V.
2. See other Figures for details.
   Active mode: $I_{CC(MAX)}$ = tbd
   Idle mode: $I_{CC(MAX)}$ = tbd
3. Ports in quasi-bidirectional mode with weak pull-up (applies to all port pins with pull-ups). Does not apply to open drain pins.
4. Ports in PUSH-PULL mode. Does not apply to open drain pins.
5. In all output modes except high impedance mode.
6. Port pins source a transition current when used in quasi-bidirectional mode and externally driven from 1 to 0. This current is highest when V_{IN} is approximately 2 V.
7. Measured with port in high impedance mode. Parameter is guaranteed but not tested at cold temperature.
8. Measured with port in quasi-bidirectional mode.
9. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 20 mA
   Maximum total I_{OL} for all outputs: 80 mA
   Maximum total I_{OH} for all outputs: 5 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
10. Pin capacitance is characterized but not tested.
11. The I_{DD}, I_{ID}, and I_{PD} specifications are measured using an external clock with the following functions disabled: comparators, brownout detect, and watchdog timer. For V_{DD} = 3 V, LPEP = 1. Refer to the appropriate figures on the following pages for additional current drawn by each of these functions and detailed graphs for other frequency and voltage combinations.
12. Devices initially operating at V_{DD} = 2.7V or above and at f_{OSC} = 10 MHz or less are guaranteed to continue to execute instructions correctly at the brownout trip point. Initial power-on operation below V_{DD} = 2.7 V is not guaranteed.
13. Devices initially operating at V_{DD} = 4.0 V or above and at f_{OSC} = 20 MHz or less are guaranteed to continue to execute instructions correctly at the brownout trip point. Initial power-on operation below V_{DD} = 4.0 V and F_{OSC} > 10 MHz is not guaranteed.
14. This internal resistor is disconnected if P1.5 is used as a general purpose input pin instead of the reset pin.

COMPARATOR ELECTRICAL CHARACTERISTICS (FOR P87LPC764HDH)

V_{DD} = 4.5 V to 5.5 V; T_{amb} = –40°C to +125°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{IO}	Offset voltage comparator inputs[1]				±20	mV
V_{CR}	Common mode range comparator inputs		0		V_{DD}–0.3	V
CMRR	Common mode rejection ratio[1]				–50	dB
	Response time			250	500	ns
	Comparator enable to output valid				10	µs
I_{IL}	Input leakage current, comparator	$0 < V_{IN} < V_{DD}$			±10	µA

NOTE:
1. This parameter is guaranteed by characterization, but not tested in production.

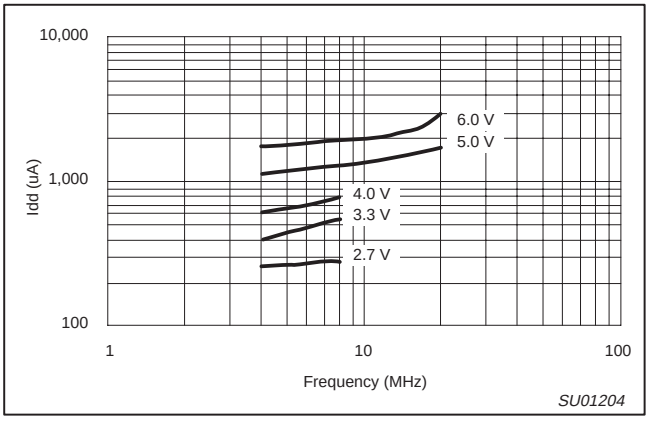


Figure 42. Typical Idd versus frequency (high frequency oscillator, 25°C)

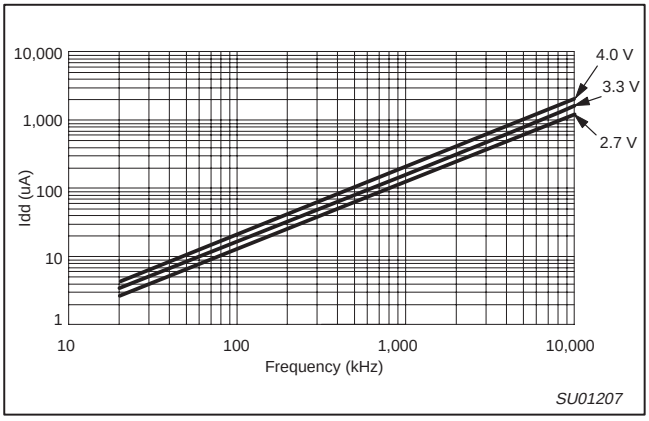


Figure 45. Typical Idle Idd versus frequency (external clock, 25°C, LPEP=1)

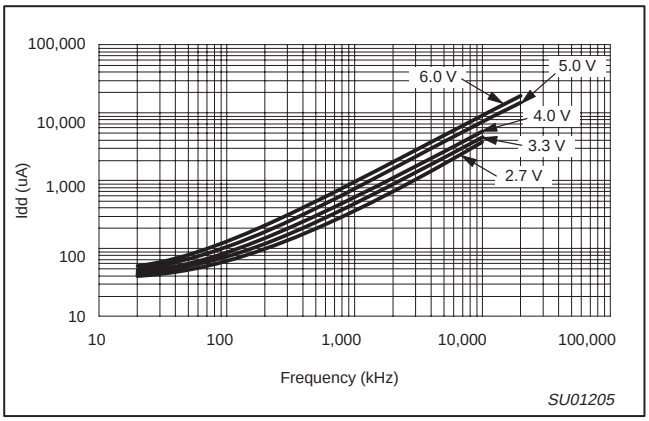


Figure 43. Typical Active Idd versus frequency (external clock, 25°C, LPEP=0)

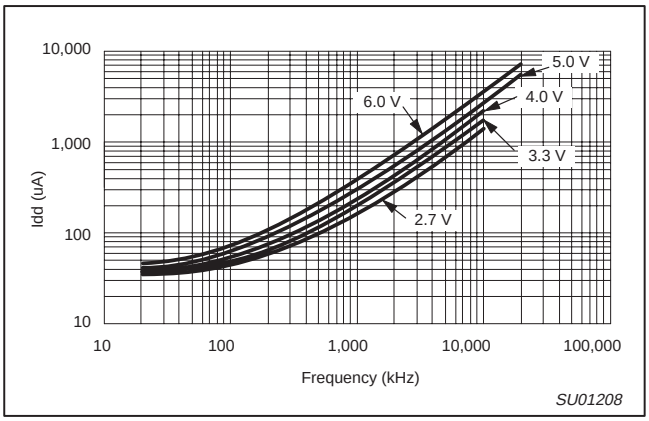


Figure 46. Typical Idle Idd versus frequency (external clock, 25°C, LPEP=0)

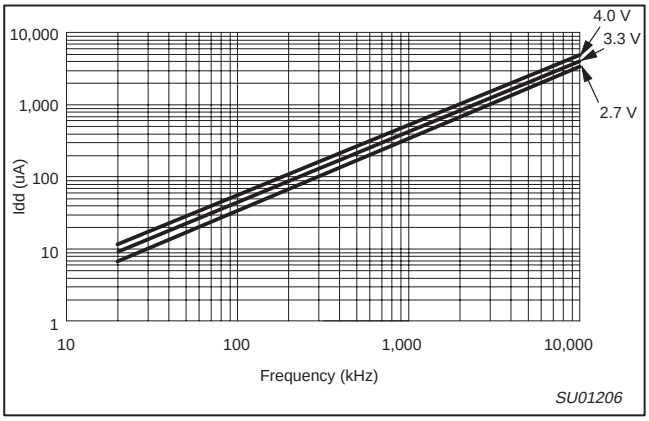
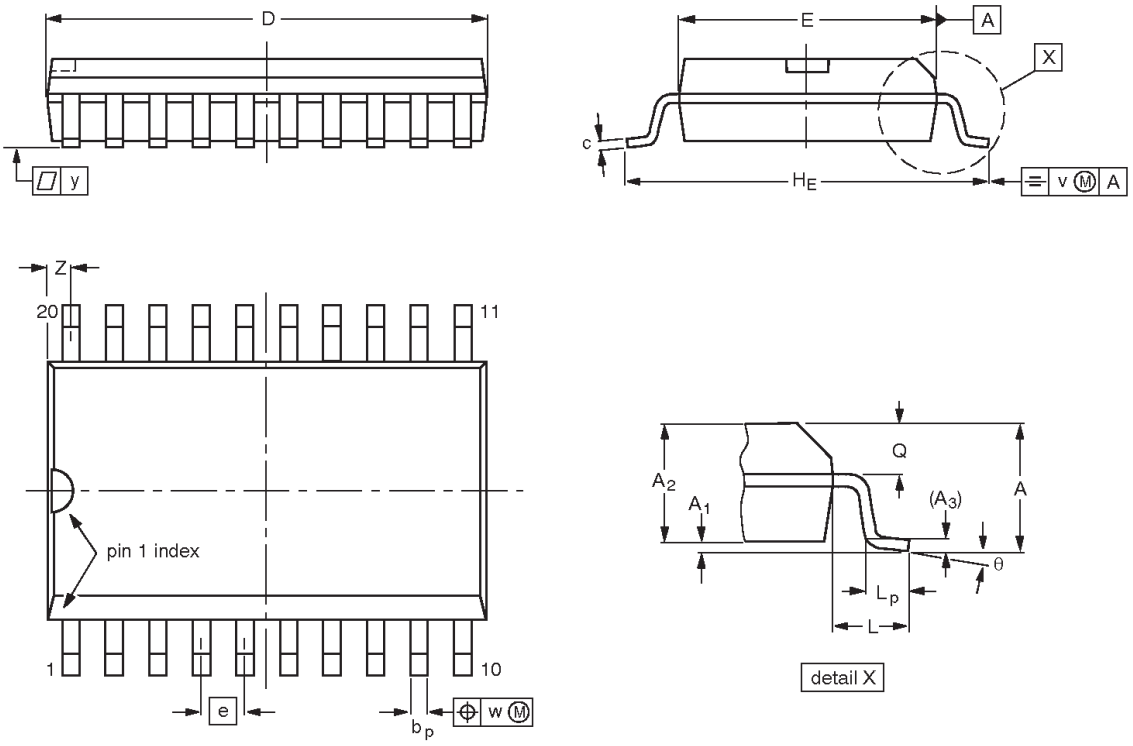
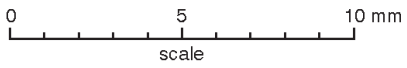


Figure 44. Typical Active Idd versus frequency (external clock, 25°C, LPEP=1)

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19