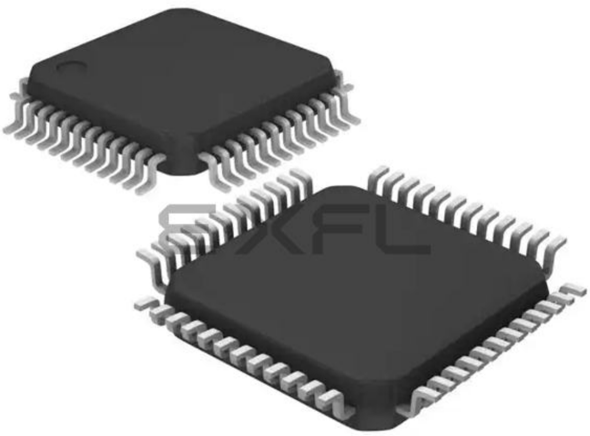

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	SCI
Peripherals	PWM, WDT
Number of I/O	30
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36012fyv

Section 1 Overview

1.1 Features

- High-speed H8/300H central processing unit with an internal 16-bit architecture
  - Upward-compatible with H8/300 CPU on an object level
  - Sixteen 16-bit general registers
  - 62 basic instructions
- Various peripheral functions
  - Timer V (8-bit timer)
  - Timer W (16-bit timer)
  - Watchdog timer
  - SCI3 (Asynchronous or clocked synchronous serial communication interface)
  - 10-bit A/D converter
- On-chip memory

Product Classification		Model: Standard Version	Model: On-Chip Power-On Reset and Low-Voltage Detecting Circuit Version	ROM	RAM
Flash memory version (F-ZTAT™ version)	H8/36024F	HD64F36024	HD64F36024G	32 kbytes	2,048 bytes
	H8/36022F	HD64F36022	HD64F36022G	16 kbytes	2,048 bytes
	H8/36014F	HD64F36014	HD64F36014G	32 kbytes	2,048 bytes
	H8/36012F	HD64F36012	HD64F36012G	16 kbytes	2,048 bytes
Masked ROM version	H8/36024	HD64336024	HD64336024G	32 kbytes	1,024 bytes
	H8/36023	HD64336023	HD64336023G	24 kbytes	1,024 bytes
	H8/36022	HD64336022	HD64336022G	16 kbytes	512 bytes
	H8/36014	HD64336014	HD64336014G	32 kbytes	1,024 bytes
	H8/36013	HD64336013	HD64336013G	24 kbytes	1,024 bytes
	H8/36012	HD64336012	HD64336012G	16 kbytes	512 bytes
	H8/36011	HD64336011	HD64336011G	12 kbytes	512 bytes
	H8/36010	HD64336010	HD64336010G	8 kbytes	512 bytes

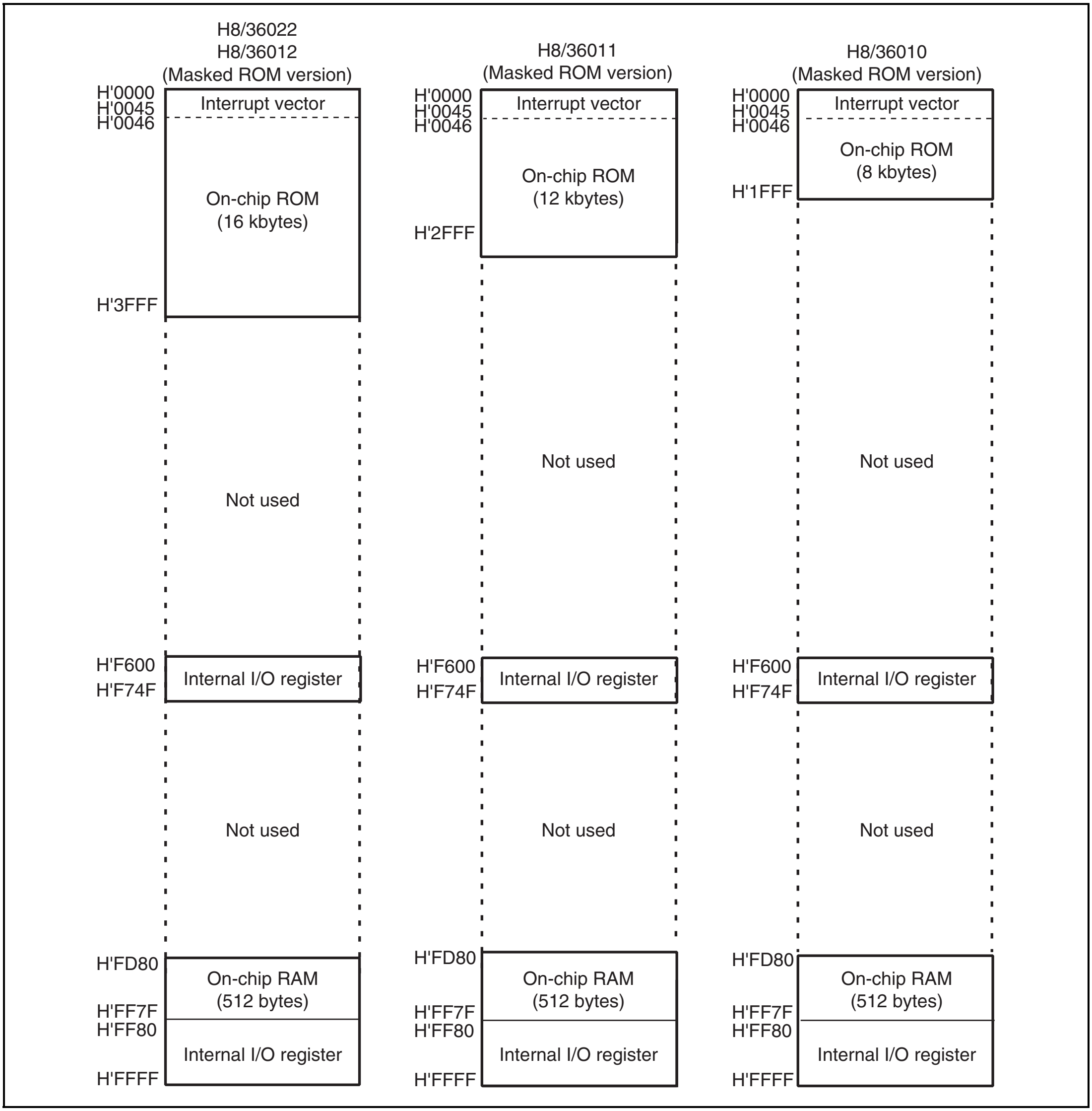


Figure 2.1 Memory Map (2)

3.2.4 Interrupt Flag Register 1 (IRR1)

IRR1 is a status flag register for direct transition interrupts, and $\overline{\text{IRQ3}}$ and $\overline{\text{IRQ0}}$ interrupt requests.

Bit	Bit Name	Initial Value	R/W	Description
7	IRRDT	0	R/W	Direct Transfer Interrupt Request Flag [Setting condition] When a direct transfer is made by executing a SLEEP instruction while DTON in SYSCR2 is set to 1. [Clearing condition] When IRRDT is cleared by writing 0
6	—	0	—	Reserved This bit is always read as 0.
5, 4	—	All 1	—	Reserved These bits are always read as 1.
3	IRRI3	0	R/W	IRQ3 Interrupt Request Flag [Setting condition] When $\overline{\text{IRQ3}}$ pin is designated for interrupt input and the designated signal edge is detected. [Clearing condition] When IRRI3 is cleared by writing 0
2, 1	—	All 0	—	Reserved These bits are always read as 0.
0	IRRI0	0	R/W	IRQ0 Interrupt Request Flag [Setting condition] When $\overline{\text{IRQ0}}$ pin is designated for interrupt input and the designated signal edge is detected. [Clearing condition] When IRRI0 is cleared by writing 0

4.1.3 Break Address Registers (BARH, BARL)

BARH and BARL are 16-bit read/write registers that set the address for generating an address break interrupt. When setting the address break condition to the instruction execution cycle, set the first byte address of the instruction. The initial value of this register is H'FFFF.

4.1.4 Break Data Registers (BDRH, BDRL)

BDRH and BDRL are 16-bit read/write registers that set the data for generating an address break interrupt. BDRH is compared with the upper 8-bit data bus. BDRL is compared with the lower 8-bit data bus. When memory or registers are accessed by byte, the upper 8-bit data bus is used for even and odd addresses in the data transmission. Therefore, comparison data must be set in BDRH for byte access. For word access, the data bus used depends on the address. See section 4.1.1, Address Break Control Register (ABRKCR), for details. The initial value of this register is undefined.

4.2 Operation

When the ABIF and ABIE bits in ABRKSR are set to 1, the address break function generates an interrupt request to the CPU. The ABIF bit in ABRKSR is set to 1 by the combination of the address set in BAR, the data set in BDR, and the conditions set in ABRKCR. When the interrupt request is accepted, interrupt exception handling starts after the instruction being executed ends. The address break interrupt is not masked because of the I bit in CCR of the CPU.

Figures 4.2 show the operation examples of the address break interrupt setting.

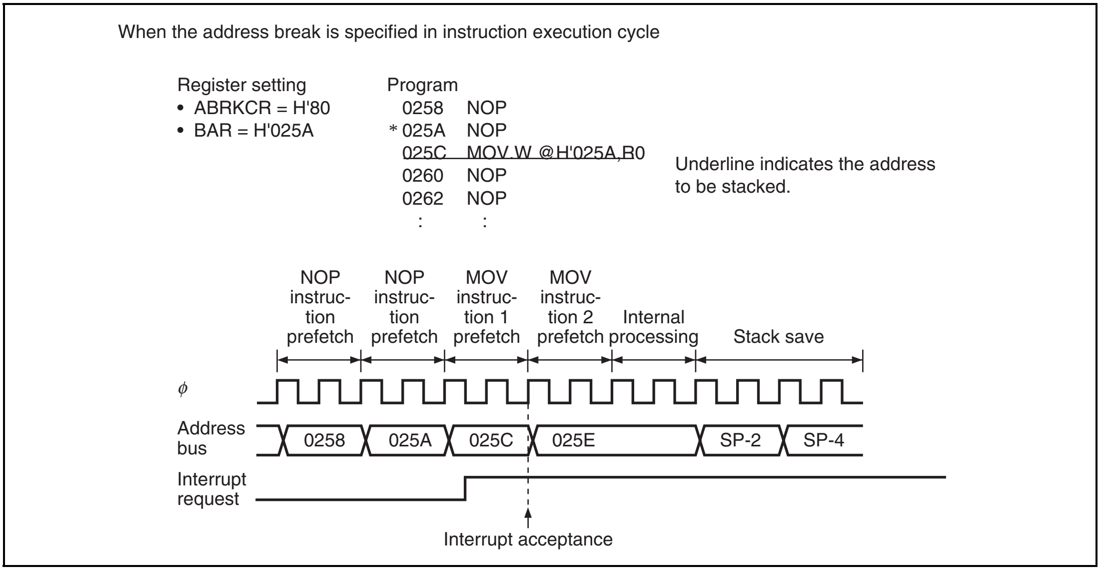


Figure 4.2 Address Break Interrupt Operation Example (1)

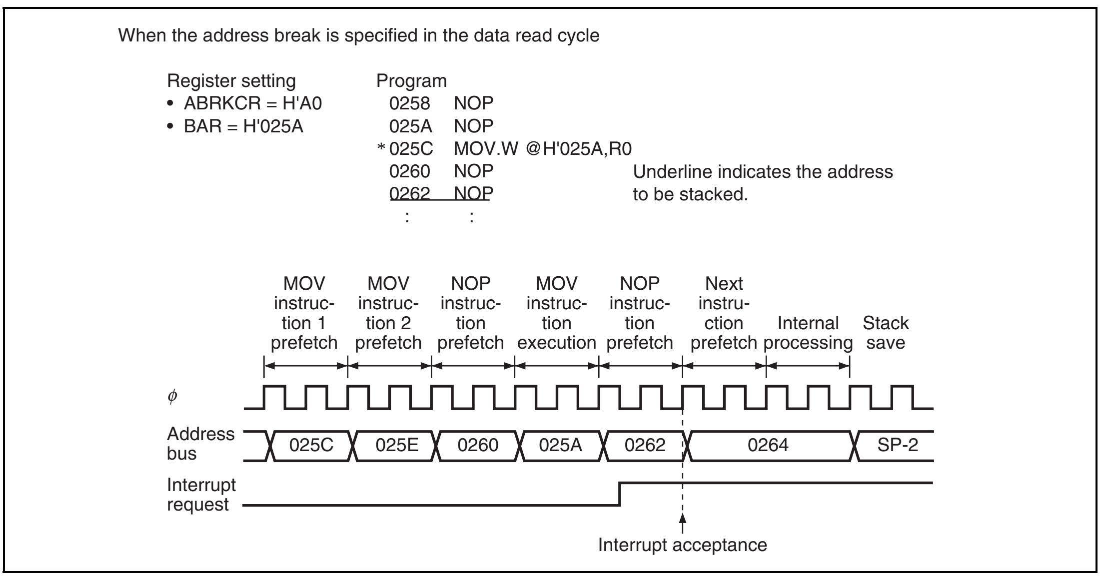


Figure 4.2 Address Break Interrupt Operation Example (2)

7.2 Register Descriptions

The flash memory has the following registers.

- Flash memory control register 1 (FLMCR1)
- Flash memory control register 2 (FLMCR2)
- Erase block register 1 (EBR1)
- Flash memory enable register (FENR)

7.2.1 Flash Memory Control Register 1 (FLMCR1)

FLMCR1 is a register that makes the flash memory change to program mode, program-verify mode, erase mode, or erase-verify mode. For details on register setting, refer to section 7.4, Flash Memory Programming/Erasing.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	—	Reserved This bit is always read as 0.
6	SWE	0	R/W	Software Write Enable When this bit is set to 1, flash memory programming/erasing is enabled. When this bit is cleared to 0, other FLMCR1 register bits and all EBR1 bits cannot be set.
5	ESU	0	R/W	Erase Setup When this bit is set to 1, the flash memory changes to the erase setup state. When it is cleared to 0, the erase setup state is cancelled. Set this bit to 1 before setting the E bit to 1 in FLMCR1.
4	PSU	0	R/W	Program Setup When this bit is set to 1, the flash memory changes to the program setup state. When it is cleared to 0, the program setup state is cancelled. Set this bit to 1 before setting the P bit in FLMCR1.
3	EV	0	R/W	Erase-Verify When this bit is set to 1, the flash memory changes to erase-verify mode. When it is cleared to 0, erase-verify mode is cancelled.

9.4.1 Port Control Register 7 (PCR7)

PCR7 selects inputs/outputs in bit units for pins to be used as general I/O ports of port 7.

Bit	Bit Name	Initial Value	R/W	Description
7	—	—	—	Reserved
6	PCR76	0	W	Setting a PCR7 bit to 1 makes the corresponding pin an output port, while clearing the bit to 0 makes the pin an input port. Note that the TCSRV setting of the timer V has priority for deciding input/output direction of the P76/TMOV pin.
5	PCR75	0	W	
4	PCR74	0	W	
3	PCR73	0	W	
2	PCR72	0	W	
1	PCR71	0	W	
0	PCR70	0	W	

9.4.2 Port Data Register 7 (PDR7)

PDR7 is a general I/O port data register of port 7.

Bit	Bit Name	Initial Value	R/W	Description
7	—	1	—	Reserved This bit is always read as 1.
6	P76	0	R/W	PDR7 stores output data for port 7 pins. If PDR7 is read while PCR7 bits are set to 1, the value stored in PDR7 is read. If PDR7 is read while PCR7 bits are cleared to 0, the pin states are read regardless of the value stored in PDR7.
5	P75	0	R/W	
4	P74	0	R/W	
3	P73	0	R/W	
2	P72	0	R/W	
1	P71	0	R/W	
0	P70	0	R/W	

10.4 Operation

10.4.1 Timer V Operation

1. According to table 10.2, six internal/external clock signals output by prescaler S can be selected as the timer V operating clock signals. When the operating clock signal is selected, TCNTV starts counting-up. Figure 10.2 shows the count timing with an internal clock signal selected, and figure 10.3 shows the count timing with both edges of an external clock signal selected.
2. When TCNTV overflows (changes from H'FF to H'00), the overflow flag (OVF) in TCRV0 will be set. The timing at this time is shown in figure 10.4. An interrupt request is sent to the CPU when OVIE in TCRV0 is 1.
3. TCNTV is constantly compared with TCORA and TCORB. Compare match flag A or B (CMFA or CMFB) is set to 1 when TCNTV matches TCORA or TCORB, respectively. The compare-match signal is generated in the last state in which the values match. Figure 10.5 shows the timing. An interrupt request is generated for the CPU when CMIEA or CMIEB in TCRV0 is 1.
4. When a compare match A or B is generated, the TMOV responds with the output value selected by bits OS3 to OS0 in TCSRV. Figure 10.6 shows the timing when the output is toggled by compare match A.
5. When CCLR1 or CCLR0 in TCRV0 is 01 or 10, TCNTV can be cleared by the corresponding compare match. Figure 10.7 shows the timing.
6. When CCLR1 or CCLR0 in TCRV0 is 11, TCNTV can be cleared by the rising edge of the input of TMRIV pin. A TMRIV input pulse-width of at least 1.5 system clocks is necessary. Figure 10.8 shows the timing.
7. When a counter-clearing source is generated with TRGE in TCRV1 set to 1, the counting-up is halted as soon as TCNTV is cleared. TCNTV resumes counting-up when the edge selected by TVEG1 or TVEG0 in TCRV1 is input from the TGRV pin.

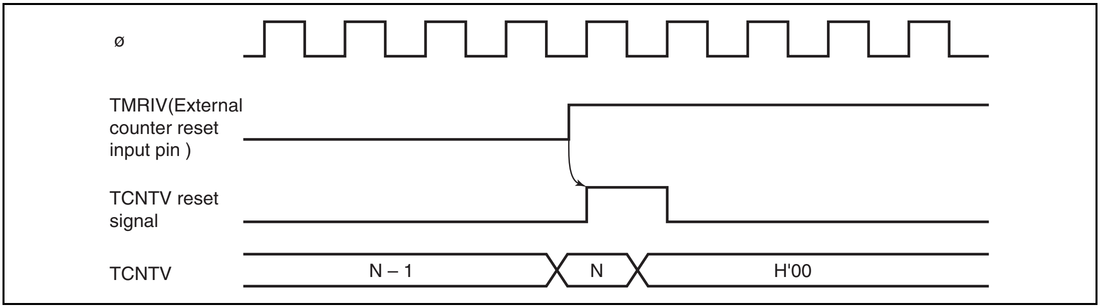


Figure 10.8 Clear Timing by TMRIV Input

11.3.7 Timer Counter (TCNT)

TCNT is a 16-bit readable/writable up-counter. The clock source is selected by bits CKS2 to CKS0 in TCRW. TCNT can be cleared to H'0000 through a compare match with GRA by setting the CCLR in TCRW to 1. When TCNT overflows (changes from H'FFFF to H'0000), the OVF flag in TSRW is set to 1. If OVIE in TIERW is set to 1 at this time, an interrupt request is generated. TCNT must always be read or written in 16-bit units; 8-bit access is not allowed. TCNT is initialized to H'0000 by a reset.

11.3.8 General Registers A to D (GRA to GRD)

Each general register is a 16-bit readable/writable register that can function as either an output-compare register or an input-capture register. The function is selected by settings in TIOR0 and TIOR1.

When a general register is used as an input-compare register, its value is constantly compared with the TCNT value. When the two values match (a compare match), the corresponding flag (IMFA, IMFB, IMFC, or IMFD) in TSRW is set to 1. An interrupt request is generated at this time, when IMIEA, IMIEB, IMIEC, or IMIED is set to 1. Compare match output can be selected in TIOR.

When a general register is used as an input-capture register, an external input-capture signal is detected and the current TCNT value is stored in the general register. The corresponding flag (IMFA, IMFB, IMFC, or IMFD) in TSRW is set to 1. If the corresponding interrupt-enable bit (IMIEA, IMIEB, IMIEC, or IMIED) in TSRW is set to 1 at this time, an interrupt request is generated. The edge of the input-capture signal is selected in TIOR.

GRC and GRD can be used as buffer registers of GRA and GRB, respectively, by setting BUFEA and BUFEB in TMRW.

For example, when GRA is set as an output-compare register and GRC is set as the buffer register for GRA, the value in the buffer register GRC is sent to GRA whenever compare match A is generated.

When GRA is set as an input-capture register and GRC is set as the buffer register for GRA, the value in TCNT is transferred to GRA and the value in the buffer register GRC is transferred to GRA whenever an input capture is generated.

GRA to GRD must be written or read in 16-bit units; 8-bit access is not allowed. GRA to GRD are initialized to H'FFFF by a reset.

14.3.2 A/D Control/Status Register (ADCSR)

ADCSR consists of the control bits and conversion end status bits of the A/D converter.

Bit	Bit Name	Initial Value	R/W	Description
7	ADF	0	R/W	A/D End Flag [Setting conditions] • When A/D conversion ends in single mode • When A/D conversion ends on all the channels selected in scan mode [Clearing conditions] • When 0 is written after reading ADF = 1
6	ADIE	0	R/W	A/D Interrupt Enable A/D conversion end interrupt (ADI) request enabled by ADF when 1 is set
5	ADST	0	R/W	A/D Start Setting this bit to 1 starts A/D conversion. In single mode, this bit is cleared to 0 automatically when conversion on the specified channel is complete. In scan mode, conversion continues sequentially on the specified channels until this bit is cleared to 0 by software, a reset, or a transition to standby mode.
4	SCAN	0	R/W	Scan Mode Selects single mode or scan mode as the A/D conversion operating mode. 0: Single mode 1: Scan mode
3	CKS	0	R/W	Clock Select Selects the A/D conversions time 0: Conversion time = 134 states (max.) 1: Conversion time = 70 states (max.) Clear the ADST bit to 0 before switching the conversion time.

14.5 A/D Conversion Accuracy Definitions

This LSI's A/D conversion accuracy definitions are given below.

- Resolution
  The number of A/D converter digital output codes
- Quantization error
  The deviation inherent in the A/D converter, given by 1/2 LSB (see figure 14.4).
- Offset error
  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from the minimum voltage value 0000000000 to 0000000001 (see figure 14.5).
- Full-scale error
  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from 1111111110 to 1111111111 (see figure 14.5).
- Nonlinearity error
  The error with respect to the ideal A/D conversion characteristics between zero voltage and full-scale voltage. Does not include offset error, full-scale error, or quantization error.
- Absolute accuracy
  The deviation between the digital value and the analog input value. Includes offset error, full-scale error, quantization error, and nonlinearity error.

Table A.2 Operation Code Map (2)

Instruction code:

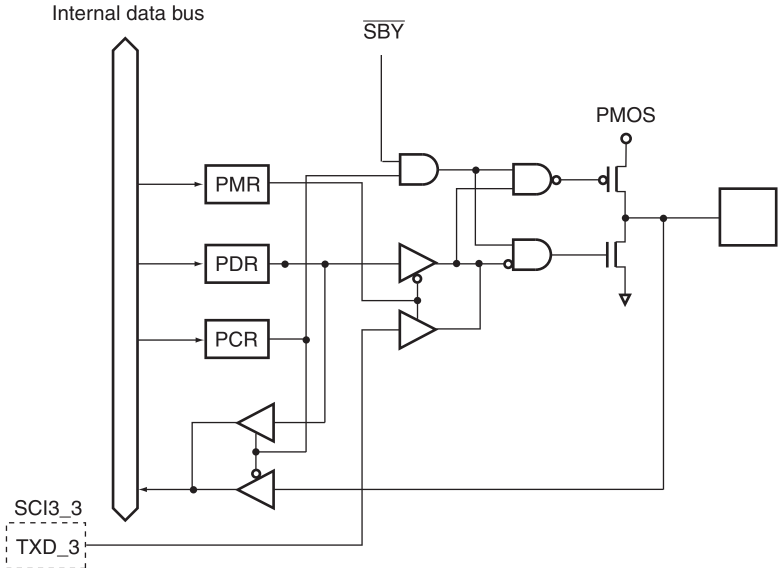
1st byte		2nd byte	
AH	AL	BH	BL

AH AL \ BH	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
01	MOV				LDC/STC				SLEEP				Table A-2 (3)	Table A-2 (3)		Table A-2 (3)
0A	INC								ADD							
0B	ADDS					INC		INC	ADDS					INC		INC
0F	DAA								MOV							
10	SHLL			SHLL					SHAL			SHAL				
11	SHLR			SHLR					SHAR			SHAR				
12	ROTXL			ROTXL					ROTL			ROTL				
13	ROTXR			ROTXR					ROTR			ROTR				
17	NOT			NOT		EXTU		EXTU	NEG			NEG		EXTS		EXTS
1A	DEC								SUB							
1B	SUBS					DEC		DEC	SUB					DEC		DEC
1F	DAS								CMP							
58	BRA	BRN	BHI	BLS	BCC	BCS	BNE	BEQ	BVC	BVS	BPL	BMI	BGE	BLT	BGT	BLE
79	MOV	ADD	CMP	SUB	OR	XOR	AND									
7A	MOV	ADD	CMP	SUB	OR	XOR	AND									

Table A.3 Number of Cycles in Each Instruction

Execution Status (Instruction Cycle)		Access Location	
		On-Chip Memory	On-Chip Peripheral Module
Instruction fetch	S_I	2	—
Branch address read	S_J		
Stack operation	S_K		
Byte data access	S_L		2 or 3*
Word data access	S_M		2 or 3*
Internal operation	S_N	1	

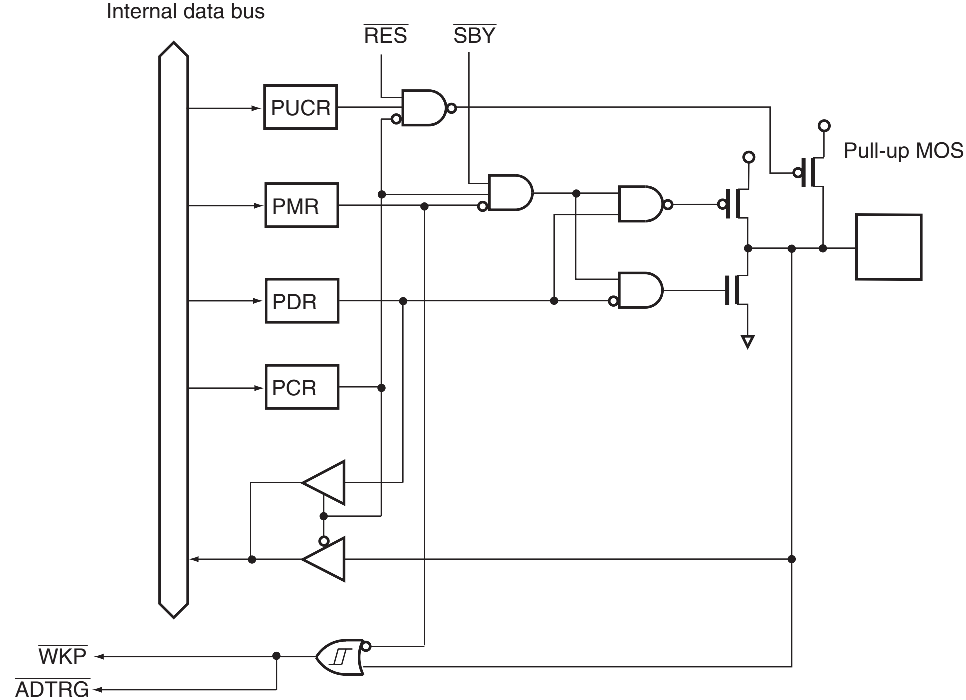
Note: * Depends on which on-chip peripheral module is accessed. See section 17.1, Register Addresses (Address Order).



Legend

PMR: Port mode register
PDR: Port data register
PCR: Port control register

Figure B.10 Port 5 Block Diagram (P57) (H8/36024)



Legend
PUCR: Port pull-up control register
PMR: Port mode register
PDR: Port data register
PCR: Port control register

Figure B.12 Port 5 Block Diagram (P55)

Product Type			Product Code	Model Marking	Package Code
H8/36013	Masked ROM version	Standard product	HD64336013FP	HD64336013(***)FP	LQFP-64 (FP-64E)
			HD64336013FX	HD64336013(***)FX	LQFP-48 (FP-48F)
			HD64336013FY	HD64336013(***)FY	LQFP-48 (FP-48B)
			HD64336013FT	HD64336013(***)FT	QFN-48(TNP-48)
		Product with POR & LVDC	HD64336013GFP	HD64336013G(***)FP	LQFP-64 (FP-64E)
			HD64336013GFX	HD64336013G(***)FX	LQFP-48 (FP-48F)
			HD64336013GFY	HD64336013G(***)FY	LQFP-48 (FP-48B)
			HD64336013GFT	HD64336013G(***)FT	QFN-48(TNP-48)
H8/36012	Flash memory version	Standard product	HD64F36012FP	HD64F36012FP	LQFP-64 (FP-64E)
			HD64F36012FX	HD64F36012FX	LQFP-48 (FP-48F)
			HD64F36012FY	HD64F36012FY	LQFP-48 (FP-48B)
			HD64F36012FT	HD64F36012FT	QFN-48(TNP-48)
		Product with POR & LVDC	HD64F36012GFP	HD64F36012GFP	LQFP-64 (FP-64E)
			HD64F36012GFX	HD64F36012GFX	LQFP-48 (FP-48F)
			HD64F36012GFY	HD64F36012GFY	LQFP-48 (FP-48B)
			HD64F36012GFT	HD64F36012GFT	QFN-48(TNP-48)
	Masked ROM version	Standard product	HD64336012FP	HD64336012(***)FP	LQFP-64 (FP-64E)
			HD64336012FX	HD64336012(***)FX	LQFP-48 (FP-48F)
			HD64336012FY	HD64336012(***)FY	LQFP-48 (FP-48B)
			HD64336012FT	HD64336012(***)FT	QFN-48(TNP-48)
		Product with POR & LVDC	HD64336012GFP	HD64336012G(***)FP	LQFP-64 (FP-64E)
			HD64336012GFX	HD64336012G(***)FX	LQFP-48 (FP-48F)
			HD64336012GFY	HD64336012G(***)FY	LQFP-48 (FP-48B)
			HD64336012GFT	HD64336012G(***)FT	QFN-48(TNP-48)
H8/36011	Masked ROM version	Standard product	HD64336011FP	HD64336011(***)FP	LQFP-64 (FP-64E)
			HD64336011FX	HD64336011(***)FX	LQFP-48 (FP-48F)
			HD64336011FY	HD64336011(***)FY	LQFP-48 (FP-48B)
			HD64336011FT	HD64336011(***)FT	QFN-48(TNP-48)
		Product with POR & LVDC	HD64336011GFP	HD64336011G(***)FP	LQFP-64 (FP-64E)
			HD64336011GFX	HD64336011G(***)FX	LQFP-48 (FP-48F)
			HD64336011GFY	HD64336011G(***)FY	LQFP-48 (FP-48B)
			HD64336011GFT	HD64336011G(***)FT	QFN-48(TNP-48)