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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	SCI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	30
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36012gfpwv

2.2.1 General Registers

The H8/300H CPU has eight 32-bit general registers. These general registers are all functionally identical and can be used as both address registers and data registers. When a general register is used as a data register, it can be accessed as a 32-bit, 16-bit, or 8-bit register. Figure 2.3 illustrates the usage of the general registers. When the general registers are used as 32-bit registers or address registers, they are designated by the letters ER (ER0 to ER7).

The ER registers divide into 16-bit general registers designated by the letters E (E0 to E7) and R (R0 to R7). These registers are functionally equivalent, providing a maximum of sixteen 16-bit registers. The E registers (E0 to E7) are also referred to as extended registers.

The R registers divide into 8-bit registers designated by the letters RH (R0H to R7H) and RL (R0L to R7L). These registers are functionally equivalent, providing a maximum of sixteen 8-bit registers.

The usage of each register can be selected independently.

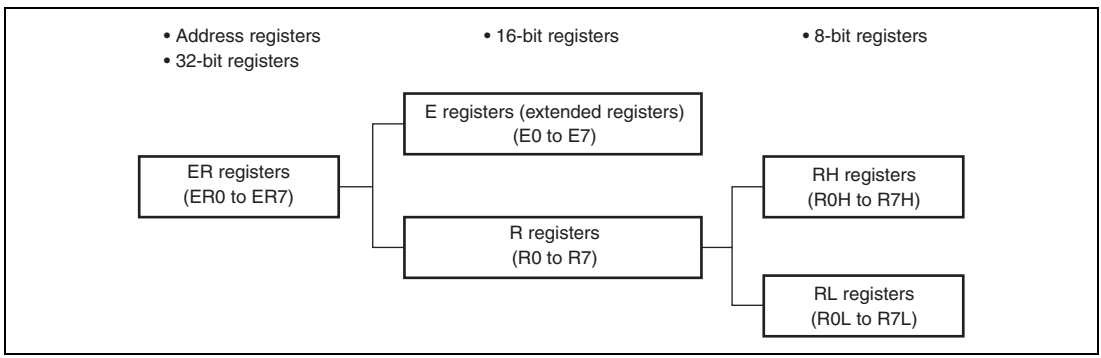


Figure 2.3 Usage of General Registers

General register ER7 has the function of stack pointer (SP) in addition to its general-register function, and is used implicitly in exception handling and subroutine calls. Figure 2.4 shows the stack.

Table 2.7 Branch Instructions

Instruction	Size	Function		
Bcc*	—	Branches to a specified address if a specified condition is true. The branching conditions are listed below.		
		Mnemonic	**Description**	**Condition**
		BRA(BT)	Always (true)	Always
		BRN(BF)	Never (false)	Never
		BHI	High	$C \vee Z = 0$
		BLS	Low or same	$C \vee Z = 1$
		BCC(BHS)	Carry clear (high or same)	$C = 0$
		BCS(BLO)	Carry set (low)	$C = 1$
		BNE	Not equal	$Z = 0$
		BEQ	Equal	$Z = 1$
		BVC	Overflow clear	$V = 0$
		BVS	Overflow set	$V = 1$
		BPL	Plus	$N = 0$
		BMI	Minus	$N = 1$
		BGE	Greater or equal	$N \oplus V = 0$
		BLT	Less than	$N \oplus V = 1$
		BGT	Greater than	$Z \vee (N \oplus V) = 0$
		BLE	Less or equal	$Z \vee (N \oplus V) = 1$
JMP	—	Branches unconditionally to a specified address.		
BSR	—	Branches to a subroutine at a specified address.		
JSR	—	Branches to a subroutine at a specified address.		
RTS	—	Returns from a subroutine		

Note: * Bcc is the general name for conditional branch instructions.

As a result of the BSET instruction, bit 0 in PDR5 becomes 1, and P50 outputs a high-level signal. However, bits 7 and 6 of PDR5 end up with different values. To prevent this problem, store a copy of the PDR5 data in a work area in memory. Perform the bit manipulation on the data in the work area, then write this data to PDR5.

- Prior to executing BSET

```
MOV.B   #80,  R0L
MOV.B   R0L,  @RAM0
MOV.B   R0L,  @PDR5
```

The PDR5 value (H'80) is written to a work area in memory (RAM0) as well as to PDR5.

	P57	**P56**	**P55**	**P54**	**P53**	**P52**	**P51**	**P50**
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1	1
PDR5	1	0	0	0	0	0	0	0
RAM0	1	0	0	0	0	0	0	0

- BSET instruction executed

```
BSET    #0,     @RAM0
```

The BSET instruction is executed designating the PDR5 work area (RAM0).

- After executing BSET

```
MOV.B   @RAM0, R0L
MOV.B   R0L,  @PDR5
```

The work area (RAM0) value is written to PDR5.

	P57	**P56**	**P55**	**P54**	**P53**	**P52**	**P51**	**P50**
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	High level
PCR5	0	0	1	1	1	1	1	1
PDR5	1	0	0	0	0	0	0	1
RAM0	1	0	0	0	0	0	0	1

Section 3 Exception Handling

Exception handling may be caused by a reset, a trap instruction (TRAPA), or interrupts.

- Reset

A reset has the highest exception priority. Exception handling starts as soon as the reset is cleared by the $\overline{\text{RES}}$ pin. The chip is also reset when the watchdog timer overflows, and exception handling starts. Exception handling is the same as exception handling by the $\overline{\text{RES}}$ pin.

- Trap Instruction

Exception handling starts when a trap instruction (TRAPA) is executed. The TRAPA instruction generates a vector address corresponding to a vector number from 0 to 3, as specified in the instruction code. Exception handling can be executed at all times in the program execution state.

- Interrupts

External interrupts other than NMI and internal interrupts other than address break are masked by the I bit in CCR, and kept masked while the I bit is set to 1. Exception handling starts when the current instruction or exception handling ends, if an interrupt request has been issued.

3.1 Exception Sources and Vector Address

Table 3.1 shows the vector addresses and priority of each exception handling. When more than one interrupt is requested, handling is performed from the interrupt with the highest priority.

Table 3.1 Exception Sources and Vector Address

Relative Module	Exception Sources	Vector Number	Vector Address	Priority
$\overline{\text{RES}}$ pin Watchdog timer	Reset	0	H'0000 to H'0001	High
—	Reserved for system use	1 to 6	H'0002 to H'000D	
External interrupt pin	NMI	7	H'000E to H'000F	
CPU	Trap instruction (#0)	8	H'0010 to H'0011	
	(#1)	9	H'0012 to H'0013	
	(#2)	10	H'0014 to H'0015	
	(#3)	11	H'0016 to H'0017	
Address break	Break conditions satisfied	12	H'0018 to H'0019	Low

11.4.2 PWM Operation

In PWM mode, PWM waveforms are generated by using GRA as the period register and GRB, GRC, and GRD as duty registers. PWM waveforms are output from the FTIOB, FTIOC, and FTIOD pins. Up to three-phase PWM waveforms can be output. In PWM mode, a general register functions as an output compare register automatically. The output level of each pin depends on the corresponding timer output level set bit (TOB, TOC, and TOD) in TCRW. When TOB is 1, the FTIOB output goes to 1 at compare match A and to 0 at compare match B. When TOB is 0, the FTIOB output goes to 0 at compare match A and to 1 at compare match B. Thus the compare match output level settings in TIOR0 and TIOR1 are ignored for the output pin set to PWM mode. If the same value is set in the cycle register and the duty register, the output does not change when a compare match occurs.

Figure 11.9 shows an example of operation in PWM mode. The output signals go to 1 and TCNT is cleared at compare match A, and the output signals go to 0 at compare match B, C, and D (TOB, TOC, and TOD = 1: initial output values are set to 1).

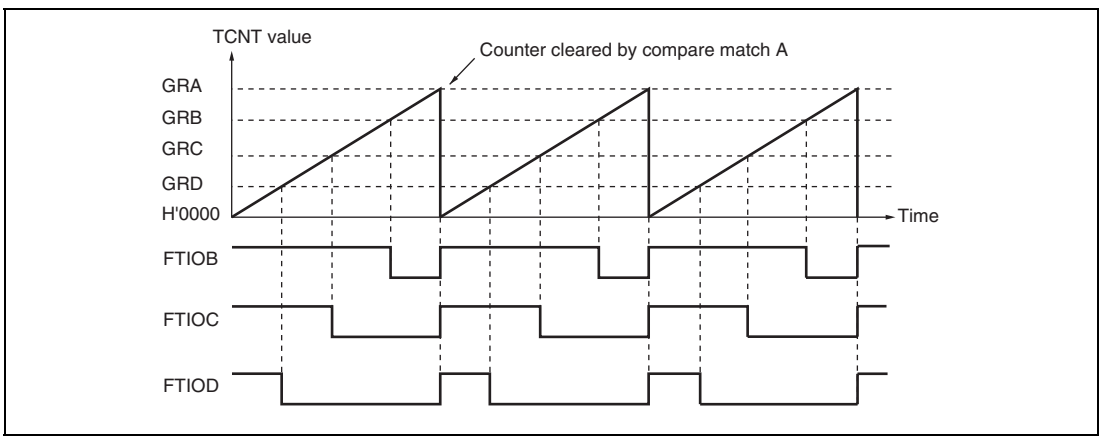


Figure 11.9 PWM Mode Example (1)

Bit	Bit Name	Initial Value	R/W	Description
2	WDON	0	R/W	Watchdog Timer On TCWD starts counting up when WDON is set to 1 and halts when WDON is cleared to 0. [Setting condition] When 1 is written to the WDON bit while writing 0 to the B2WI bit when the TCSRWE bit=1 [Clearing condition] • Reset by $\overline{RES}$ pin • When 0 is written to the WDON bit while writing 0 to the B2WI when the TCSRWE bit=1
1	B0WI	1	R/W	Bit 0 Write Inhibit This bit can be written to the WRST bit only when the write value of the B0WI bit is 0. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Setting condition] When TCWD overflows and an internal reset signal is generated [Clearing condition] • Reset by $\overline{RES}$ pin • When 0 is written to the WRST bit while writing 0 to the B0WI bit when the TCSRWE bit=1

12.2.2 Timer Counter WD (TCWD)

TCWD is an 8-bit readable/writable up-counter. When TCWD overflows from H'FF to H'00, the internal reset signal is generated and the WRST bit in TCSRWD is set to 1. TCWD is initialized to H'00.

14.6 Usage Notes

14.6.1 Permissible Signal Source Impedance

This LSI's analog input is designed such that conversion accuracy is guaranteed for an input signal for which the signal source impedance is 5 kΩ or less. This specification is provided to enable the A/D converter's sample-and-hold circuit input capacitance to be charged within the sampling time; if the sensor output impedance exceeds 5 kΩ, charging may be insufficient and it may not be possible to guarantee A/D conversion accuracy. However, for A/D conversion in single mode with a large capacitance provided externally, the input load will essentially comprise only the internal input resistance of 10 kΩ, and the signal source impedance is ignored. However, as a low-pass filter effect is obtained in this case, it may not be possible to follow an analog signal with a large differential coefficient (e.g., 5 mV/µs or greater) (see figure 14.6). When converting a high-speed analog signal or converting in scan mode, a low-impedance buffer should be inserted.

14.6.2 Influences on Absolute Accuracy

Adding capacitance results in coupling with GND, and therefore noise in GND may adversely affect absolute accuracy. Be sure to make the connection to an electrically stable GND.

Care is also required to ensure that filter circuits do not interfere with digital signals or act as antennas on the mounting board.

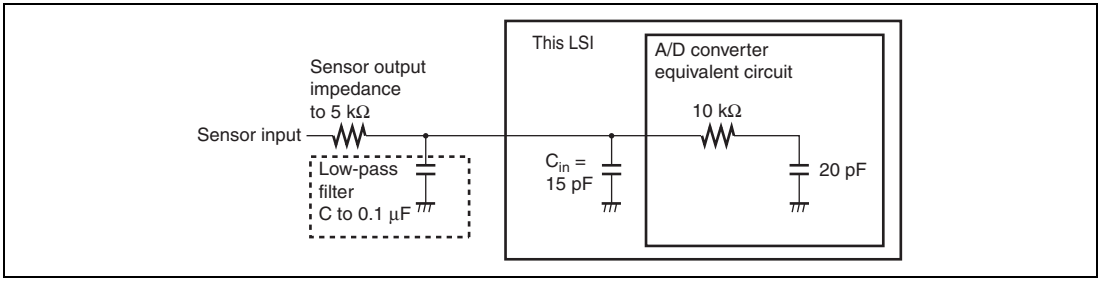


Figure 14.6 Analog Input Circuit Example

18.2.4 A/D Converter Characteristics

Table 18.5 A/D Converter Characteristics

V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C, unless otherwise specified.

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Notes
				Min	Typ	Max		
Analog power supply voltage	AV_{CC}	AV_{CC}		3.3	V_{CC}	5.5	V	*1
Analog input voltage	AV_{IN}	AN3 to AN0		V_{SS} – 0.3	—	AV_{CC} + 0.3	V	
Analog power supply current	AI_{OPE}	AV_{CC}	AV_{CC} = 5.0 V f_{OSC} = 20 MHz	—	—	2.0	mA	
	AI_{STOP1}	AV_{CC}		—	50	—	µA	*2 Reference value
	AI_{STOP2}	AV_{CC}		—	—	5.0	µA	*3
Analog input capacitance	C_{AIN}	AN3 to AN0		—	—	30.0	pF	
Allowable signal source impedance	R_{AIN}	AN3 to AN0		—	—	5.0	kΩ	
Resolution (data length)				10	10	10	bit	
Conversion time (single mode)			AV_{CC} = 3.3 V to 5.5 V	134	—	—	t_{cyc}	
Nonlinearity error				—	—	±7.5	LSB	
Offset error				—	—	±7.5	LSB	
Full-scale error				—	—	±7.5	LSB	
Quantization error				—	—	±0.5	LSB	
Absolute accuracy				—	—	±8.0	LSB	
Conversion time (single mode)			AV_{CC} = 4.0 V to 5.5 V	70	—	—	t_{cyc}	
Nonlinearity error				—	—	±7.5	LSB	
Offset error				—	—	±7.5	LSB	
Full-scale error				—	—	±7.5	LSB	
Quantization error				—	—	±0.5	LSB	
Absolute accuracy				—	—	±8.0	LSB	

Item	Symbol	Applicable Pins	Test Condition	Values Min	Typ	Max	Unit	Notes
Conversion time (single mode)			AV_{CC} = 4.0 V to 5.5 V	134	—	—	t_{cyc}	
Nonlinearity error				—	—	±3.5	LSB	
Offset error				—	—	±3.5	LSB	
Full-scale error				—	—	±3.5	LSB	
Quantization error				—	—	±0.5	LSB	
Absolute accuracy				—	—	±4.0	LSB	

Notes: 1. Set $AV_{CC} = V_{CC}$ when the A/D converter is not used.
2. AI_{STOP1} is the current in active and sleep modes while the A/D converter is idle.
3. AI_{STOP2} is the current at reset and in standby and subsleep modes while the A/D converter is idle.

18.2.5 Watchdog Timer Characteristics

Table 18.6 Watchdog Timer Characteristics

V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C, unless otherwise specified.

Item	Symbol	Applicable Pins	Test Condition	Values Min	Typ	Max	Unit	Notes
On-chip oscillator overflow time	t_{OVF}			0.2	0.4	—	s	*

Note: * Shows the time to count from 0 to 255, at which point an internal reset is generated, when the internal oscillator is selected.

18.2.8 Power-On Reset Circuit Characteristics (Optional)

Table 18.9 Power-On Reset Circuit Characteristics

V_{SS} = 0.0 V, T_a = –20 to +75°C, unless otherwise indicated.

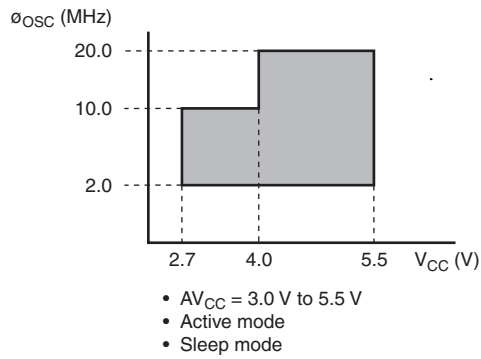
Item	Symbol	Test Condition	Values			Unit
			Min	Typ	Max	
Pull-up resistance of $\overline{RES}$ pin	R_{RES}		100	150	—	kΩ
Power-on reset start voltage*	V_{por}		—	—	100	mV

Note: * The power-supply voltage (Vcc) must fall below Vpor = 100 mV and then rise after charge of the $\overline{RES}$ pin is removed completely. In order to remove charge of the $\overline{RES}$ pin, it is recommended that the diode be placed in the Vcc side. If the power-supply voltage (Vcc) rises from the point over 100 mV, a power-on reset may not occur.

18.3 Electrical Characteristics (Masked ROM Version)

18.3.1 Power Supply Voltage and Operating Ranges

(1) Power Supply Voltage and Oscillation Frequency Range



Item	Symbol	Applicable Pins	Test Condition	Values Min	Typ	Max	Unit	Notes
Pull-up MOS current	$-I_p$	P12 to P10, P17 to P14, P55 to P50	V_{CC} = 5.0 V, V_{IN} = 0.0 V	50.0	—	300.0	µA	
			V_{CC} = 3.0 V, V_{IN} = 0.0 V	—	60.0	—		Reference value
Input capacitance	C_{in}	All input pins except power supply pins	f = 1 MHz, V_{IN} = 0.0 V, T_a = 25°C	—	—	15.0	pF	
Active mode current consumption	I_{OPE1}	V_{CC}	Active mode 1 V_{CC} = 5.0 V, f_{OSC} = 20 MHz	—	15.0	30.0	mA	*2
			Active mode 1 V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	8.0	—		*2 Reference value
	I_{OPE2}	V_{CC}	Active mode 2 V_{CC} = 5.0 V, f_{OSC} = 20 MHz	—	1.8	3.0	mA	*2
			Active mode 2 V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	1.2	—		*2 Reference value
Sleep mode current consumption	I_{SLEEP1}	V_{CC}	Sleep mode 1 V_{CC} = 5.0 V, f_{OSC} = 20 MHz	—	11.5	22.5	mA	*2
			Sleep mode 1 V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	6.5	—		*2 Reference value
	I_{SLEEP2}	V_{CC}	Sleep mode 2 V_{CC} = 5.0 V, f_{OSC} = 20 MHz	—	1.7	2.7	mA	*2
			Sleep mode 2 V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	1.1	—		*2 Reference value
Standby mode current consumption	I_{STBY}	V_{CC}		—	—	5.0	µA	*2

Item	Symbol	Applicable Pins	Test Condition	Values Min	Typ	Max	Unit	Reference Figure
Conversion time (single mode)			AV_{CC} = 4.0 V to 5.5 V	134	—	—	t_{cyc}	
Nonlinearity error				—	—	±3.5	LSB	
Offset error				—	—	±3.5	LSB	
Full-scale error				—	—	±3.5	LSB	
Quantization error				—	—	±0.5	LSB	
Absolute accuracy				—	—	±4.0	LSB	

Notes: 1. Set $AV_{CC} = V_{CC}$ when the A/D converter is not used.
2. AI_{STOP1} is the current in active and sleep modes while the A/D converter is idle.
3. AI_{STOP2} is the current at reset and in standby and subsleep modes while the A/D converter is idle.

18.3.5 Watchdog Timer Characteristics

Table 18.14 Watchdog Timer Characteristics

V_{CC} = 2.7 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C, unless otherwise specified.

Item	Symbol	Applicable Pins	Test Condition	Values Min	Typ	Max	Unit	Notes
On-chip oscillator overflow time	t_{OVF}			0.2	0.4	—	s	*

Note: * Shows the time to count from 0 to 255, at which point an internal reset is generated, when the internal oscillator is selected.

7. System control instructions

Mnemonic		Operand Size	Addressing Mode and Instruction Length (bytes)									Operation	Condition Code						No. of States*1	
			#xx	Rn	@ERn	@(d, ERn)	@–ERn/@ERn+	@aa	@(d, PC)	@@aa	|		I	H	N	Z	V	C	Normal	Advanced
TRAPA	TRAPA #x:2	—									2	PC → @–SP CCR → @–SP <vector> → PC	1	—	—	—	—	—	14	16
RTE	RTE	—										CCR ← @SP+ PC ← @SP+	↕	↕	↕	↕	↕	↕	10	
SLEEP	SLEEP	—										Transition to power-down state	—	—	—	—	—	—	2	
LDC	LDC #xx:8, CCR	B	2									#xx:8 → CCR	↕	↕	↕	↕	↕	↕	2	
	LDC Rs, CCR	B		2								Rs8 → CCR	↕	↕	↕	↕	↕	↕	2	
	LDC @ERs, CCR	W			4							@ERs → CCR	↕	↕	↕	↕	↕	↕	6	
	LDC @(d:16, ERs), CCR	W				6						@(d:16, ERs) → CCR	↕	↕	↕	↕	↕	↕	8	
	LDC @(d:24, ERs), CCR	W				10						@(d:24, ERs) → CCR	↕	↕	↕	↕	↕	↕	12	
	LDC @ERs+, CCR	W					4					@ERs → CCR ERs32+2 → ERs32	↕	↕	↕	↕	↕	↕	8	
	LDC @aa:16, CCR	W						6				@aa:16 → CCR	↕	↕	↕	↕	↕	↕	8	
	LDC @aa:24, CCR	W						8				@aa:24 → CCR	↕	↕	↕	↕	↕	↕	10	
STC	STC CCR, Rd	B		2								CCR → Rd8	—	—	—	—	—	—	2	
	STC CCR, @ERd	W			4							CCR → @ERd	—	—	—	—	—	—	6	
	STC CCR, @(d:16, ERd)	W				6						CCR → @(d:16, ERd)	—	—	—	—	—	—	8	
	STC CCR, @(d:24, ERd)	W				10						CCR → @(d:24, ERd)	—	—	—	—	—	—	12	
	STC CCR, @–ERd	W					4					ERd32–2 → ERd32 CCR → @ERd	—	—	—	—	—	—	8	
	STC CCR, @aa:16	W						6				CCR → @aa:16	—	—	—	—	—	—	8	
	STC CCR, @aa:24	W						8				CCR → @aa:24	—	—	—	—	—	—	10	
ANDC	ANDC #xx:8, CCR	B	2									CCR∧#xx:8 → CCR	↕	↕	↕	↕	↕	↕	2	
ORC	ORC #xx:8, CCR	B	2									CCR#xx:8 → CCR	↕	↕	↕	↕	↕	↕	2	
XORC	XORC #xx:8, CCR	B	2									CCR⊕#xx:8 → CCR	↕	↕	↕	↕	↕	↕	2	
NOP	NOP	—									2	PC ← PC+2	—	—	—	—	—	—	2	

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
SUBX	SUBX #xx:8, Rd	1					
	SUBX. Rs, Rd	1					
TRAPA	TRAPA #xx:2	2	1	2			4
XOR	XOR.B #xx:8, Rd	1					
	XOR.B Rs, Rd	1					
	XOR.W #xx:16, Rd	2					
	XOR.W Rs, Rd	1					
	XOR.L #xx:32, ERd	3					
	XOR.L ERs, ERd	2					
XORC	XORC #xx:8, CCR	1					

Notes: 1. n: Specified value in R4L and R4. The source and destination operands are accessed n+1 times respectively.

2. Cannot be used in this LSI.

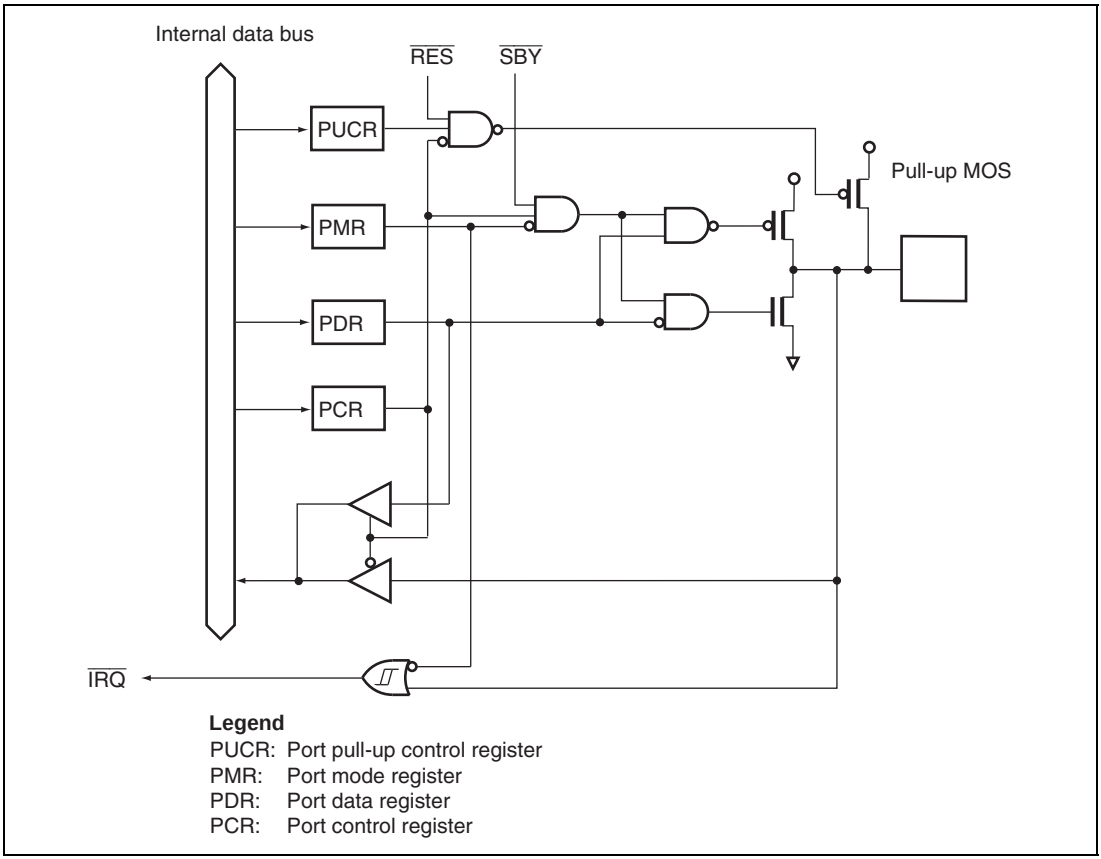


Figure B.2 Port 1 Block Diagram (P14)

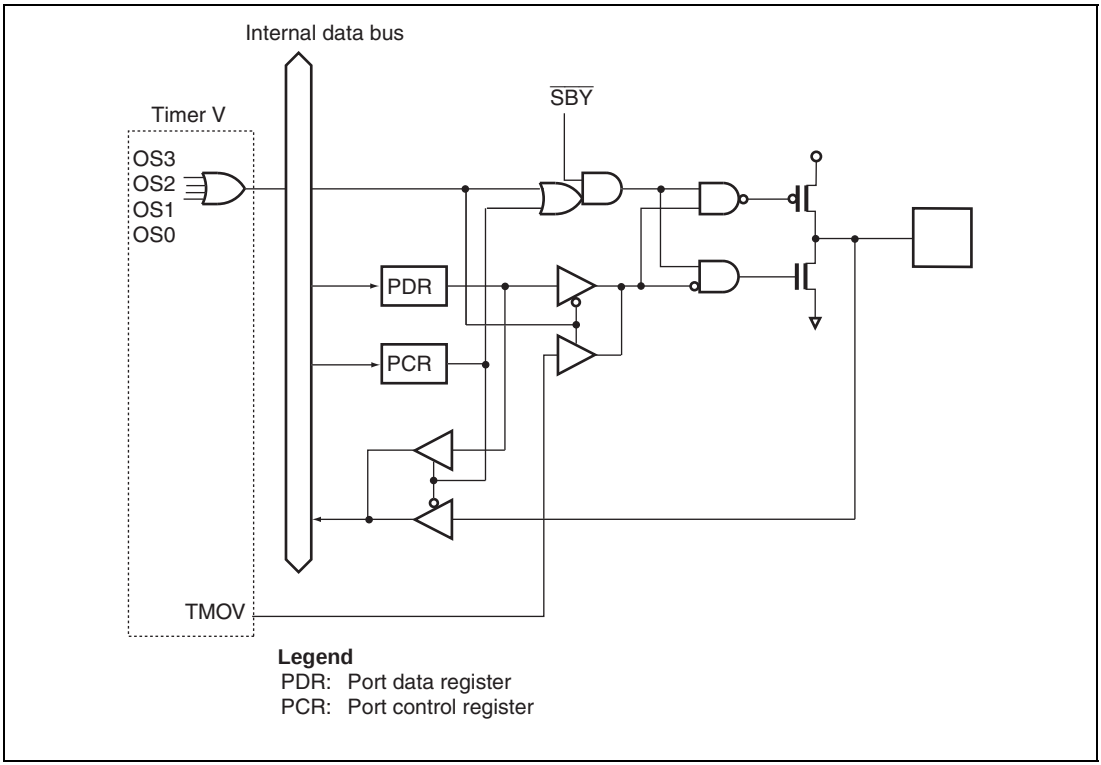


Figure B.14 Port 7 Block Diagram (P76)

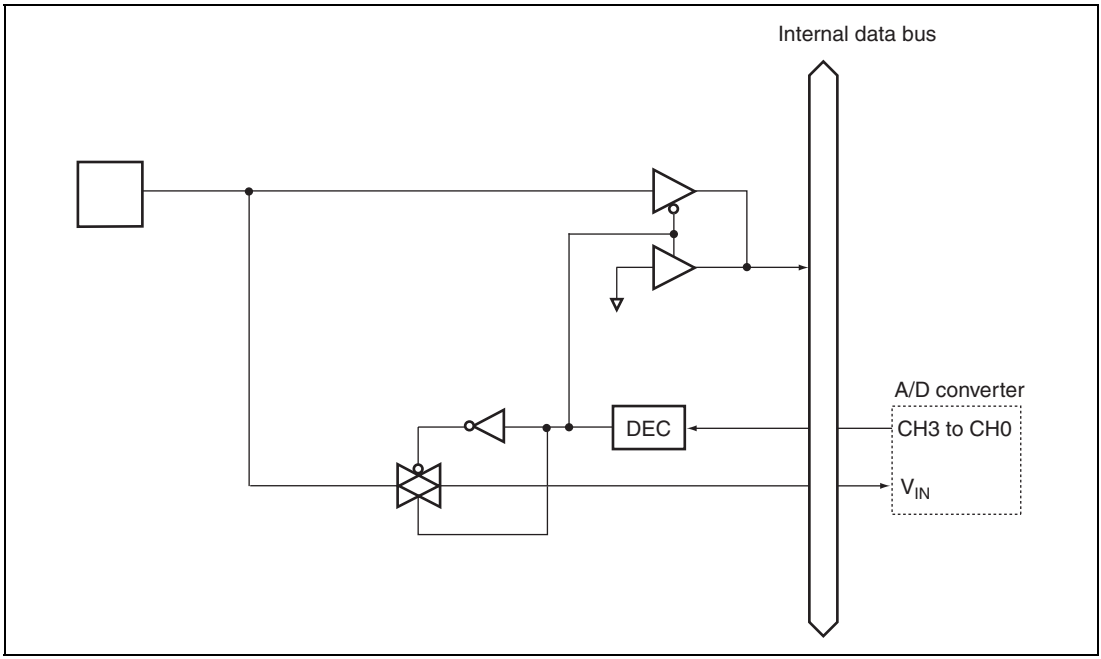


Figure B.23 Port B Block Diagram (PB3 to PB0)

B.2 Port States in Each Operating State

Port	Reset	Active	Sleep	Subsleep	Standby
P17 to P14, P12 to P10	High impedance	Functioning	Retained	Retained	High impedance*
P22 to P20	High impedance	Functioning	Retained	Retained	High impedance
P57 to P50	High impedance	Functioning	Retained	Retained	High impedance*
P76 to P70	High impedance	Functioning	Retained	Retained	High impedance
P84 to P80	High impedance	Functioning	Retained	Retained	High impedance
PB3 to PB0	High impedance	High impedance	High impedance	Retained	High impedance

Note: * High level output when the pull-up MOS is in on state.

Product Type			Product Code	Model Marking	Package Code
H8/36022	Flash memory version	Standard product	HD64F36022FP	HD64F36022FP	LQFP-64 (FP-64E)
			HD64F36022FX	HD64F36022FX	LQFP-48 (FP-48F)
			HD64F36022FY	HD64F36022FY	LQFP-48 (FP-48B)
			HD64F36022FT	HD64F36022FT	QFN-48(TNP-48)
		Product with POR & LVDC	HD64F36022GFP	HD64F36022GFP	LQFP-64 (FP-64E)
			HD64F36022GFX	HD64F36022GFX	LQFP-48 (FP-48F)
			HD64F36022GFY	HD64F36022GFY	LQFP-48 (FP-48B)
			HD64F36022GFT	HD64F36022GFT	QFN-48(TNP-48)
	Masked ROM version	Standard product	HD64336022FP	HD64336022(***)FP	LQFP-64 (FP-64E)
			HD64336022FX	HD64336022(***)FX	LQFP-48 (FP-48F)
			HD64336022FY	HD64336022(***)FY	LQFP-48 (FP-48B)
			HD64336022FT	HD64336022(***)FT	QFN-48(TNP-48)
		Product with POR & LVDC	HD64336022GFP	HD64336022G(***)FP	LQFP-64 (FP-64E)
			HD64336022GFX	HD64336022G(***)FX	LQFP-48 (FP-48F)
			HD64336022GFY	HD64336022G(***)FY	LQFP-48 (FP-48B)
			HD64336022GFT	HD64336022G(***)FT	QFN-48(TNP-48)
H8/36014	Flash memory version	Standard product	HD64F36014FP	HD64F36014FP	LQFP-64 (FP-64E)
			HD64F36014FX	HD64F36014FX	LQFP-48 (FP-48F)
			HD64F36014FY	HD64F36014FY	LQFP-48 (FP-48B)
			HD64F36014FT	HD64F36014FT	QFN-48(TNP-48)
		Product with POR & LVDC	HD64F36014GFP	HD64F36014GFP	LQFP-64 (FP-64E)
			HD64F36014GFX	HD64F36014GFX	LQFP-48 (FP-48F)
			HD64F36014GFY	HD64F36014GFY	LQFP-48 (FP-48B)
			HD64F36014GFT	HD64F36014GFT	QFN-48(TNP-48)
	Masked ROM version	Standard product	HD64336014FP	HD64336014(***)FP	LQFP-64 (FP-64E)
			HD64336014FX	HD64336014(***)FX	LQFP-48 (FP-48F)
			HD64336014FY	HD64336014(***)FY	LQFP-48 (FP-48B)
			HD64336014FT	HD64336014(***)FT	QFN-48(TNP-48)
		Product with POR & LVDC	HD64336014GFP	HD64336014G(***)FP	LQFP-64 (FP-64E)
			HD64336014GFX	HD64336014G(***)FX	LQFP-48 (FP-48F)
			HD64336014GFY	HD64336014G(***)FY	LQFP-48 (FP-48B)
			HD64336014GFT	HD64336014G(***)FT	QFN-48(TNP-48)