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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	SCI
Peripherals	PWM, WDT
Number of I/O	30
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36014fpjv

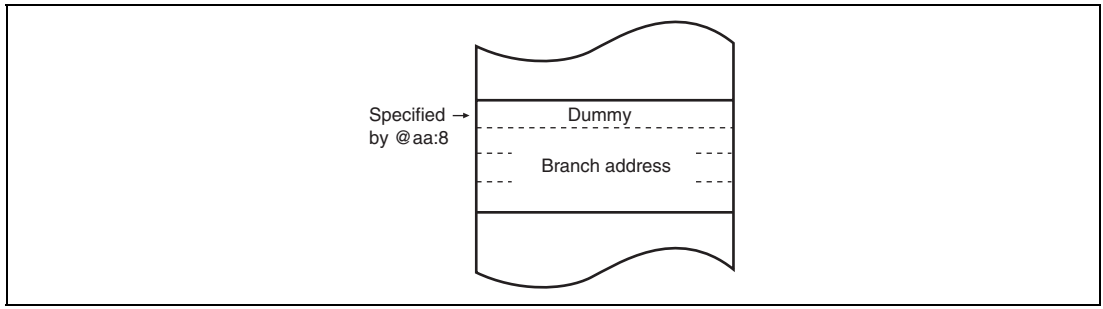


Figure 2.8 Branch Address Specification in Memory Indirect Mode

2.5.2 Effective Address Calculation

Table 2.12 indicates how effective addresses are calculated in each addressing mode. In this LSI the upper 8 bits of the effective address are ignored in order to generate a 16-bit effective address.

Table 2.12 Effective Address Calculation (1)

No	Addressing Mode and Instruction Format	Effective Address Calculation	Effective Address (EA)
1	Register direct(Rn) op | rm | rn		Operand is general register contents.
2	Register indirect(@ERn) op | r	31 … 0: General register contents	23 … 0
3	Register indirect with displacement @(d:16,ERn) or @(d:24,ERn) op | r | disp	31 … 0: General register contents 31 … 0: Sign extension | disp	23 … 0
4	Register indirect with post-increment or pre-decrement •Register indirect with post-increment @ERn+ op | r •Register indirect with pre-decrement @-ERn op | r	31 … 0: General register contents ± 1, 2, or 4 The value to be added or subtracted is 1 when the operand is byte size, 2 for word size, and 4 for longword size.	23 … 0

Bit	Bit Name	Initial Value	R/W	Description
0	IWPF0	0	R/W	WKP0 Interrupt Request Flag [Setting condition] When $\overline{\text{WKP0}}$ pin is designated for interrupt input and the designated signal edge is detected. [Clearing condition] When IWPF0 is cleared by writing 0.

3.3 Reset Exception Handling

When the $\overline{\text{RES}}$ pin goes low, all processing halts and this LSI enters the reset. The internal state of the CPU and the registers of the on-chip peripheral modules are initialized by the reset. To ensure that this LSI is reset at power-up, hold the $\overline{\text{RES}}$ pin low until the clock pulse generator output stabilizes. To reset the chip during operation, hold the $\overline{\text{RES}}$ pin low for at least 10 system clock cycles. When the $\overline{\text{RES}}$ pin goes high after being held low for the necessary time, this LSI starts reset exception handling. The reset exception handling sequence is shown in figure 3.1.

The reset exception handling sequence is as follows. However, for the reset exception handling sequence of the product with on-chip power-on reset circuit, refer to section 15, Power-On Reset and Low-Voltage Detection Circuits (Optional).

1. Set the I bit in the condition code register (CCR) to 1.
2. The CPU generates a reset exception handling vector address (from H'0000 to H'0001), the data in that address is sent to the program counter (PC) as the start address, and program execution starts from that address.

Table 6.2 Transition Mode after SLEEP Instruction Execution and Interrupt Handling

DTON	SSBY	SMSEL	Transition Mode after SLEEP Instruction Execution	Transition Mode due to Interrupt
0	0	0	Sleep mode	Active mode
	0	1	Subsleep mode	Active mode
	1	X	Standby mode	Active mode
1	X	0*	Active mode (direct transition)	—

Legend: X: Don't care.

* When a state transition is performed while SMSEL is 1, timer V, SCI3, SCI3_2, SCI3_3 (only for the H8/36024) and the A/D converter are reset, and all registers are set to their initial values. To use these functions after entering active mode, reset the registers.

Table 6.3 Internal State in Each Operating Mode

Function		Active Mode	Sleep Mode	Subsleep Mode	Standby Mode
System clock oscillator		Functioning	Functioning	Halted	Halted
CPU operations	Instructions	Functioning	Halted	Halted	Halted
	Registers	Functioning	Retained	Retained	Retained
RAM		Functioning	Retained	Retained	Retained
IO ports		Functioning	Retained	Retained	Register contents are retained, but output is the high-impedance state.
External interrupts	IRQ3, IRQ0	Functioning	Functioning	Functioning	Functioning
	WKP5 to WKP0	Functioning	Functioning	Functioning	Functioning
Peripheral functions	Timer V	Functioning	Functioning	Reset	Reset
	Timer W	Functioning	Functioning	Retained	Retained (if internal clock ϕ is selected as a count clock, the counter is incremented by a subclock)
	Watchdog timer	Functioning	Functioning	Retained	Retained (functioning if the internal oscillator is selected as a count clock)
	SCI3	Functioning	Functioning	Reset	Reset
	A/D converter	Functioning	Functioning	Reset	Reset

4. After matching the bit rates, the chip transmits one H'00 byte to the host to indicate the completion of bit rate adjustment. The host should confirm that this adjustment end indication (H'00) has been received normally, and transmit one H'55 byte to the chip. If reception could not be performed normally, initiate boot mode again by a reset. Depending on the host's transfer bit rate and system clock frequency of this LSI, there will be a discrepancy between the bit rates of the host and the chip. To operate the SCI properly, set the host's transfer bit rate and system clock frequency of this LSI within the ranges listed in table 7.3.
5. In boot mode, a part of the on-chip RAM area is used by the boot program. The area H'F780 to H'FEEF is the area to which the programming control program is transferred from the host. The boot program area cannot be used until the execution state in boot mode switches to the programming control program.
6. Before branching to the programming control program, the chip terminates transfer operations by SCI3 (by clearing the RE and TE bits in SCR3 to 0), however the adjusted bit rate value remains set in BRR. Therefore, the programming control program can still use it for transfer of write data or verify data with the host. The TxD pin is high (PCR22 = 1, P22 = 1). The contents of the CPU general registers are undefined immediately after branching to the programming control program. These registers must be initialized at the beginning of the programming control program, as the stack pointer (SP), in particular, is used implicitly in subroutine calls, etc.
7. Boot mode can be cleared by a reset. End the reset after driving the reset pin low, waiting at least 20 states, and then setting the $\overline{\text{NMI}}$ pin. Boot mode is also cleared when a WDT overflow occurs.
8. Do not change the TEST pin and $\overline{\text{NMI}}$ pin input levels in boot mode.

7.5 Program/Erase Protection

There are three kinds of flash memory program/erase protection; hardware protection, software protection, and error protection.

7.5.1 Hardware Protection

Hardware protection refers to a state in which programming/erasing of flash memory is forcibly disabled or aborted because of a transition to reset, subsleep mode or standby mode. Flash memory control register 1 (FLMCR1), flash memory control register 2 (FLMCR2), and erase block register 1 (EBR1) are initialized. In a reset via the $\overline{\text{RES}}$ pin, the reset state is not entered unless the $\overline{\text{RES}}$ pin is held low until oscillation stabilizes after powering on. In the case of a reset during operation, hold the $\overline{\text{RES}}$ pin low for the $\overline{\text{RES}}$ pulse width specified in the AC Characteristics section.

7.5.2 Software Protection

Software protection can be implemented against programming/erasing of all flash memory blocks by clearing the SWE bit in FLMCR1. When software protection is in effect, setting the P or E bit in FLMCR1 does not cause a transition to program mode or erase mode. By setting the erase block register 1 (EBR1), erase protection can be set for individual blocks. When EBR1 is set to H'00, erase protection is set for all blocks.

7.5.3 Error Protection

In error protection, an error is detected when CPU runaway occurs during flash memory programming/erasing, or operation is not performed in accordance with the program/erase algorithm, and the program/erase operation is aborted. Aborting the program/erase operation prevents damage to the flash memory due to overprogramming or overerasing.

When the following errors are detected during programming/erasing of flash memory, the FLER bit in FLMCR2 is set to 1, and the error protection state is entered.

- When the flash memory of the relevant address area is read during programming/erasing (including vector read and instruction fetch)
- Immediately after exception handling excluding a reset during programming/erasing
- When a SLEEP instruction is executed during programming/erasing

The FLMCR1, FLMCR2, and EBR1 settings are retained, however program mode or erase mode is aborted at the point at which the error occurred. Program mode or erase mode cannot be re-entered by re-setting the P or E bit. However, PV and EV bit setting is enabled, and a transition can be made to verify mode. Error protection can be cleared only by a reset.

Section 9 I/O Ports

The group of this LSI has thirty general I/O ports and four general input-only ports. Port 8 is a large current port, which can drive 20 mA ($@V_{OL}$ = 1.5 V) when a low level signal is output. Any of these ports can become an input port immediately after a reset. They can also be used as I/O pins of the on-chip peripheral modules or external interrupt input pins, and these functions can be switched depending on the register settings. The registers for selecting these functions can be divided into two types: those included in I/O ports and those included in each on-chip peripheral module. General I/O ports are comprised of the port control register for controlling inputs/outputs and the port data register for storing output data and can select inputs/outputs in bit units. For functions in each port, see Appendix B.1, I/O Port Block Diagrams. For the execution of bit manipulation instructions to the port control register and port data register, see section 2.8.3, Bit Manipulation Instruction.

9.1 Port 1

Port 1 is a general I/O port also functioning as IRQ interrupt input pins, timer V input pin, and SCI3 I/O pin. Figure 9.1 shows its pin configuration.

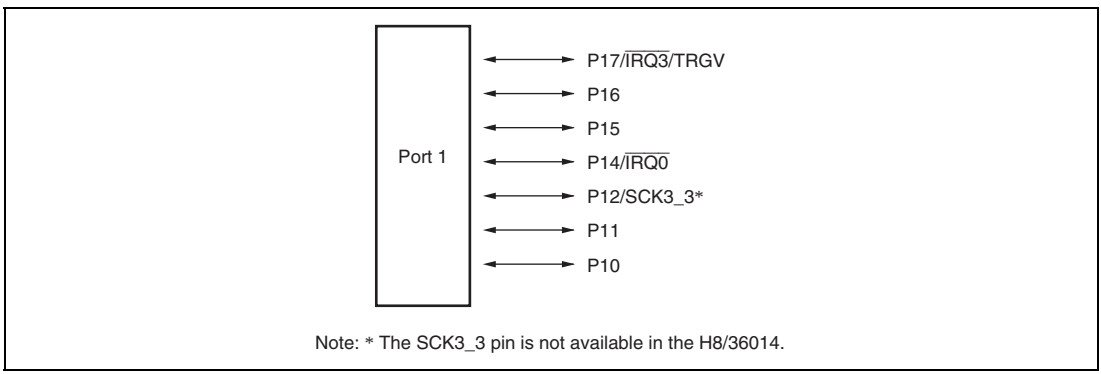


Figure 9.1 Port 1 Pin Configuration

Port 1 has the following registers.

- Port mode register 1 (PMR1)
- Port control register 1 (PCR1)
- Port data register 1 (PDR1)
- Port pull-up control register 1 (PUCR1)

Figure 11.8 shows an example of buffer operation when the GRA is set as an input-capture register and GRC is set as the buffer register for GRA. TCNT operates as a free-running counter, and FTIOA captures both rising and falling edge of the input signal. Due to the buffer operation, the GRA value is transferred to GRC by input-capture A and the TCNT value is stored in GRA.

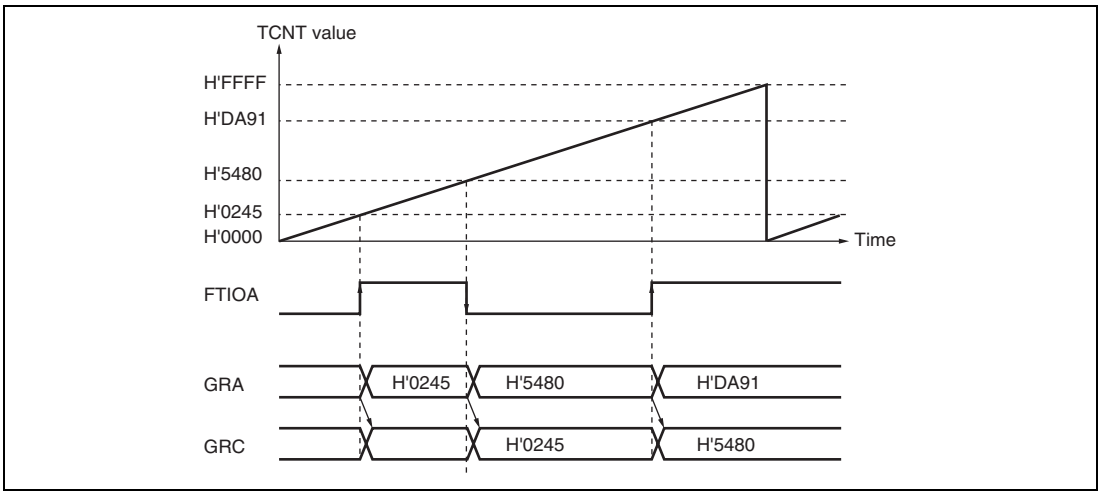


Figure 11.8 Buffer Operation Example (Input Capture)

13.3.5 Serial Mode Register (SMR)

SMR is used to set the SCI3's serial transfer format and select the baud rate generator clock source.

Bit	Bit Name	Initial Value	R/W	Description
7	COM	0	R/W	Communication Mode 0: Asynchronous mode 1: Clocked synchronous mode
6	CHR	0	R/W	Character Length (enabled only in asynchronous mode) 0: Selects 8 bits as the data length. 1: Selects 7 bits as the data length.
5	PE	0	R/W	Parity Enable (enabled only in asynchronous mode) When this bit is set to 1, the parity bit is added to transmit data before transmission, and the parity bit is checked in reception.
4	PM	0	R/W	Parity Mode (enabled only when the PE bit is 1 in asynchronous mode) 0: Selects even parity. 1: Selects odd parity.
3	STOP	0	R/W	Stop Bit Length (enabled only in asynchronous mode) Selects the stop bit length in transmission. 0: 1 stop bit 1: 2 stop bits For reception, only the first stop bit is checked, regardless of the value in the bit. If the second stop bit is 0, it is treated as the start bit of the next transmit character.
2	MP	0	R/W	Multiprocessor Mode When this bit is set to 1, the multiprocessor communication function is enabled. The PE bit and PM bit settings are invalid in multiprocessor mode. In clocked synchronous mode, clear this bit to 0.

13.4 Operation in Asynchronous Mode

Figure 13.2 shows the general format for asynchronous serial communication. One character (or frame) consists of a start bit (low level), followed by data (in LSB-first order), a parity bit (high or low level), and finally stop bits (high level). Inside the SCI3, the transmitter and receiver are independent units, enabling full-duplex. Both the transmitter and the receiver also have a double-buffered structure, so data can be read or written during transmission or reception, enabling continuous data transfer.

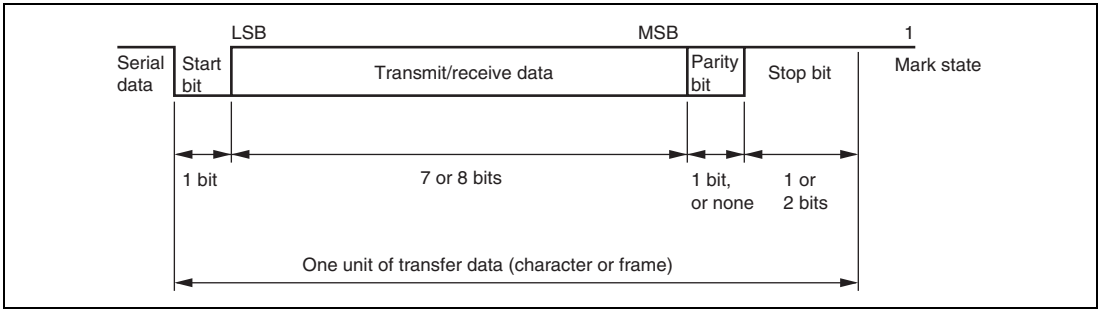


Figure 13.2 Data Format in Asynchronous Communication

13.4.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external clock input at the SCK3 pin can be selected as the SCI3's serial clock, according to the setting of the COM bit in SMR and the CKE0 and CKE1 bits in SCR3. When an external clock is input at the SCK3 pin, the clock frequency should be 16 times the bit rate used.

When the SCI3 is operated on an internal clock, the clock can be output from the SCK3 pin. The frequency of the clock output in this case is equal to the bit rate, and the phase is such that the rising edge of the clock is in the middle of the transmit data, as shown in figure 13.3.

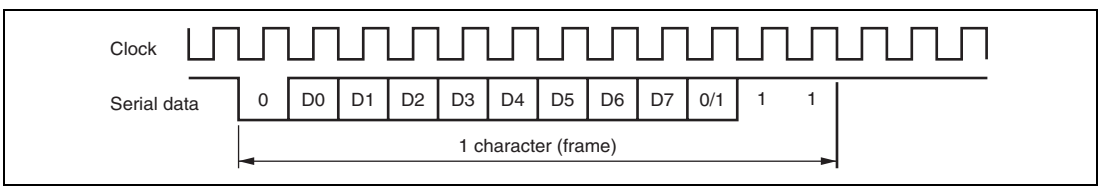


Figure 13.3 Relationship between Output Clock and Transfer Data Phase (Asynchronous Mode)(Example with 8-Bit Data, Parity, Two Stop Bits)

17.3 Register States in Each Operating Mode

Register Name	Reset	Active	Sleep	Subsleep	Standby	Module
SMR_3	Initialized	—	—	Initialized	Initialized	SCI3_3
BRR_3	Initialized	—	—	Initialized	Initialized	
SCR3_3	Initialized	—	—	Initialized	Initialized	
TDR_3	Initialized	—	—	Initialized	Initialized	
SSR_3	Initialized	—	—	Initialized	Initialized	
RDR_3	Initialized	—	—	Initialized	Initialized	
SMCR	Initialized	—	—	Initialized	Initialized	
LVDCR	Initialized	—	—	—	—	LVDC (optional)
LVDSR	Initialized	—	—	—	—	
SMR_2	Initialized	—	—	Initialized	Initialized	SCI3_2
BRR_2	Initialized	—	—	Initialized	Initialized	
SCR3_2	Initialized	—	—	Initialized	Initialized	
TDR_2	Initialized	—	—	Initialized	Initialized	
SSR_2	Initialized	—	—	Initialized	Initialized	
RDR_2	Initialized	—	—	Initialized	Initialized	
TMRW	Initialized	—	—	—	—	Timer W
TCRW	Initialized	—	—	—	—	
TIERW	Initialized	—	—	—	—	
TSRW	Initialized	—	—	—	—	
TIOR0	Initialized	—	—	—	—	
TIOR1	Initialized	—	—	—	—	
TCNT	Initialized	—	—	—	—	
GRA	Initialized	—	—	—	—	
GRB	Initialized	—	—	—	—	
GRC	Initialized	—	—	—	—	
GRD	Initialized	—	—	—	—	
FLMCR1	Initialized	—	—	Initialized	Initialized	ROM
FLMCR2	Initialized	—	—	—	—	
EBR1	Initialized	—	—	Initialized	Initialized	
FENR	Initialized	—	—	—	—	

Section 18 Electrical Characteristics

18.1 Absolute Maximum Ratings

Table 18.1 Absolute Maximum Ratings

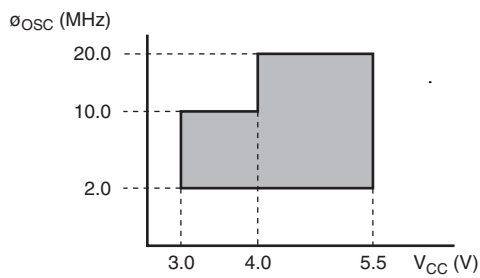
Item		Symbol	Value	Unit	Note
Power supply voltage		V_{CC}	–0.3 to +7.0	V	*
Analog power supply voltage		AV_{CC}	–0.3 to +7.0	V	
Input voltage	Ports other than Port B	V_{IN}	–0.3 to V_{CC} +0.3	V	
	Port B		–0.3 to AV_{CC} +0.3	V	
Operating temperature		T_{opr}	–20 to +75	°C	
Storage temperature		T_{stg}	–55 to +125	°C	

Note: * Permanent damage may result if maximum ratings are exceeded. Normal operation should be under the conditions specified in Electrical Characteristics. Exceeding these values can result in incorrect operation and reduced reliability.

18.2 Electrical Characteristics (F-ZTAT™ Version)

18.2.1 Power Supply Voltage and Operating Ranges

(1) Power Supply Voltage and Oscillation Frequency Range



- AV_{CC} = 3.3 V to 5.5 V
- Active mode
- Sleep mode

Item	Symbol	Applicable Pins	Test Condition	Values Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	P12 to P10, P17 to P14, P22 to P20, P57 to P50, P76 to P70, P84 to P80	V_{CC} = 4.0 V to 5.5 V $-I_{OH}$ = 1.5 mA	V_{CC} – 1.0	—	—	V	
			$-I_{OH}$ = 0.1 mA	V_{CC} – 0.5	—	—		
Output low voltage	V_{OL}	P12 to P10, P17 to P14, P22 to P20, P57 to P50, P76 to P70	V_{CC} = 4.0 V to 5.5 V I_{OL} = 1.6 mA	—	—	0.6	V	
			I_{OL} = 0.4 mA	—	—	0.4		
		P84 to P80	V_{CC} = 4.0 V to 5.5 V I_{OL} = 20.0 mA	—	—	1.5	V	
			V_{CC} = 4.0 V to 5.5 V I_{OL} = 10.0 mA	—	—	1.0		
			V_{CC} = 4.0 V to 5.5 V I_{OL} = 1.6 mA	—	—	0.4		
			I_{OL} = 0.4 mA	—	—	0.4		
Input/ output leakage current	$\lvert I_{IL} \rvert$	OSC1, $\overline{\text{RES}}$, $\overline{\text{NMI}}$, $\overline{\text{WKP0}}$ to $\overline{\text{WKP5}}$, $\overline{\text{IRQ0}}$, $\overline{\text{IRQ3}}$, $\overline{\text{ADTRG}}$, TRGV, TMRIV, TMCIV, FTCI, FTIOA to FTIOD, RXD, RXD_2, RXD_3*[1], SCK3, SCK3_2, SCK3_3*[1]	V_{IN} = 0.5 V to (V_{CC} – 0.5 V)	—	—	1.0	μA	
		P12 to P10, P17 to P14, P22 to P20, P57 to P50, P76 to P70, P84 to P80	V_{IN} = 0.5 V to (V_{CC} – 0.5 V)	—	—	1.0	μA	
		PB3 to PB0	V_{IN} = 0.5 V to (AV_{CC} – 0.5 V)	—	—	1.0	μA	

Item	Symbol	Applicable Pins	Test Condition	Values Min	Typ	Max	Unit	Notes
Pull-up MOS current	$-I_p$	P12 to P10, P17 to P14, P55 to P50	V_{CC} = 5.0 V, V_{IN} = 0.0 V	50.0	—	300.0	µA	
			V_{CC} = 3.0 V, V_{IN} = 0.0 V	—	60.0	—		Reference value
Input capacitance	C_{in}	All input pins except power supply pins	f = 1 MHz, V_{IN} = 0.0 V, T_a = 25°C	—	—	15.0	pF	
Active mode current consumption	I_{OPE1}	V_{CC}	Active mode 1 V_{CC} = 5.0 V, f_{OSC} = 20 MHz	—	15.0	30.0	mA	*2
			Active mode 1 V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	8.0	—		*2 Reference value
	I_{OPE2}	V_{CC}	Active mode 2 V_{CC} = 5.0 V, f_{OSC} = 20 MHz	—	1.8	3.0	mA	*2
			Active mode 2 V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	1.2	—		*2 Reference value
Sleep mode current consumption	I_{SLEEP1}	V_{CC}	Sleep mode 1 V_{CC} = 5.0 V, f_{OSC} = 20 MHz	—	11.5	22.5	mA	*2
			Sleep mode 1 V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	6.5	—		*2 Reference value
	I_{SLEEP2}	V_{CC}	Sleep mode 2 V_{CC} = 5.0 V, f_{OSC} = 20 MHz	—	1.7	2.7	mA	*2
			Sleep mode 2 V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	1.1	—		*2 Reference value
Standby mode current consumption	I_{STBY}	V_{CC}		—	—	5.0	µA	*2

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
Bcc	BLT d:8	2					
	BGT d:8	2					
	BLE d:8	2					
	BRA d:16(BT d:16)	2					2
	BRN d:16(BF d:16)	2					2
	BHI d:16	2					2
	BLS d:16	2					2
	BCC d:16(BHS d:16)	2					2
	BCS d:16(BLO d:16)	2					2
	BNE d:16	2					2
	BEQ d:16	2					2
	BVC d:16	2					2
	BVS d:16	2					2
	BPL d:16	2					2
	BMI d:16	2					2
	BGE d:16	2					2
	BLT d:16	2					2
	BGT d:16	2					2
	BLE d:16	2					2
BCLR	BCLR #xx:3, Rd	1					
	BCLR #xx:3, @ERd	2			2		
	BCLR #xx:3, @aa:8	2			2		
	BCLR Rn, Rd	1					
	BCLR Rn, @ERd	2			2		
	BCLR Rn, @aa:8	2			2		
BIAND	BIAND #xx:3, Rd	1					
	BIAND #xx:3, @ERd	2			1		
	BIAND #xx:3, @aa:8	2			1		
BILD	BILD #xx:3, Rd	1					
	BILD #xx:3, @ERd	2			1		
	BILD #xx:3, @aa:8	2			1		

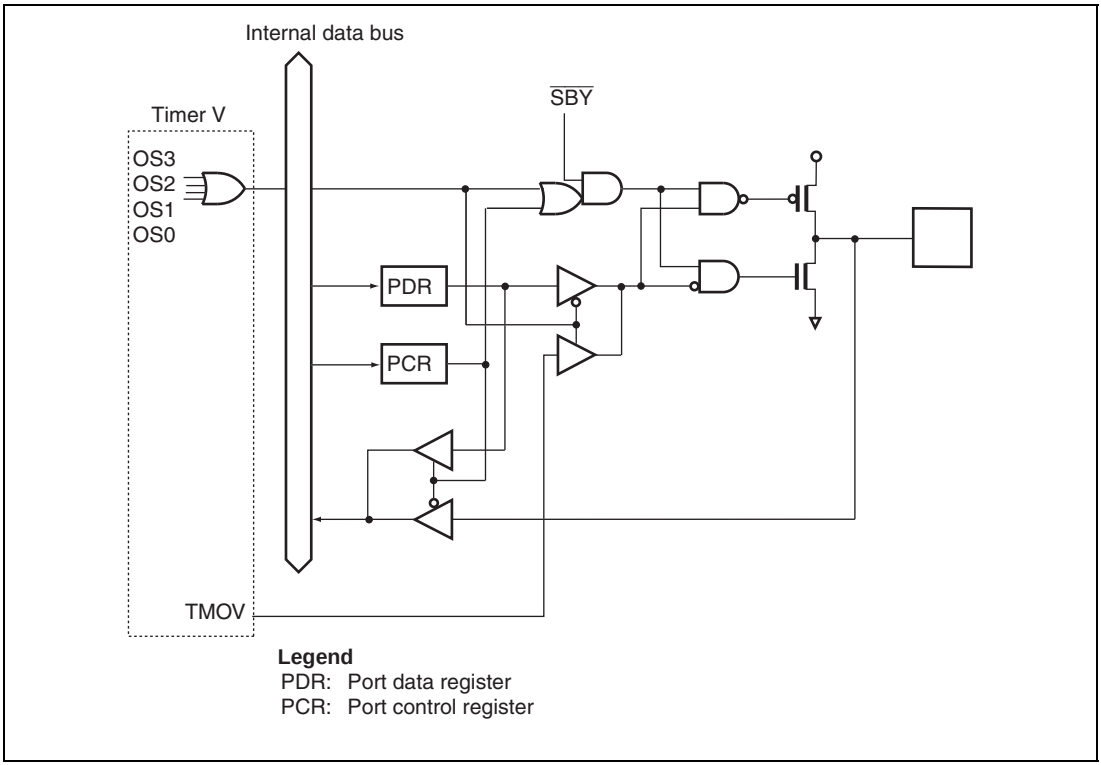


Figure B.14 Port 7 Block Diagram (P76)

Product Type			Product Code	Model Marking	Package Code
H8/36022	Flash memory version	Standard product	HD64F36022FP	HD64F36022FP	LQFP-64 (FP-64E)
			HD64F36022FX	HD64F36022FX	LQFP-48 (FP-48F)
			HD64F36022FY	HD64F36022FY	LQFP-48 (FP-48B)
			HD64F36022FT	HD64F36022FT	QFN-48(TNP-48)
		Product with POR & LVDC	HD64F36022GFP	HD64F36022GFP	LQFP-64 (FP-64E)
			HD64F36022GFX	HD64F36022GFX	LQFP-48 (FP-48F)
			HD64F36022GFY	HD64F36022GFY	LQFP-48 (FP-48B)
			HD64F36022GFT	HD64F36022GFT	QFN-48(TNP-48)
	Masked ROM version	Standard product	HD64336022FP	HD64336022(***)FP	LQFP-64 (FP-64E)
			HD64336022FX	HD64336022(***)FX	LQFP-48 (FP-48F)
			HD64336022FY	HD64336022(***)FY	LQFP-48 (FP-48B)
			HD64336022FT	HD64336022(***)FT	QFN-48(TNP-48)
		Product with POR & LVDC	HD64336022GFP	HD64336022G(***)FP	LQFP-64 (FP-64E)
			HD64336022GFX	HD64336022G(***)FX	LQFP-48 (FP-48F)
			HD64336022GFY	HD64336022G(***)FY	LQFP-48 (FP-48B)
			HD64336022GFT	HD64336022G(***)FT	QFN-48(TNP-48)
H8/36014	Flash memory version	Standard product	HD64F36014FP	HD64F36014FP	LQFP-64 (FP-64E)
			HD64F36014FX	HD64F36014FX	LQFP-48 (FP-48F)
			HD64F36014FY	HD64F36014FY	LQFP-48 (FP-48B)
			HD64F36014FT	HD64F36014FT	QFN-48(TNP-48)
		Product with POR & LVDC	HD64F36014GFP	HD64F36014GFP	LQFP-64 (FP-64E)
			HD64F36014GFX	HD64F36014GFX	LQFP-48 (FP-48F)
			HD64F36014GFY	HD64F36014GFY	LQFP-48 (FP-48B)
			HD64F36014GFT	HD64F36014GFT	QFN-48(TNP-48)
	Masked ROM version	Standard product	HD64336014FP	HD64336014(***)FP	LQFP-64 (FP-64E)
			HD64336014FX	HD64336014(***)FX	LQFP-48 (FP-48F)
			HD64336014FY	HD64336014(***)FY	LQFP-48 (FP-48B)
			HD64336014FT	HD64336014(***)FT	QFN-48(TNP-48)
		Product with POR & LVDC	HD64336014GFP	HD64336014G(***)FP	LQFP-64 (FP-64E)
			HD64336014GFX	HD64336014G(***)FX	LQFP-48 (FP-48F)
			HD64336014GFY	HD64336014G(***)FY	LQFP-48 (FP-48B)
			HD64336014GFT	HD64336014G(***)FT	QFN-48(TNP-48)

Main Revisions and Additions in this Edition

Item	Page	Revision (See Manual for Details)
Preface	vi, vii	When using the on-chip emulator (E7, E8) for H8/36014 program development and debugging, the following restrictions must be noted. 1. The $\overline{\text{NMI}}$ pin is reserved for the E7 or E8, and cannot be used. 2. Area H'7000 to H'7FFF is used by the E7 or E8, and is not available to the user. 4. When the E7 or E8 is used, address breaks can be set as either available to the user or for use by the E7 or E8. If address breaks are set as being used by the E7 or E8, the address break control registers must not be accessed. 5. When the E7 or E8 is used, $\overline{\text{NMI}}$ is an input/output pin (open-drain in output mode). 6. Use channel 1 of the SCI3 (P21/RXD, P22/TXD) in on-board programming mode by boot mode. Note has been deleted.
Section 1 Overview 1.2 Internal Block Diagram Figure 1.1 Internal Block Diagram	3	3 Can also be used for the E7 or E8 emulator.
Figure 1.2 Pin Arrangement (FP-64E)	4	2 Can also be used for the E7 or E8 emulator.
Figure 1.3 Pin Arrangement (FP-48F, FP-48B, TNP-48)	5	2 Can also be used for the E7 or E8 emulator.
Table 1.1 Pin Functions	7	**Type** : **Functions** E10T : Interface pin for the E10T, E8, or E7 emulator
Section 7 ROM	77	The features of the 32-kbyte (4 kbytes of them are the control program area for E7 or E8) flash memory built into the HD64F36024 and HD64F36014 are summarized below.
Section 8 RAM	93	Note: When the E7 or E8 is used, area H'F780 to H'FB7F must not be accessed.

Item	Page	Revision (See Manual for Details)
Table 18.10 DC Characteristics (1)	270	

Item	Symbol	Applicable Pins	Test Condition	Values Min
Input high voltage	V_{IH}	PB3 to PB0	V_{CC} = 4.0 V to 5.5 V	V_{CC} × 0.7
				V_{CC} × 0.8
Input low voltage	V_{IL}	RXD, RXD_2, RXD_3*[1], P12 to P10, P17 to P14, : PB3 to PB0	V_{CC} = 4.0 V to 5.5 V	–0.3

Table 18.10 DC Characteristics (1)	273	

Mode	$\overline{RES}$ Pin	Internal State
Active mode 1	V_{CC}	Operates
Active mode 2		Operates (φOSC/64)
Sleep mode 1	V_{CC}	Only timers operate
Sleep mode 2		Only timers operate (φOSC/64)

Appendix D Package Dimensions Figure D.1 FP-64E Package Dimensions	343	Swapped with new one.
Figure D.2 FP-48F Package Dimensions	344	Swapped with new one.
Figure D.3 FP-48B Package Dimensions	345	Swapped with new one.
Figure D.4 TNP-48 Package Dimensions	346	Swapped with new one.