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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | H8/300H |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | SCI |
| Peripherals | PWM, WDT |
| Number of I/O | 30 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 4x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LFQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/df36014fpwv |

User's Manual

16

The revision list can be viewed directly by clicking the title page.

The revision list summarizes the locations of revisions and additions. Details should always be checked by referring to the relevant text.

# H8/36024Group, H8/36014Group

## Hardware Manual

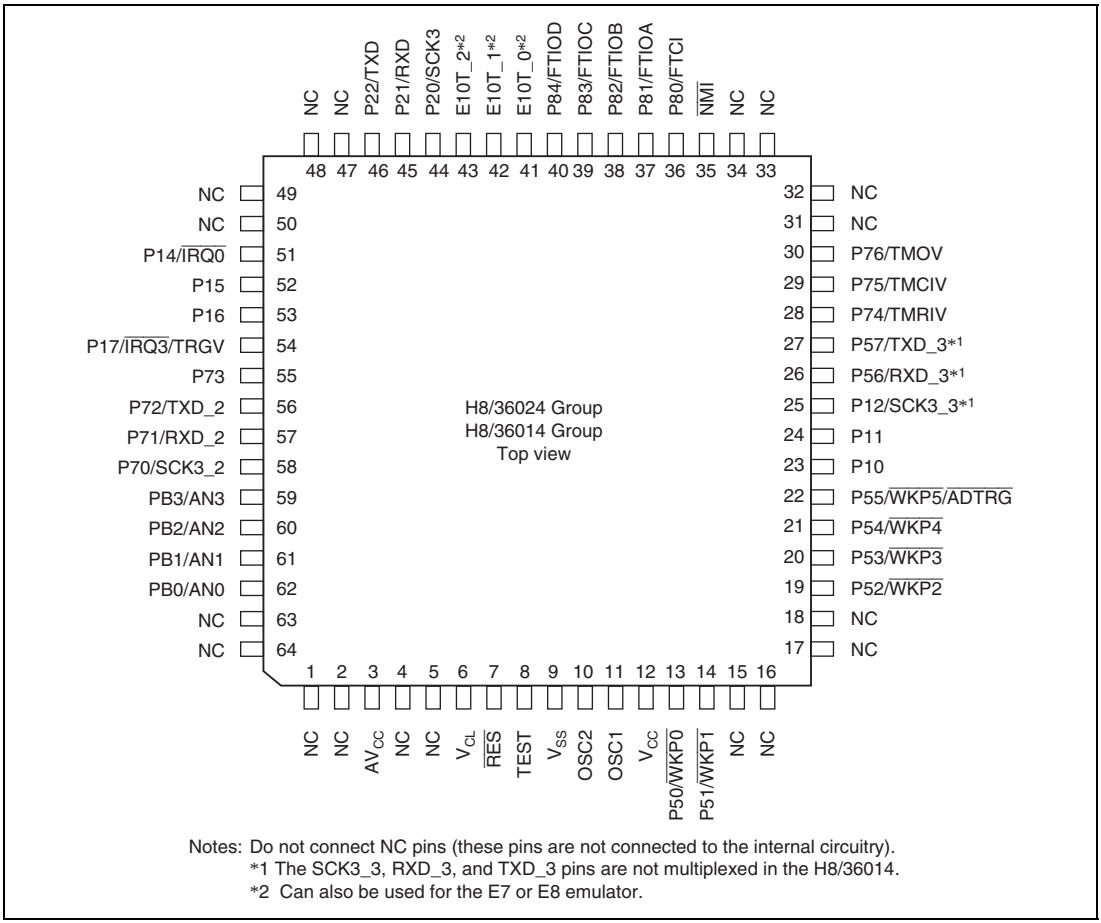
## Renesas 16-Bit Single-Chip Microcomputer H8 Family/H8/300H Tiny Series

| | |
|---|---|
| H8/36024F | HD64F36024, HD64F36024G, |
| H8/36022F | HD64F36022, HD64F36022G, |
| H8/36014F | HD64F36014, HD64F36014G, |
| H8/36012F | HD64F36012, HD64F36012G, |
| H8/36024 | HD64336024, HD64336024G, |
| H8/36023 | HD64336023, HD64336023G, |
| H8/36022 | HD64336022, HD64336022G, |
| H8/36014 | HD64336014, HD64336014G, |
| H8/36013 | HD64336013, HD64336013G, |
| H8/36012 | HD64336012, HD64336012G, |
| H8/36011 | HD64336011, HD64336011G, |
| H8/36010 | HD64336010, HD64336010G |

Renesas Electronics
www.renesas.com

Rev.4.00 2005.09

## 1.3 Pin Arrangement




Notes: Do not connect NC pins (these pins are not connected to the internal circuitry).
*1 The SCK3_3, RXD_3, and TXD_3 pins are not multiplexed in the H8/36014.
*2 Can also be used for the E7 or E8 emulator.

**Figure 1.2 Pin Arrangement (FP-64E)**

**Table 2.6 Bit Manipulation Instructions (2)**

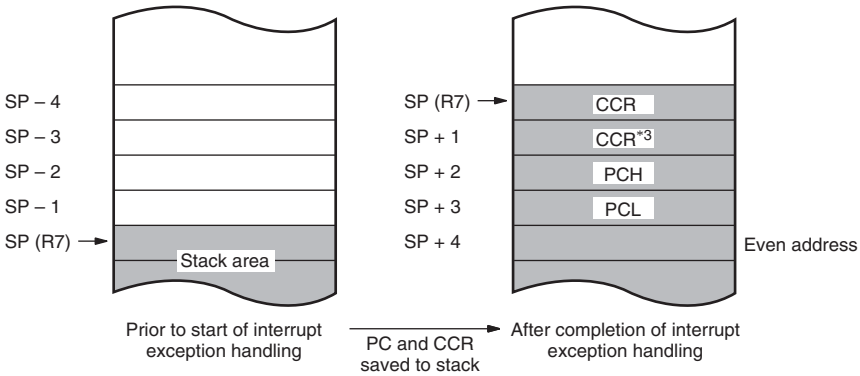
| Instruction | Size* | Function |
|---|---|---|
| BXOR | B | C ⊕ (<bit-No.> of <EAd>) → C<br>XORs the carry flag with a specified bit in a general register or memory operand and stores the result in the carry flag. |
| BIXOR | B | C ⊕ ¬ (<bit-No.> of <EAd>) → C<br>XORs the carry flag with the inverse of a specified bit in a general register or memory operand and stores the result in the carry flag.<br>The bit number is specified by 3-bit immediate data. |
| BLD | B | (<bit-No.> of <EAd>) → C<br>Transfers a specified bit in a general register or memory operand to the carry flag. |
| BILD | B | ¬ (<bit-No.> of <EAd>) → C<br>Transfers the inverse of a specified bit in a general register or memory operand to the carry flag.<br>The bit number is specified by 3-bit immediate data. |
| BST | B | C → (<bit-No.> of <EAd>)<br>Transfers the carry flag value to a specified bit in a general register or memory operand. |
| BIST | B | ¬ C → (<bit-No.> of <EAd>)<br>Transfers the inverse of the carry flag value to a specified bit in a general register or memory operand.<br>The bit number is specified by 3-bit immediate data. |

Note: * Refers to the operand size.
B: Byte

### 3.2.2 Interrupt Edge Select Register 2 (IEGR2)

IEGR2 selects the direction of an edge that generates interrupt requests of the pins $\overline{\text{ADTRG}}$ and $\overline{\text{WKP5}}$ to $\overline{\text{WKP0}}$.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7, 6 | — | All 1 | — | Reserved<br>These bits are always read as 1. |
| 5 | WPEG5 | 0 | R/W | WKP5 Edge Select<br>0: Falling edge of $\overline{\text{WKP5}}$ ($\overline{\text{ADTRG}}$) pin input is detected<br>1: Rising edge of $\overline{\text{WKP5}}$ ($\overline{\text{ADTRG}}$) pin input is detected |
| 4 | WPEG4 | 0 | R/W | WKP4 Edge Select<br>0: Falling edge of $\overline{\text{WKP4}}$ pin input is detected<br>1: Rising edge of $\overline{\text{WKP4}}$ pin input is detected |
| 3 | WPEG3 | 0 | R/W | WKP3 Edge Select<br>0: Falling edge of $\overline{\text{WKP3}}$ pin input is detected<br>1: Rising edge of $\overline{\text{WKP3}}$ pin input is detected |
| 2 | WPEG2 | 0 | R/W | WKP2 Edge Select<br>0: Falling edge of $\overline{\text{WKP2}}$ pin input is detected<br>1: Rising edge of $\overline{\text{WKP2}}$ pin input is detected |
| 1 | WPEG1 | 0 | R/W | WKP1Edge Select<br>0: Falling edge of $\overline{\text{WKP1}}$ pin input is detected<br>1: Rising edge of $\overline{\text{WKP1}}$ pin input is detected |
| 0 | WPEG0 | 0 | R/W | WKP0 Edge Select<br>0: Falling edge of $\overline{\text{WKP0}}$ pin input is detected<br>1: Rising edge of $\overline{\text{WKP0}}$ pin input is detected |




**Legend:**
PCH: Upper 8 bits of program counter (PC)
PCL: Lower 8 bits of program counter (PC)
CCR: Condition code register
SP: Stack pointer

Notes: 1. PC shows the address of the first instruction to be executed upon return from the interrupt handling routine.
2. Register contents must always be saved and restored by word length, starting from an even-numbered address.
3. Ignored when returning from the interrupt handling routine.

**Figure 3.2 Stack Status after Exception Handling**

### 3.4.4 Interrupt Response Time

Table 3.2 shows the number of wait states after an interrupt request flag is set until the first instruction of the interrupt handling-routine is executed.

**Table 3.2 Interrupt Wait States**

| Item | States | Total |
|---|---|---|
| Waiting time for completion of executing instruction* | 1 to 23 | 15 to 37 |
| Saving of PC and CCR to stack | 4 | |
| Vector fetch | 2 | |
| Instruction fetch | 4 | |
| Internal processing | 4 | |

Note: * Not including EEPMOV instruction.

Figures 4.2 show the operation examples of the address break interrupt setting.

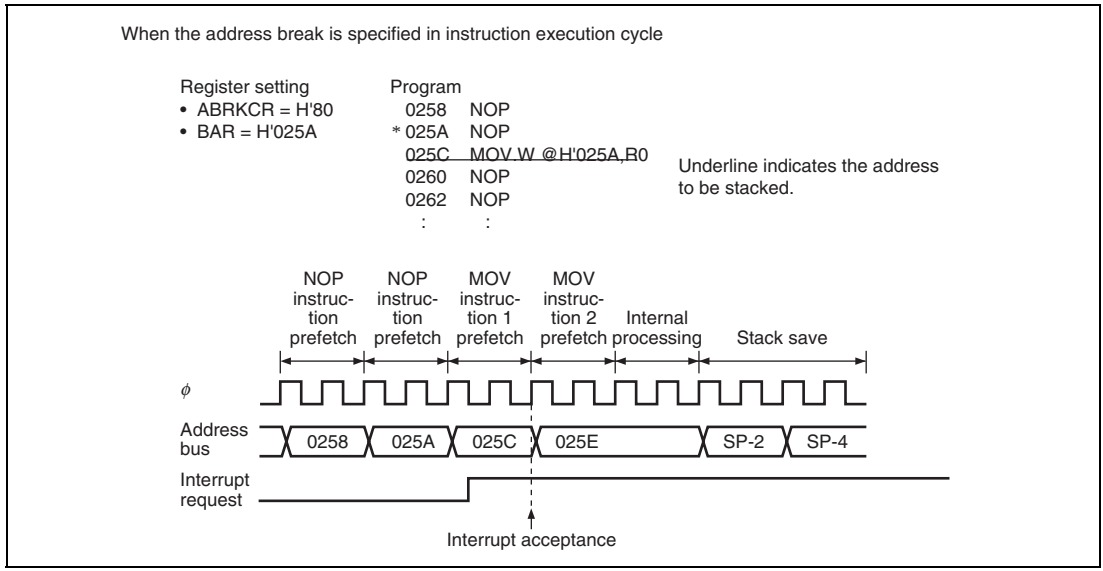



**Figure 4.2 Address Break Interrupt Operation Example (1)**

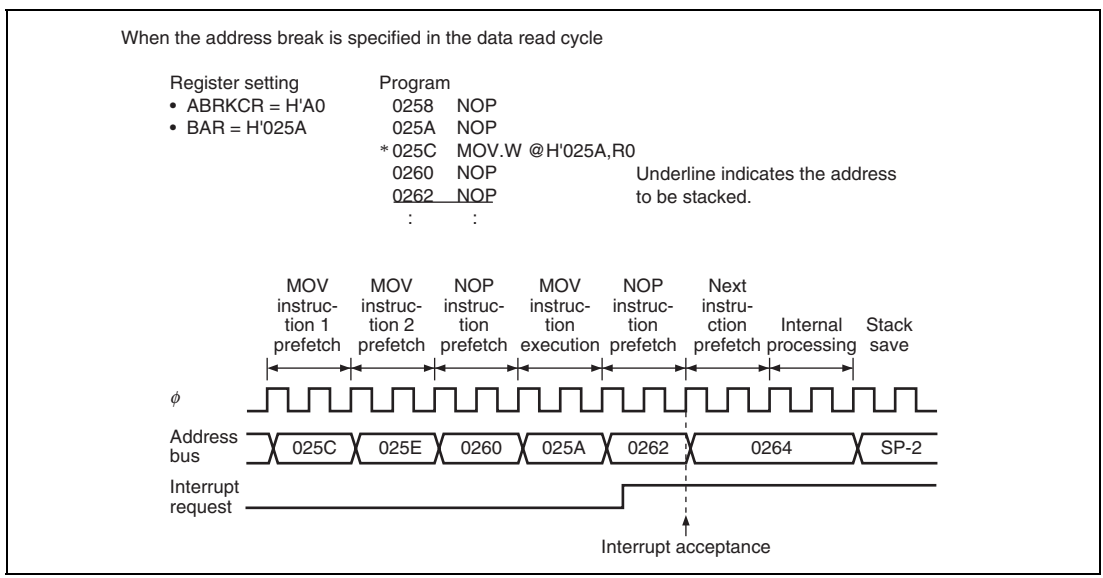



**Figure 4.2 Address Break Interrupt Operation Example (2)**

## 7.5 Program/Erase Protection

There are three kinds of flash memory program/erase protection; hardware protection, software protection, and error protection.

### 7.5.1 Hardware Protection

Hardware protection refers to a state in which programming/erasing of flash memory is forcibly disabled or aborted because of a transition to reset, subsleep mode or standby mode. Flash memory control register 1 (FLMCR1), flash memory control register 2 (FLMCR2), and erase block register 1 (EBR1) are initialized. In a reset via the $\overline{\text{RES}}$ pin, the reset state is not entered unless the $\overline{\text{RES}}$ pin is held low until oscillation stabilizes after powering on. In the case of a reset during operation, hold the $\overline{\text{RES}}$ pin low for the $\overline{\text{RES}}$ pulse width specified in the AC Characteristics section.

### 7.5.2 Software Protection

Software protection can be implemented against programming/erasing of all flash memory blocks by clearing the SWE bit in FLMCR1. When software protection is in effect, setting the P or E bit in FLMCR1 does not cause a transition to program mode or erase mode. By setting the erase block register 1 (EBR1), erase protection can be set for individual blocks. When EBR1 is set to H'00, erase protection is set for all blocks.

### 7.5.3 Error Protection

In error protection, an error is detected when CPU runaway occurs during flash memory programming/erasing, or operation is not performed in accordance with the program/erase algorithm, and the program/erase operation is aborted. Aborting the program/erase operation prevents damage to the flash memory due to overprogramming or overerasing.

When the following errors are detected during programming/erasing of flash memory, the FLER bit in FLMCR2 is set to 1, and the error protection state is entered.

- When the flash memory of the relevant address area is read during programming/erasing (including vector read and instruction fetch)
- Immediately after exception handling excluding a reset during programming/erasing
- When a SLEEP instruction is executed during programming/erasing

### 9.4.3 Pin Functions

The correspondence between the register specification and the port functions is shown below.

- P76/TMOV pin

| Register | TCSRV | PCR7 | |
|---|---|---|---|
| **Bit Name** | **OS3 to OS0** | **PCR76** | **Pin Function** |
| Setting Value | 0000 | 0 | P76 input pin |
| | | 1 | P76 output pin |
| | Other than the above values | X | TMOV output pin |

Legend X: Don't care.

- P75/TMCIV pin

| Register | PCR7 | |
|---|---|---|
| **Bit Name** | **PCR75** | **Pin Function** |
| Setting Value | 0 | P75 input/TMCIV input pin |
| | 1 | P75 output/TMCIV input pin |

- P74/TMRIV pin

| Register | PCR7 | |
|---|---|---|
| **Bit Name** | **PCR74** | **Pin Function** |
| Setting Value | 0 | P74 input/TMRIV input pin |
| | 1 | P74 output/TMRIV input pin |

- P73 pin

| Register | PCR7 | |
|---|---|---|
| **Bit Name** | **PCR73** | **Pin Function** |
| Setting Value | 0 | P73 input pin |
| | 1 | P73 output pin |

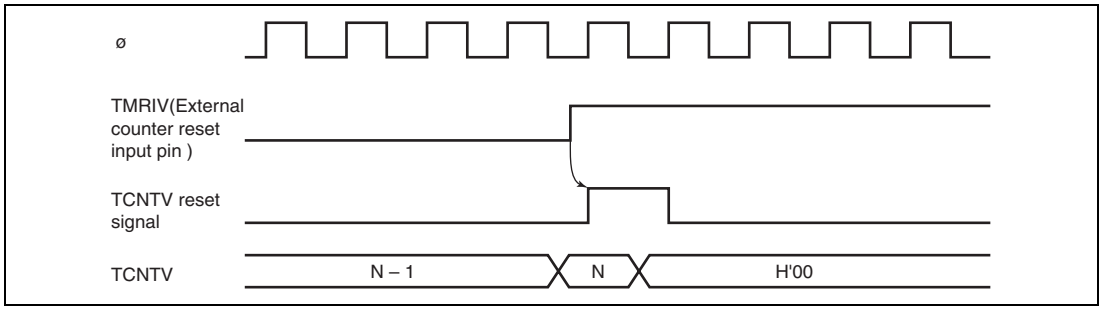



**Figure 10.8 Clear Timing by TMRIV Input**

### 11.4.2 PWM Operation

In PWM mode, PWM waveforms are generated by using GRA as the period register and GRB, GRC, and GRD as duty registers. PWM waveforms are output from the FTIOB, FTIOC, and FTIOD pins. Up to three-phase PWM waveforms can be output. In PWM mode, a general register functions as an output compare register automatically. The output level of each pin depends on the corresponding timer output level set bit (TOB, TOC, and TOD) in TCRW. When TOB is 1, the FTIOB output goes to 1 at compare match A and to 0 at compare match B. When TOB is 0, the FTIOB output goes to 0 at compare match A and to 1 at compare match B. Thus the compare match output level settings in TIOR0 and TIOR1 are ignored for the output pin set to PWM mode. If the same value is set in the cycle register and the duty register, the output does not change when a compare match occurs.

Figure 11.9 shows an example of operation in PWM mode. The output signals go to 1 and TCNT is cleared at compare match A, and the output signals go to 0 at compare match B, C, and D (TOB, TOC, and TOD = 1: initial output values are set to 1).

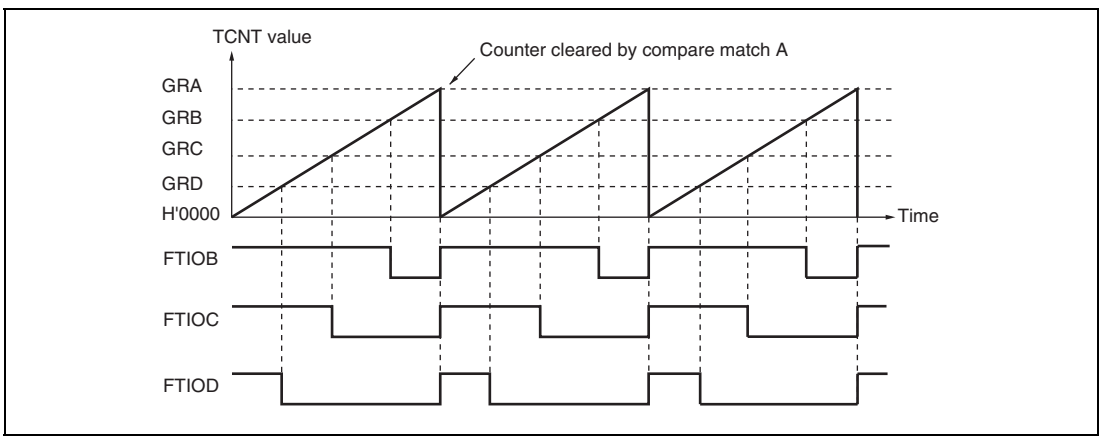



**Figure 11.9 PWM Mode Example (1)**

## 13.6 Multiprocessor Communication Function

Use of the multiprocessor communication function enables data transfer between a number of processors sharing communication lines by asynchronous serial communication using the multiprocessor format, in which a multiprocessor bit is added to the transfer data. When multiprocessor communication is performed, each receiving station is addressed by a unique ID code. The serial communication cycle consists of two component cycles; an ID transmission cycle that specifies the receiving station, and a data transmission cycle. The multiprocessor bit is used to differentiate between the ID transmission cycle and the data transmission cycle. If the multiprocessor bit is 1, the cycle is an ID transmission cycle; if the multiprocessor bit is 0, the cycle is a data transmission cycle. Figure 13.15 shows an example of inter-processor communication using the multiprocessor format. The transmitting station first sends the ID code of the receiving station with which it wants to perform serial communication as data with a 1 multiprocessor bit added. It then sends transmit data as data with a 0 multiprocessor bit added. When data with a 1 multiprocessor bit is received, the receiving station compares that data with its own ID. The station whose ID matches then receives the data sent next. Stations whose IDs do not match continue to skip data until data with a 1 multiprocessor bit is again received.

The SCI3 uses the MPIE bit in SCR3 to implement this function. When the MPIE bit is set to 1, transfer of receive data from RSR to RDR, error flag detection, and setting the SSR status flags, RDRF, FER, and OER, to 1, are inhibited until data with a 1 multiprocessor bit is received. On reception of a receive character with a 1 multiprocessor bit, the MPBR bit in SSR is set to 1 and the MPIE bit is automatically cleared, thus normal reception is resumed. If the RIE bit in SCR3 is set to 1 at this time, an RXI interrupt is generated.

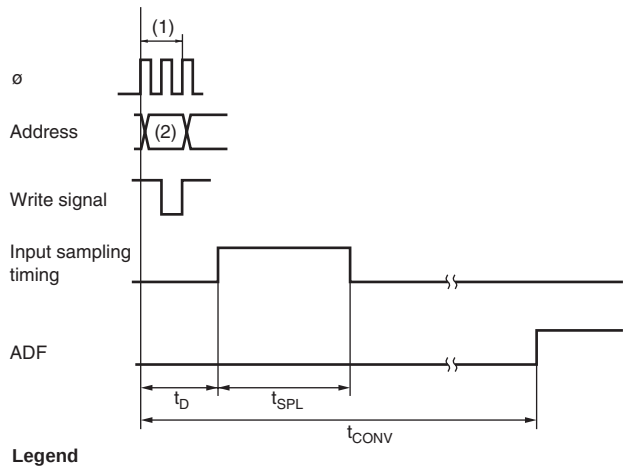
When the multiprocessor format is selected, the parity bit setting is rendered invalid. All other bit settings are the same as those in normal asynchronous mode. The clock used for multiprocessor communication is the same as that in normal asynchronous mode.

### 14.4.3 Input Sampling and A/D Conversion Time

The A/D converter has a built-in sample-and-hold circuit. The A/D converter samples the analog input when the A/D conversion start delay time ($t_D$) has passed after the ADST bit is set to 1, then starts conversion. Figure 14.2 shows the A/D conversion timing. Table 14.3 shows the A/D conversion time.

As indicated in figure 14.2, the A/D conversion time includes $t_D$ and the input sampling time. The length of $t_D$ varies depending on the timing of the write access to ADCSR. The total conversion time therefore varies within the ranges indicated in table 14.3.

In scan mode, the values given in table 14.3 apply to the first conversion time. In the second and subsequent conversions, the conversion time is 128 states (fixed) when CKS = 0 and 66 states (fixed) when CKS = 1.




**Legend**
(1) : ADCSR write cycle
(2) : ADCSR address
$t_D$ : A/D conversion start delay
$t_{SPL}$ : Input sampling time
$t_{CONV}$ : A/D conversion time

**Figure 14.2 A/D Conversion Timing**

## Table 18.4 Serial Interface (SCI3) Timing

$V_{CC}$ = 3.0 V to 5.5 V, $V_{SS}$ = 0.0 V, $T_a$ = –20°C to +75°C, unless otherwise specified.

| Item | | Symbol | Applicable Pins | Test Condition | Values Min | Typ | Max | Unit | Reference Figure |
|---|---|---|---|---|---|---|---|---|---|
| Input clock cycle | Asynchronous | $t_{Scyc}$ | SCK3, SCK3_2, SCK3_3* | | 4 | — | — | $t_{cyc}$ | Figure 18.4 |
| | Clocked synchronous | | | | 6 | — | — | $t_{cyc}$ | |
| Input clock pulse width | | $t_{SCKW}$ | SCK3, SCK3_2, SCK3_3* | | 0.4 | — | 0.6 | $t_{Scyc}$ | |
| Transmit data delay time (clocked synchronous) | | $t_{TXD}$ | TXD, TXD_2, TXD_3* | $V_{CC}$ = 4.0 V to 5.5 V | — | — | 1 | $t_{cyc}$ | Figure 18.5 |
| | | | | | — | — | 1 | $t_{cyc}$ | |
| Receive data setup time (clocked synchronous) | | $t_{RXS}$ | RXD, RXD_2, RXD_3* | $V_{CC}$ = 4.0 V to 5.5 V | 50.0 | — | — | ns | |
| | | | | | 100.0 | — | — | ns | |
| Receive data hold time (clocked synchronous) | | $t_{RXH}$ | RXD, RXD_2, RXD_3* | $V_{CC}$ = 4.0 V to 5.5 V | 50.0 | — | — | ns | |
| | | | | | 100.0 | — | — | ns | |

Note: * The SCK3_3, RXD_3, and TXD_3 pins are not available in the H8/36014.

### 18.2.6 Flash Memory Characteristics

**Table 18.7 Flash Memory Characteristics**

$V_{CC}$ = 3.0 V to 5.5 V, $V_{SS}$ = 0.0 V, $T_a$ = –20°C to +75°C, unless otherwise specified.

| Item | | Symbol | Test Condition | Values Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Programming time (per 128 bytes)*1*2*4 | | $t_P$ | | — | 7 | 200 | ms |
| Erase time (per block) *1*3*6 | | $t_E$ | | — | 100 | 1200 | ms |
| Reprogramming count | | $N_{WEC}$ | | 1000 | 10000 | — | Times |
| Programming | Wait time after SWE bit setting*1 | x | | 1 | — | — | µs |
| | Wait time after PSU bit setting*1 | y | | 50 | — | — | µs |
| | Wait time after P bit setting *1*4 | z1 | 1 ≤ n ≤ 6 | 28 | 30 | 32 | µs |
| | | z2 | 7 ≤ n ≤ 1000 | 198 | 200 | 202 | µs |
| | | z3 | Additional-programming | 8 | 10 | 12 | µs |
| | Wait time after P bit clear*1 | α | | 5 | — | — | µs |
| | Wait time after PSU bit clear*1 | β | | 5 | — | — | µs |
| | Wait time after PV bit setting*1 | γ | | 4 | — | — | µs |
| | Wait time after dummy write*1 | ε | | 2 | — | — | µs |
| | Wait time after PV bit clear*1 | η | | 2 | — | — | µs |
| | Wait time after SWE bit clear*1 | θ | | 100 | — | — | µs |
| | Maximum programming count*1*4*5 | N | | — | — | 1000 | Times |

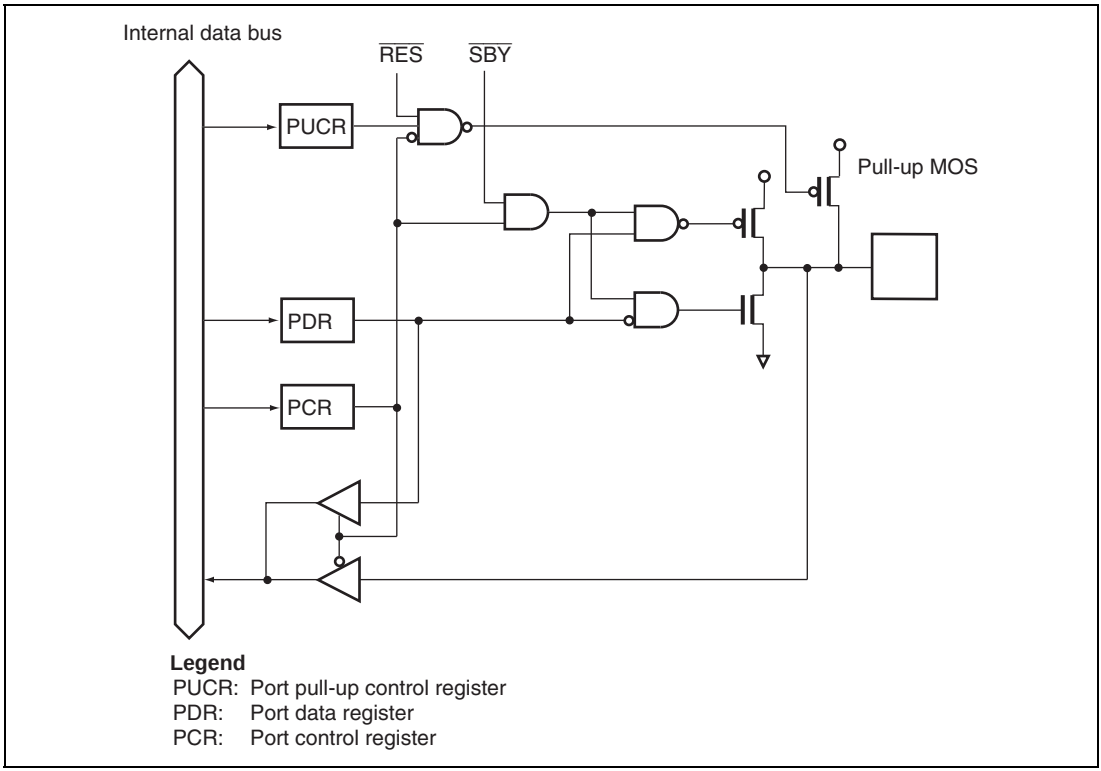



**Figure B.3 Port 1 Block Diagram (P16, P15, P12*, P10)**

Note: * This pin is available only in the H8/36014.