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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | H8/300H |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | SCI |
| Peripherals | LVD, POR, PWM, WDT |
| Number of I/O | 30 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 4x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LFQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/df36014gfpwv |

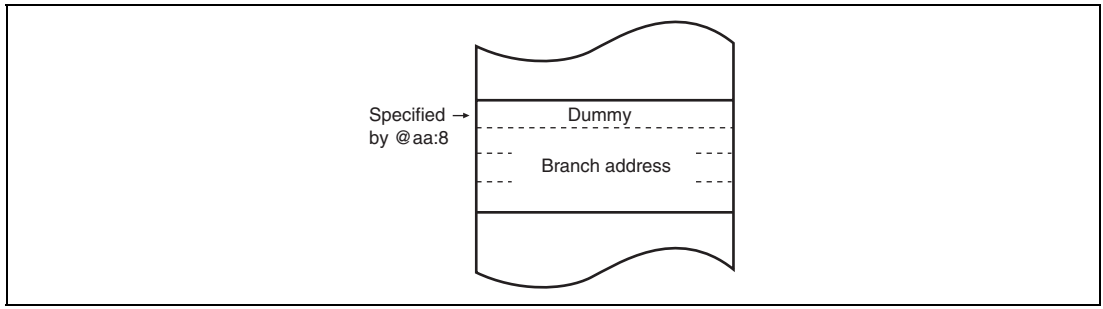



**Figure 2.8 Branch Address Specification in Memory Indirect Mode**

### 2.5.2 Effective Address Calculation

Table 2.12 indicates how effective addresses are calculated in each addressing mode. In this LSI the upper 8 bits of the effective address are ignored in order to generate a 16-bit effective address.

**Table 2.12 Effective Address Calculation (1)**

| No | Addressing Mode and Instruction Format | Effective Address Calculation | Effective Address (EA) |
|---|---|---|---|
| 1 | Register direct(Rn)<br>op \| rm \| rn | | Operand is general register contents. |
| 2 | Register indirect(@ERn)<br>op \| r | 31 … 0: General register contents | 23 … 0 |
| 3 | Register indirect with displacement<br>@(d:16,ERn) or @(d:24,ERn)<br>op \| r \| disp | 31 … 0: General register contents<br>31 … 0: Sign extension \| disp | 23 … 0 |
| 4 | Register indirect with post-increment or pre-decrement<br>•Register indirect with post-increment @ERn+<br>op \| r<br>•Register indirect with pre-decrement @-ERn<br>op \| r | 31 … 0: General register contents ± 1, 2, or 4<br>The value to be added or subtracted is 1 when the operand is byte size, 2 for word size, and 4 for longword size. | 23 … 0 |

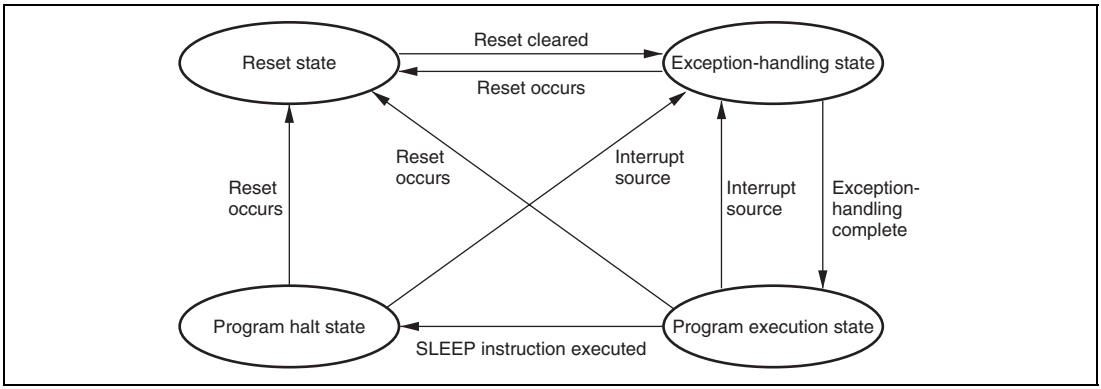



**Figure 2.12 State Transitions**

## 2.8 Usage Notes

### 2.8.1 Notes on Data Access to Empty Areas

The address space of this LSI includes empty areas in addition to the ROM, RAM, and on-chip I/O registers areas available to the user. When data is transferred from CPU to empty areas, the transferred data will be lost. This action may also cause the CPU to malfunction. When data is transferred from an empty area to CPU, the contents of the data cannot be guaranteed.

### 2.8.2 EEPMOV Instruction

EEPMOV is a block-transfer instruction and transfers the byte size of data indicated by R4L, which starts from the address indicated by R5, to the address indicated by R6. Set R4L and R6 so that the end address of the destination address (value of R6 + R4L) does not exceed H'FFFF (the value of R6 must not change from H'FFFF to H'0000 during execution).

### 2.8.3 Bit Manipulation Instruction

The BSET, BCLR, BNOT, BST, and BIST instructions read data from the specified address in byte units, manipulate the data of the target bit, and write data to the same address again in byte units. Special care is required when using these instructions in cases where two registers are assigned to the same address or when a bit is directly manipulated for a port, because this may rewrite data of a bit other than the bit to be manipulated.

### 3.2.3 Interrupt Enable Register 1 (IENR1)

IENR1 enables direct transition interrupts, and external pin interrupts.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | IENDT | 0 | R/W | Direct Transfer Interrupt Enable<br>When this bit is set to 1, direct transition interrupt requests are enabled. |
| 6 | — | 0 | — | Reserved<br>This bit is always read as 0. |
| 5 | IENWP | 0 | R/W | Wakeup Interrupt Enable<br>This bit is an enable bit, which is common to the pins $\overline{\text{WKP5}}$ to $\overline{\text{WKP0}}$. When the bit is set to 1, interrupt requests are enabled. |
| 4 | — | 1 | — | Reserved<br>This bit is always read as 1. |
| 3 | IEN3 | 0 | R/W | IRQ3 Interrupt Enable<br>When this bit is set to 1, interrupt requests of the $\overline{\text{IRQ3}}$ pin are enabled. |
| 2, 1 | — | All 0 | — | Reserved<br>These bits are always read as 0. |
| 0 | IEN0 | 0 | R/W | IRQ0 Interrupt Enable<br>When this bit is set to 1, interrupt requests of the $\overline{\text{IRQ0}}$ pin are enabled. |

When disabling interrupts by clearing bits in an interrupt enable register, or when clearing bits in an interrupt flag register, always do so while interrupts are masked (I = 1). If the above clear operations are performed while I = 0, and as a result a conflict arises between the clear instruction and an interrupt request, exception handling for the interrupt will be executed after the clear instruction has been executed.

## 7.2 Register Descriptions

The flash memory has the following registers.

- Flash memory control register 1 (FLMCR1)
- Flash memory control register 2 (FLMCR2)
- Erase block register 1 (EBR1)
- Flash memory enable register (FENR)

### 7.2.1 Flash Memory Control Register 1 (FLMCR1)

FLMCR1 is a register that makes the flash memory change to program mode, program-verify mode, erase mode, or erase-verify mode. For details on register setting, refer to section 7.4, Flash Memory Programming/Erasing.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | — | 0 | — | Reserved<br>This bit is always read as 0. |
| 6 | SWE | 0 | R/W | Software Write Enable<br>When this bit is set to 1, flash memory programming/erasing is enabled. When this bit is cleared to 0, other FLMCR1 register bits and all EBR1 bits cannot be set. |
| 5 | ESU | 0 | R/W | Erase Setup<br>When this bit is set to 1, the flash memory changes to the erase setup state. When it is cleared to 0, the erase setup state is cancelled. Set this bit to 1 before setting the E bit to 1 in FLMCR1. |
| 4 | PSU | 0 | R/W | Program Setup<br>When this bit is set to 1, the flash memory changes to the program setup state. When it is cleared to 0, the program setup state is cancelled. Set this bit to 1 before setting the P bit in FLMCR1. |
| 3 | EV | 0 | R/W | Erase-Verify<br>When this bit is set to 1, the flash memory changes to erase-verify mode. When it is cleared to 0, erase-verify mode is cancelled. |

- P50/$\overline{\text{WKP0}}$ pin

| Register | PMR5 | PCR5 | |
|---|---|---|---|
| **Bit Name** | **WKP0** | **PCR50** | **Pin Function** |
| Setting Value | 0 | 0 | P50 input pin |
| | | 1 | P50 output pin |
| | 1 | X | $\overline{\text{WKP0}}$ input pin |

Legend X: Don't care.

## 9.4 Port 7

Port 7 is a general I/O port also functioning as a timer V I/O pin. Each pin of the port 7 is shown in figure 9.4. The register setting of TCSRV in timer V has priority for functions of pin P76/TMOV. The pins, P75/TMCIV and P74/TMRIV, are also functioning as timer V input ports that are connected to the timer V regardless of the register setting of port 7.

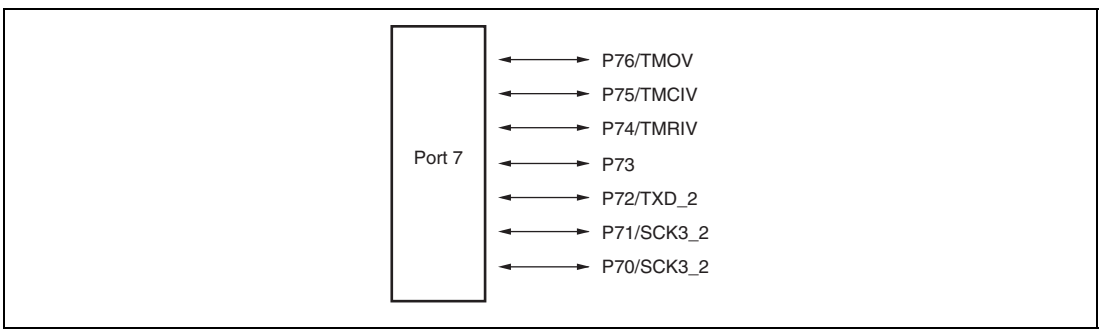



**Figure 9.4 Port 7 Pin Configuration**

Port 7 has the following registers.

- Port control register 7 (PCR7)
- Port data register 7 (PDR7)

### 9.4.3 Pin Functions

The correspondence between the register specification and the port functions is shown below.

- P76/TMOV pin

| Register | TCSRV | PCR7 | |
|---|---|---|---|
| **Bit Name** | **OS3 to OS0** | **PCR76** | **Pin Function** |
| Setting Value | 0000 | 0 | P76 input pin |
| | | 1 | P76 output pin |
| | Other than the above values | X | TMOV output pin |

Legend X: Don't care.

- P75/TMCIV pin

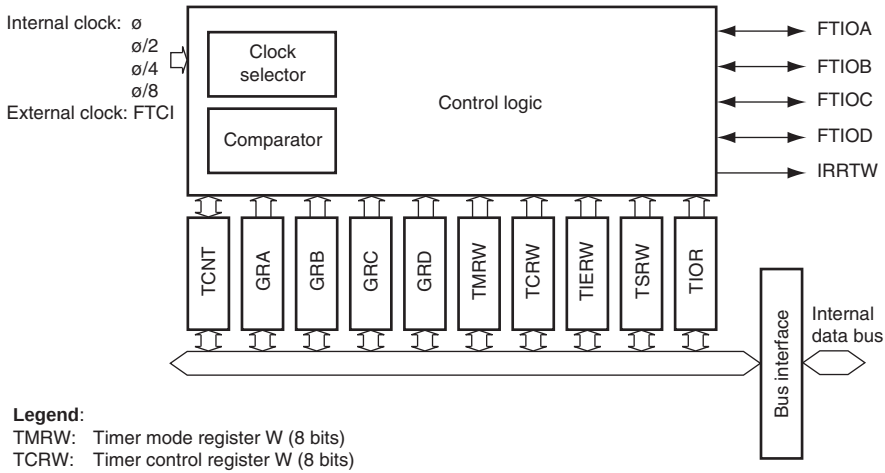
| Register | PCR7 | |
|---|---|---|
| **Bit Name** | **PCR75** | **Pin Function** |
| Setting Value | 0 | P75 input/TMCIV input pin |
| | 1 | P75 output/TMCIV input pin |

- P74/TMRIV pin

| Register | PCR7 | |
|---|---|---|
| **Bit Name** | **PCR74** | **Pin Function** |
| Setting Value | 0 | P74 input/TMRIV input pin |
| | 1 | P74 output/TMRIV input pin |

- P73 pin

| Register | PCR7 | |
|---|---|---|
| **Bit Name** | **PCR73** | **Pin Function** |
| Setting Value | 0 | P73 input pin |
| | 1 | P73 output pin |




**Legend**:
TMRW: Timer mode register W (8 bits)
TCRW: Timer control register W (8 bits)
TIERW: Timer interrupt enable register W (8 bits)
TSRW: Timer status register W (8 bits)
TIOR: Timer I/O control register (8 bits)
TCNT: Timer counter (16 bits)
GRA: General register A (input capture/output compare register: 16 bits)
GRB: General register B (input capture/output compare register: 16 bits)
GRC: General register C (input capture/output compare register: 16 bits)
GRD: General register D (input capture/output compare register: 16 bits)
IRRTW: Timer W interrupt request

**Figure 11.1 Timer W Block Diagram**

The TCNT value can be captured into a general register (GRA, GRB, GRC, or GRD) when a signal level changes at an input-capture pin (FTIOA, FTIOB, FTIOC, or FTIOD). Capture can take place on the rising edge, falling edge, or both edges. By using the input-capture function, the pulse width and periods can be measured. Figure 11.7 shows an example of input capture when both edges of FTIOA and the falling edge of FTIOB are selected as capture edges. TCNT operates as a free-running counter.

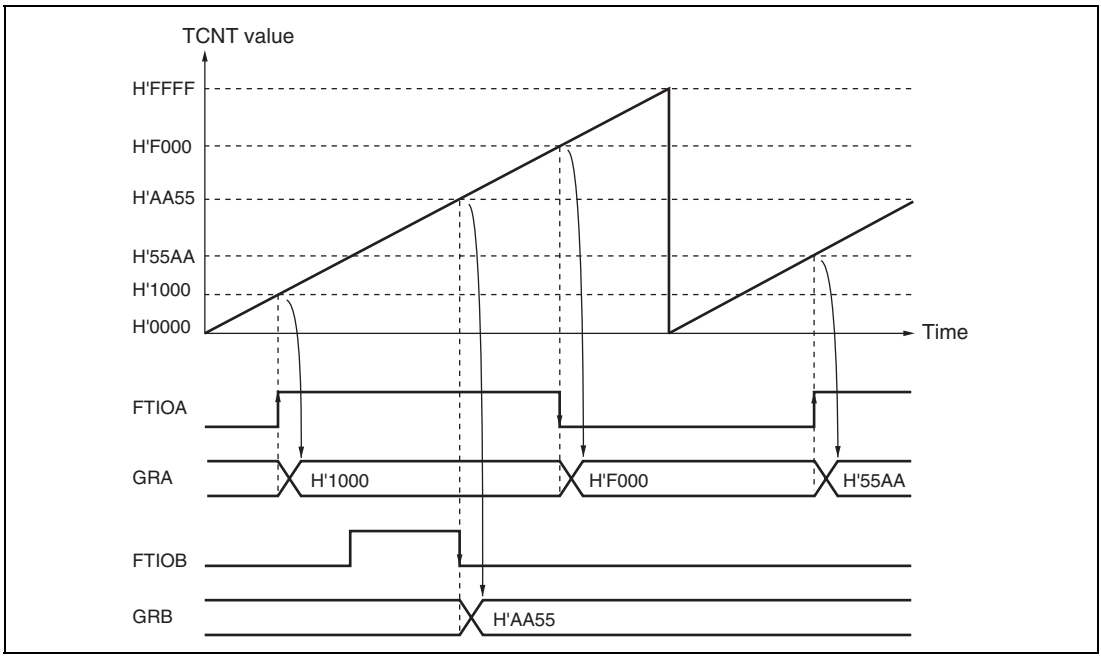



**Figure 11.7 Input Capture Operating Example**

### 13.3.5 Serial Mode Register (SMR)

SMR is used to set the SCI3's serial transfer format and select the baud rate generator clock source.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | COM | 0 | R/W | Communication Mode<br>0: Asynchronous mode<br>1: Clocked synchronous mode |
| 6 | CHR | 0 | R/W | Character Length (enabled only in asynchronous mode)<br>0: Selects 8 bits as the data length.<br>1: Selects 7 bits as the data length. |
| 5 | PE | 0 | R/W | Parity Enable (enabled only in asynchronous mode)<br>When this bit is set to 1, the parity bit is added to transmit data before transmission, and the parity bit is checked in reception. |
| 4 | PM | 0 | R/W | Parity Mode (enabled only when the PE bit is 1 in asynchronous mode)<br>0: Selects even parity.<br>1: Selects odd parity. |
| 3 | STOP | 0 | R/W | Stop Bit Length (enabled only in asynchronous mode)<br>Selects the stop bit length in transmission.<br>0: 1 stop bit<br>1: 2 stop bits<br>For reception, only the first stop bit is checked, regardless of the value in the bit. If the second stop bit is 0, it is treated as the start bit of the next transmit character. |
| 2 | MP | 0 | R/W | Multiprocessor Mode<br>When this bit is set to 1, the multiprocessor communication function is enabled. The PE bit and PM bit settings are invalid in multiprocessor mode. In clocked synchronous mode, clear this bit to 0. |

## 13.4 Operation in Asynchronous Mode

Figure 13.2 shows the general format for asynchronous serial communication. One character (or frame) consists of a start bit (low level), followed by data (in LSB-first order), a parity bit (high or low level), and finally stop bits (high level). Inside the SCI3, the transmitter and receiver are independent units, enabling full-duplex. Both the transmitter and the receiver also have a double-buffered structure, so data can be read or written during transmission or reception, enabling continuous data transfer.

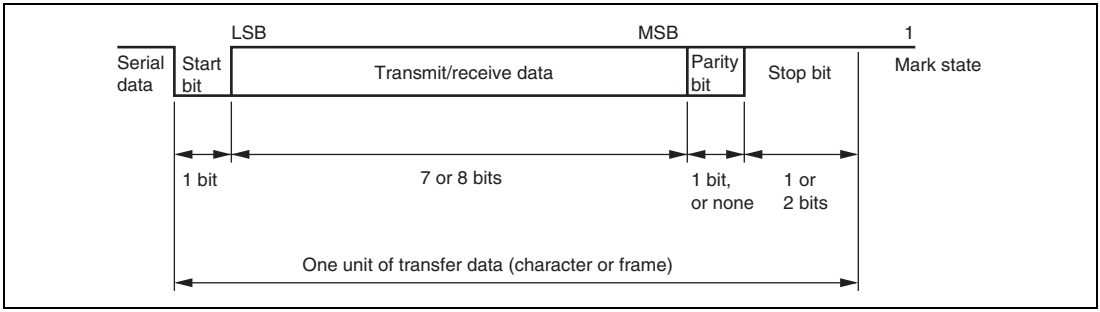



**Figure 13.2 Data Format in Asynchronous Communication**

### 13.4.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external clock input at the SCK3 pin can be selected as the SCI3's serial clock, according to the setting of the COM bit in SMR and the CKE0 and CKE1 bits in SCR3. When an external clock is input at the SCK3 pin, the clock frequency should be 16 times the bit rate used.

When the SCI3 is operated on an internal clock, the clock can be output from the SCK3 pin. The frequency of the clock output in this case is equal to the bit rate, and the phase is such that the rising edge of the clock is in the middle of the transmit data, as shown in figure 13.3.

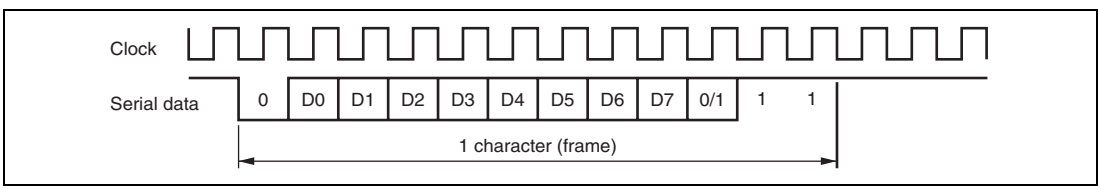
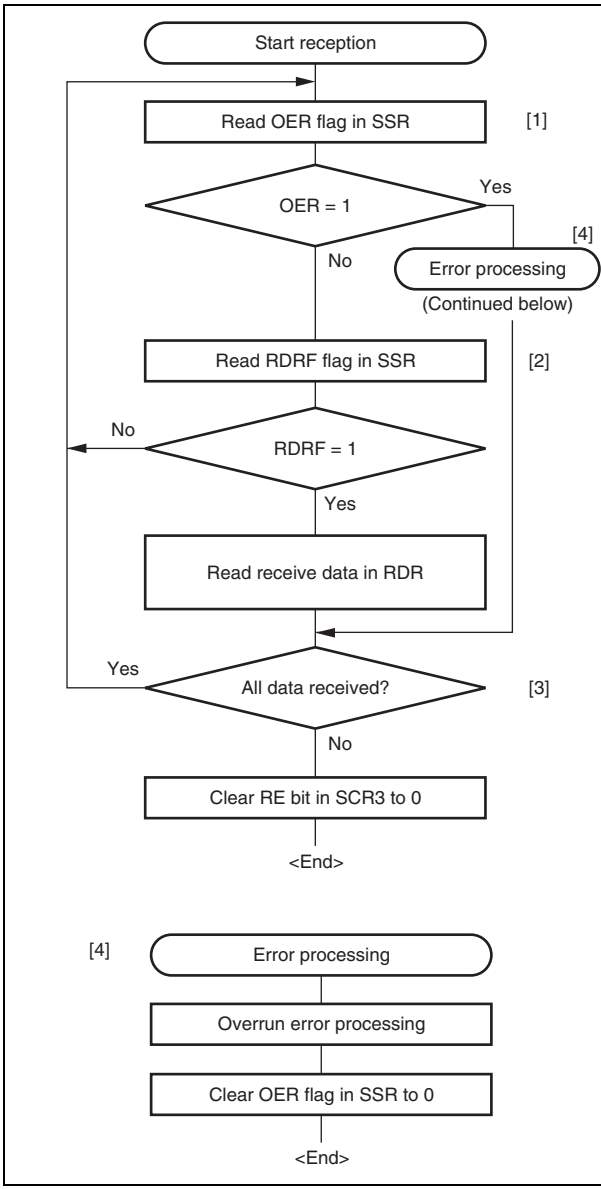



**Figure 13.3 Relationship between Output Clock and Transfer Data Phase (Asynchronous Mode)(Example with 8-Bit Data, Parity, Two Stop Bits)**




[1] Read the OER flag in SSR to determine if there is an error. If an overrun error has occurred, execute overrun error processing.

[2] Read SSR and check that the RDRF flag is set to 1, then read the receive data in RDR. When data is read from RDR, the RDRF flag is automatically cleared to 0.

[3] To continue serial reception, before the MSB (bit 7) of the current frame is received, reading the RDRF flag and reading RDR should be finished. When data is read from RDR, the RDRF flag is automatically cleared to 0.

[4] If an overrun error occurs, read the OER flag in SSR, and after performing the appropriate error processing, clear the OER flag to 0. Reception cannot be resumed if the OER flag is set to 1.

**Figure 13.13 Sample Serial Reception Flowchart (Clocked Synchronous Mode)**

## 13.7 Interrupts

SCI3 creates the following six interrupt requests: transmission end, transmit data empty, receive data full, and receive errors (overrun error, framing error, and parity error). Table 13.7 shows the interrupt sources.

**Table 13.7 SCI3 Interrupt Requests**

| Interrupt Requests | Abbreviation | Interrupt Sources |
|---|---|---|
| Receive Data Full | RXI | Setting RDRF in SSR |
| Transmit Data Empty | TXI | Setting TDRE in SSR |
| Transmission End | TEI | Setting TEND in SSR |
| Receive Error | ERI | Setting OER, FER, and PER in SSR |

The initial value of the TDRE flag in SSR is 1. Thus, when the TIE bit in SCR3 is set to 1 before transferring the transmit data to TDR, a TXI interrupt request is generated even if the transmit data is not ready. The initial value of the TEND flag in SSR is 1. Thus, when the TEIE bit in SCR3 is set to 1 before transferring the transmit data to TDR, a TEI interrupt request is generated even if the transmit data has not been sent. It is possible to make use of the most of these interrupt requests efficiently by transferring the transmit data to TDR in the interrupt routine. To prevent the generation of these interrupt requests (TXI and TEI), set the enable bits (TIE and TEIE) that correspond to these interrupt requests to 1, after transferring the transmit data to TDR.

## 13.8 Usage Notes

### 13.8.1 Break Detection and Processing

When framing error detection is performed, a break can be detected by reading the RXD pin value directly. In a break, the input from the RXD pin becomes all 0s, setting the FER flag, and possibly the PER flag. Note that as the SCI3 continues the receive operation after receiving a break, even if the FER flag is cleared to 0, it will be set to 1 again.

### 13.8.2 Mark State and Break Sending

When TE is 0, the TXD pin is used as an I/O port whose direction (input or output) and level are determined by PCR and PDR. This can be used to set the TXD pin to mark state (high level) or send a break during serial data transmission. To maintain the communication line at mark state until TE is set to 1, set both PCR and PDR to 1. As TE is cleared to 0 at this point, the TXD pin becomes an I/O port, and 1 is output from the TXD pin. To send a break during serial transmission, first set PCR to 1 and clear PDR to 0, and then clear TE to 0. When TE is cleared to 0, the transmitter is initialized regardless of the current transmission state, the TXD pin becomes an I/O port, and 0 is output from the TXD pin.

### 13.8.3 Receive Error Flags and Transmit Operations (Clocked Synchronous Mode Only)

Transmission cannot be started when a receive error flag (OER, PER, or FER) is set to 1, even if the TDRE flag is cleared to 0. Be sure to clear the receive error flags to 0 before starting transmission. Note also that receive error flags cannot be cleared to 0 even if the RE bit is cleared to 0.

## 14.5 A/D Conversion Accuracy Definitions

This LSI's A/D conversion accuracy definitions are given below.

- Resolution

  The number of A/D converter digital output codes
- Quantization error

  The deviation inherent in the A/D converter, given by 1/2 LSB (see figure 14.4).
- Offset error

  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from the minimum voltage value 0000000000 to 0000000001 (see figure 14.5).
- Full-scale error

  The deviation of the analog input voltage value from the ideal A/D conversion characteristic when the digital output changes from 1111111110 to 1111111111 (see figure 14.5).
- Nonlinearity error

  The error with respect to the ideal A/D conversion characteristics between zero voltage and full-scale voltage. Does not include offset error, full-scale error, or quantization error.
- Absolute accuracy

  The deviation between the digital value and the analog input value. Includes offset error, full-scale error, quantization error, and nonlinearity error.

## 17.1 Register Addresses (Address Order)

The data bus width indicates the numbers of bits by which the register is accessed.

The number of access states indicates the number of states based on the specified reference clock.

| Register Name | Abbre-viation | Bit No | Address | Module Name | Data Bus Width | Access State |
|---|---|---|---|---|---|---|
| Serial mode register_3 | SMR_3 | 8 | H'F600 | SCI3_3 | 8 | 3 |
| Bit rate register_3 | BRR_3 | 8 | H'F601 | SCI3_3 | 8 | 3 |
| Serial control register 3_3 | SCR3_3 | 8 | H'F602 | SCI3_3 | 8 | 3 |
| Transmit data register_3 | TDR_3 | 8 | H'F603 | SCI3_3 | 8 | 3 |
| Serial status register_3 | SSR_3 | 8 | H'F604 | SCI3_3 | 8 | 3 |
| Receive data register_3 | RDR_3 | 8 | H'F605 | SCI3_3 | 8 | 3 |
| — | — | — | H'F606, H'F607 | SCI3_3 | — | — |
| SCI3_3 module control register | SMCR | 8 | H'F608 | SCI3_3 | 8 | 3 |
| Low-voltage-detection control register | LVDCR | 8 | H'F730 | LVDC*[1] | 8 | 2 |
| Low-voltage-detection status register | LVDSR | 8 | H'F731 | LVDC*[1] | 8 | 2 |
| Serial mode register_2 | SMR_2 | 8 | H'F740 | SCI3_2 | 8 | 3 |
| Bit rate register_2 | BRR_2 | 8 | H'F741 | SCI3_2 | 8 | 3 |
| Serial control register 3_2 | SCR3_2 | 8 | H'F742 | SCI3_2 | 8 | 3 |
| Transmit data register_2 | TDR_2 | 8 | H'F743 | SCI3_2 | 8 | 3 |
| Serial status register_2 | SSR_2 | 8 | H'F744 | SCI3_2 | 8 | 3 |
| Receive data register_2 | RDR_2 | 8 | H'F745 | SCI3_2 | 8 | 3 |
| Timer mode register W | TMRW | 8 | H'FF80 | Timer W | 8 | 2 |
| Timer control register W | TCRW | 8 | H'FF81 | Timer W | 8 | 2 |
| Timer interrupt enable register W | TIERW | 8 | H'FF82 | Timer W | 8 | 2 |
| Timer status register W | TSRW | 8 | H'FF83 | Timer W | 8 | 2 |
| Timer I/O control register 0 | TIOR0 | 8 | H'FF84 | Timer W | 8 | 2 |
| Timer I/O control register 1 | TIOR1 | 8 | H'FF85 | Timer W | 8 | 2 |
| Timer counter | TCNT | 16 | H'FF86 | Timer W | 16*[2] | 2 |
| General register A | GRA | 16 | H'FF88 | Timer W | 16*[2] | 2 |

### 18.2.4 A/D Converter Characteristics

**Table 18.5 A/D Converter Characteristics**

$V_{CC}$ = 3.0 V to 5.5 V, $V_{SS}$ = 0.0 V, $T_a$ = –20°C to +75°C, unless otherwise specified.

| Item | Symbol | Applicable Pins | Test Condition | Values | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Analog power supply voltage | $AV_{CC}$ | $AV_{CC}$ | | 3.3 | $V_{CC}$ | 5.5 | V | *1 |
| Analog input voltage | $AV_{IN}$ | AN3 to AN0 | | $V_{SS}$ – 0.3 | — | $AV_{CC}$ + 0.3 | V | |
| Analog power supply current | $AI_{OPE}$ | $AV_{CC}$ | $AV_{CC}$ = 5.0 V<br>$f_{OSC}$ = 20 MHz | — | — | 2.0 | mA | |
| | $AI_{STOP1}$ | $AV_{CC}$ | | — | 50 | — | µA | *2 Reference value |
| | $AI_{STOP2}$ | $AV_{CC}$ | | — | — | 5.0 | µA | *3 |
| Analog input capacitance | $C_{AIN}$ | AN3 to AN0 | | — | — | 30.0 | pF | |
| Allowable signal source impedance | $R_{AIN}$ | AN3 to AN0 | | — | — | 5.0 | kΩ | |
| Resolution (data length) | | | | 10 | 10 | 10 | bit | |
| Conversion time (single mode) | | | $AV_{CC}$ = 3.3 V to 5.5 V | 134 | — | — | $t_{cyc}$ | |
| Nonlinearity error | | | | — | — | ±7.5 | LSB | |
| Offset error | | | | — | — | ±7.5 | LSB | |
| Full-scale error | | | | — | — | ±7.5 | LSB | |
| Quantization error | | | | — | — | ±0.5 | LSB | |
| Absolute accuracy | | | | — | — | ±8.0 | LSB | |
| Conversion time (single mode) | | | $AV_{CC}$ = 4.0 V to 5.5 V | 70 | — | — | $t_{cyc}$ | |
| Nonlinearity error | | | | — | — | ±7.5 | LSB | |
| Offset error | | | | — | — | ±7.5 | LSB | |
| Full-scale error | | | | — | — | ±7.5 | LSB | |
| Quantization error | | | | — | — | ±0.5 | LSB | |
| Absolute accuracy | | | | — | — | ±8.0 | LSB | |

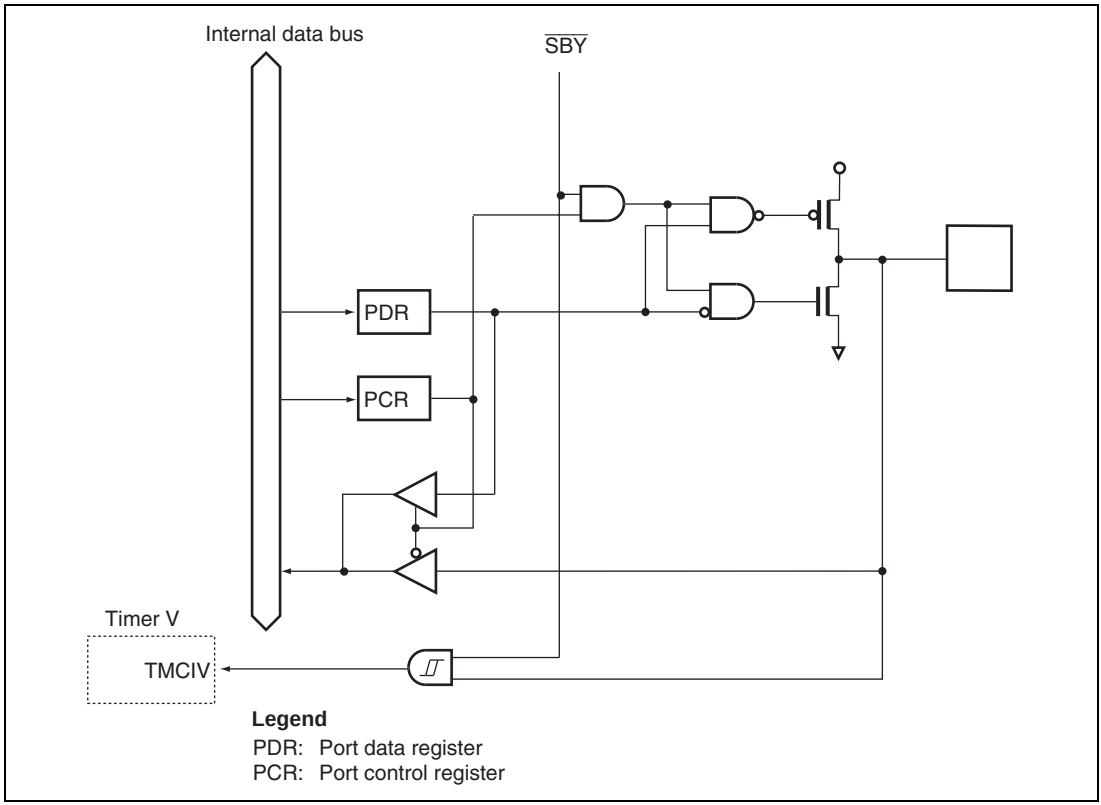
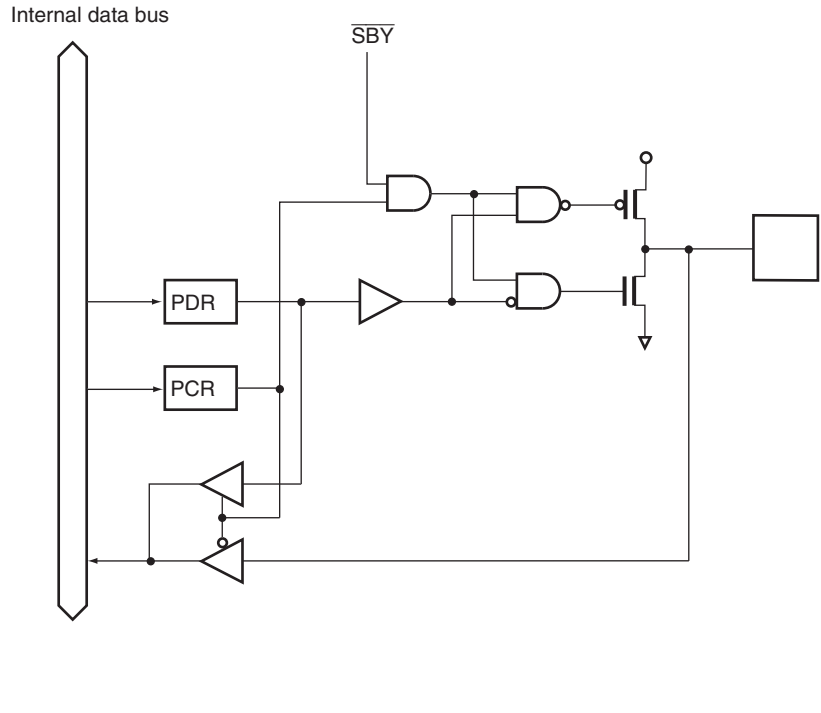



**Figure B.15 Port 7 Block Diagram (P75)**




**Legend**
PDR: Port data register
PCR: Port control register

**Figure B.17 Port 7 Block Diagram (P73)**

| Product Type | | | Product Code | Model Marking | Package Code |
|---|---|---|---|---|---|
| H8/36022 | Flash memory version | Standard product | HD64F36022FP | HD64F36022FP | LQFP-64 (FP-64E) |
| | | | HD64F36022FX | HD64F36022FX | LQFP-48 (FP-48F) |
| | | | HD64F36022FY | HD64F36022FY | LQFP-48 (FP-48B) |
| | | | HD64F36022FT | HD64F36022FT | QFN-48(TNP-48) |
| | | Product with POR & LVDC | HD64F36022GFP | HD64F36022GFP | LQFP-64 (FP-64E) |
| | | | HD64F36022GFX | HD64F36022GFX | LQFP-48 (FP-48F) |
| | | | HD64F36022GFY | HD64F36022GFY | LQFP-48 (FP-48B) |
| | | | HD64F36022GFT | HD64F36022GFT | QFN-48(TNP-48) |
| | Masked ROM version | Standard product | HD64336022FP | HD64336022(***)FP | LQFP-64 (FP-64E) |
| | | | HD64336022FX | HD64336022(***)FX | LQFP-48 (FP-48F) |
| | | | HD64336022FY | HD64336022(***)FY | LQFP-48 (FP-48B) |
| | | | HD64336022FT | HD64336022(***)FT | QFN-48(TNP-48) |
| | | Product with POR & LVDC | HD64336022GFP | HD64336022G(***)FP | LQFP-64 (FP-64E) |
| | | | HD64336022GFX | HD64336022G(***)FX | LQFP-48 (FP-48F) |
| | | | HD64336022GFY | HD64336022G(***)FY | LQFP-48 (FP-48B) |
| | | | HD64336022GFT | HD64336022G(***)FT | QFN-48(TNP-48) |
| H8/36014 | Flash memory version | Standard product | HD64F36014FP | HD64F36014FP | LQFP-64 (FP-64E) |
| | | | HD64F36014FX | HD64F36014FX | LQFP-48 (FP-48F) |
| | | | HD64F36014FY | HD64F36014FY | LQFP-48 (FP-48B) |
| | | | HD64F36014FT | HD64F36014FT | QFN-48(TNP-48) |
| | | Product with POR & LVDC | HD64F36014GFP | HD64F36014GFP | LQFP-64 (FP-64E) |
| | | | HD64F36014GFX | HD64F36014GFX | LQFP-48 (FP-48F) |
| | | | HD64F36014GFY | HD64F36014GFY | LQFP-48 (FP-48B) |
| | | | HD64F36014GFT | HD64F36014GFT | QFN-48(TNP-48) |
| | Masked ROM version | Standard product | HD64336014FP | HD64336014(***)FP | LQFP-64 (FP-64E) |
| | | | HD64336014FX | HD64336014(***)FX | LQFP-48 (FP-48F) |
| | | | HD64336014FY | HD64336014(***)FY | LQFP-48 (FP-48B) |
| | | | HD64336014FT | HD64336014(***)FT | QFN-48(TNP-48) |
| | | Product with POR & LVDC | HD64336014GFP | HD64336014G(***)FP | LQFP-64 (FP-64E) |
| | | | HD64336014GFX | HD64336014G(***)FX | LQFP-48 (FP-48F) |
| | | | HD64336014GFY | HD64336014G(***)FY | LQFP-48 (FP-48B) |
| | | | HD64336014GFT | HD64336014G(***)FT | QFN-48(TNP-48) |

# Appendix D Package Dimensions

The package dimensions that are shows in the Renesas Semiconductor Packages Data Book have priority.