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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	SCI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	30
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN
Supplier Device Package	48-VQFN (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/df36014gftv">https://www.e-xfl.com/product-detail/renesas-electronics-america/df36014gftv</a>

The revision list can be viewed directly by clicking the title page.

The revision list summarizes the locations of revisions and additions. Details should always be checked by referring to the relevant text.

# H8/36024Group, H8/36014Group

## Hardware Manual

### Renesas 16-Bit Single-Chip Microcomputer

### H8 Family/H8/300H Tiny Series

H8/36024F	HD64F36024, HD64F36024G,
H8/36022F	HD64F36022, HD64F36022G,
H8/36014F	HD64F36014, HD64F36014G,
H8/36012F	HD64F36012, HD64F36012G,
H8/36024	HD64336024, HD64336024G,
H8/36023	HD64336023, HD64336023G,
H8/36022	HD64336022, HD64336022G,
H8/36014	HD64336014, HD64336014G,
H8/36013	HD64336013, HD64336013G,
H8/36012	HD64336012, HD64336012G,
H8/36011	HD64336011, HD64336011G,
H8/36010	HD64336010, HD64336010G

# Configuration of This Manual

This manual comprises the following items:

1. General Precautions on Handling of Product
2. Configuration of This Manual
3. Preface
4. Contents
5. Overview
6. Description of Functional Modules

- CPU and System-Control Modules
- On-Chip Peripheral Modules

The configuration of the functional description of each module differs according to the module. However, the generic style includes the following items:

- i) Feature
- ii) Input/Output Pin
- iii) Register Description
- iv) Operation
- v) Usage Note

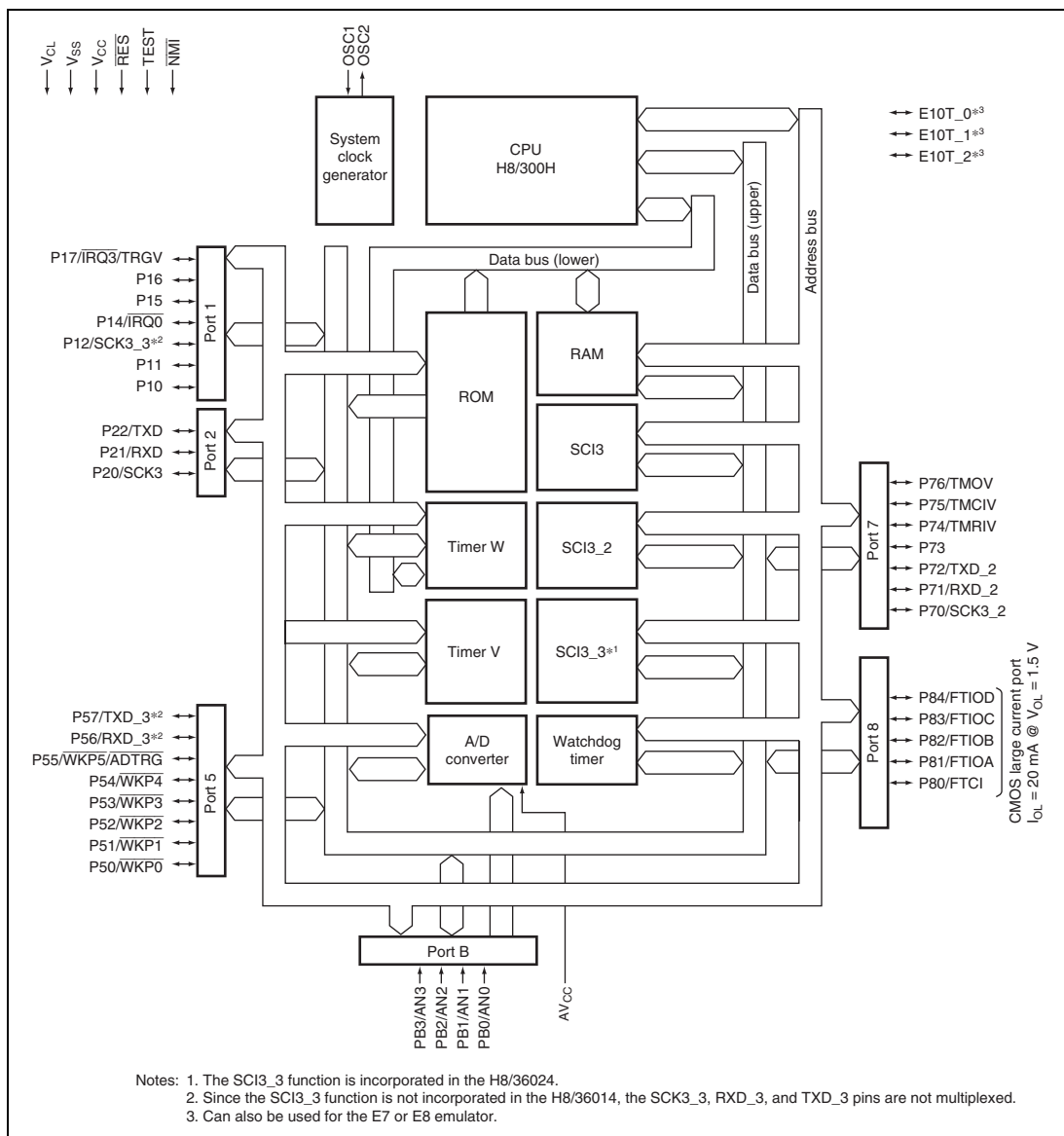
When designing an application system that includes this LSI, take notes into account. Each section includes notes in relation to the descriptions given, and usage notes are given, as required, as the final part of each section.

7. List of Registers
8. Electrical Characteristics
9. Appendix
10. Main Revisions and Additions in this Edition (only for revised versions)

The list of revisions is a summary of points that have been revised or added to earlier versions. This does not include all of the revised contents. For details, see the actual locations in this manual.

11. Index

## 1.2 Internal Block Diagram



**Figure 1.1 Internal Block Diagram**

**Example 2: The BSET instruction is executed for port 5.**

P57 and P56 are input pins, with a low-level signal input at P57 and a high-level signal input at P56. P55 to P50 are output pins and output low-level signals. An example to output a high-level signal at P50 with a BSET instruction is shown below.

- Prior to executing BSET

	<b>P57</b>	<b>P56</b>	<b>P55</b>	<b>P54</b>	<b>P53</b>	<b>P52</b>	<b>P51</b>	<b>P50</b>
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1	1
PDR5	1	0	0	0	0	0	0	0

- BSET instruction executed

```
BSET    #0,    @PDR5
```

The BSET instruction is executed for port 5.

- After executing BSET

	<b>P57</b>	<b>P56</b>	<b>P55</b>	<b>P54</b>	<b>P53</b>	<b>P52</b>	<b>P51</b>	<b>P50</b>
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	High level
PCR5	0	0	1	1	1	1	1	1
PDR5	0	1	0	0	0	0	0	1

- Description on operation

- When the BSET instruction is executed, first the CPU reads port 5.

Since P57 and P56 are input pins, the CPU reads the pin states (low-level and high-level input).

P55 to P50 are output pins, so the CPU reads the value in PDR5. In this example PDR5 has a value of H'80, but the value read by the CPU is H'40.

- Next, the CPU sets bit 0 of the read data to 1, changing the PDR5 data to H'41.
- Finally, the CPU writes H'41 to PDR5, completing execution of BSET.

### 3.2.2 Interrupt Edge Select Register 2 (IEGR2)

IEGR2 selects the direction of an edge that generates interrupt requests of the pins  $\overline{\text{ADTRG}}$  and  $\overline{\text{WKP5}}$  to  $\overline{\text{WKP0}}$ .

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 1	—	Reserved These bits are always read as 1.
5	WPEG5	0	R/W	WKP5 Edge Select 0: Falling edge of $\overline{\text{WKP5}}$ ( $\overline{\text{ADTRG}}$ ) pin input is detected 1: Rising edge of $\overline{\text{WKP5}}$ ( $\overline{\text{ADTRG}}$ ) pin input is detected
4	WPEG4	0	R/W	WKP4 Edge Select 0: Falling edge of $\overline{\text{WKP4}}$ pin input is detected 1: Rising edge of $\overline{\text{WKP4}}$ pin input is detected
3	WPEG3	0	R/W	WKP3 Edge Select 0: Falling edge of $\overline{\text{WKP3}}$ pin input is detected 1: Rising edge of $\overline{\text{WKP3}}$ pin input is detected
2	WPEG2	0	R/W	WKP2 Edge Select 0: Falling edge of $\overline{\text{WKP2}}$ pin input is detected 1: Rising edge of $\overline{\text{WKP2}}$ pin input is detected
1	WPEG1	0	R/W	WKP1 Edge Select 0: Falling edge of $\overline{\text{WKP1}}$ pin input is detected 1: Rising edge of $\overline{\text{WKP1}}$ pin input is detected
0	WPEG0	0	R/W	WKP0 Edge Select 0: Falling edge of $\overline{\text{WKP0}}$ pin input is detected 1: Rising edge of $\overline{\text{WKP0}}$ pin input is detected

### 6.3 Operating Frequency in Active Mode

Operation in active mode is clocked at the frequency designated by the MA2 to MA0 bits in SYSCR2. The operating frequency changes to the set frequency after SLEEP instruction execution.

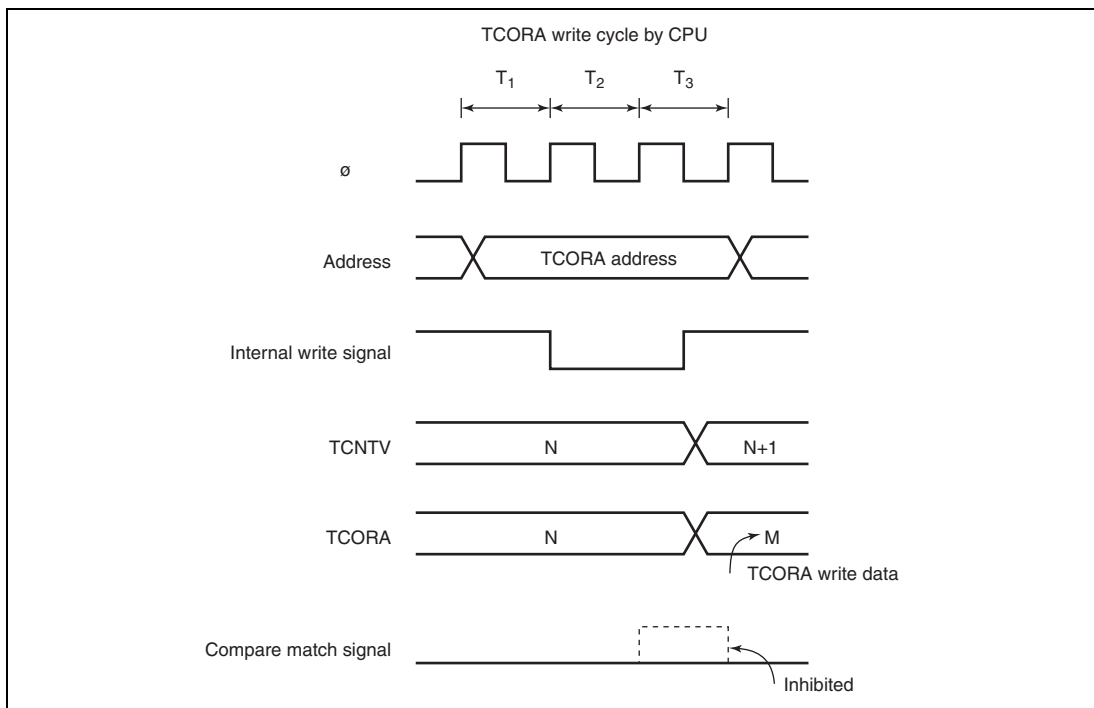
### 6.4 Direct Transition

The CPU can execute programs in active mode. The operating frequency can be changed by making a transition directly from active mode to active mode. A direct transition can be made by executing a SLEEP instruction while the DTON bit in SYSCR2 is set to 1. The direct transition also enables operating frequency modification in active mode. After the mode transition, direct transition interrupt exception handling starts.

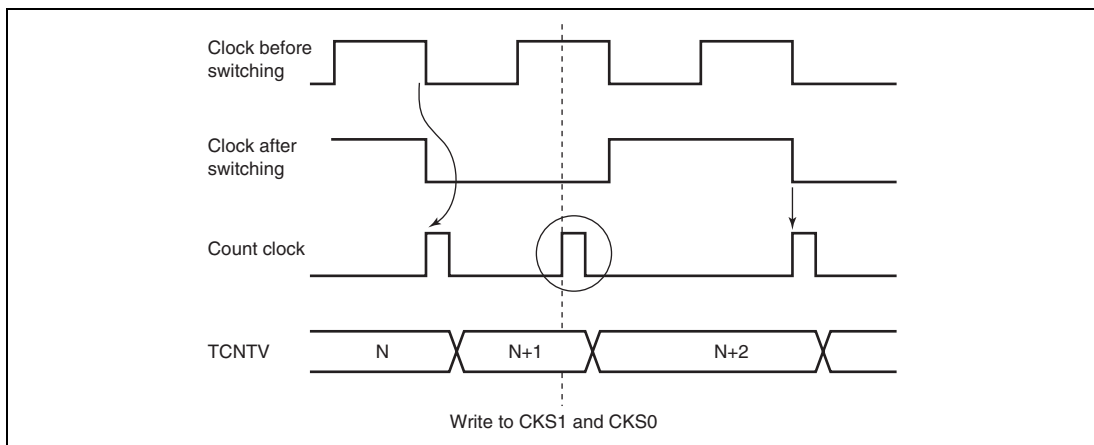
If the direct transition interrupt is disabled in interrupt enable register 1, a transition is made instead to sleep mode. Note that if a direct transition is attempted while the I bit in CCR is set to 1, sleep mode will be entered, and the resulting mode cannot be cleared by means of an interrupt.

### 6.5 Module Standby Function

The module-standby function can be set to any peripheral module. In module standby mode, the clock supply to modules stops to enter the power-down mode. Module standby mode enables each on-chip peripheral module to enter the standby state by setting a bit that corresponds to each module in MSTCR1 and MSTCR2 to 1 and cancels the mode by clearing the bit to 0.



**Figure 10.12 Contention between TCORA Write and Compare Match**



**Figure 10.13 Internal Clock Switching and TCNTV Operation**



### 11.3.7 Timer Counter (TCNT)

TCNT is a 16-bit readable/writable up-counter. The clock source is selected by bits CKS2 to CKS0 in TCRW. TCNT can be cleared to H'0000 through a compare match with GRA by setting the CCLR in TCRW to 1. When TCNT overflows (changes from H'FFFF to H'0000), the OVF flag in TSRW is set to 1. If OVIE in TIERW is set to 1 at this time, an interrupt request is generated. TCNT must always be read or written in 16-bit units; 8-bit access is not allowed. TCNT is initialized to H'0000 by a reset.

### 11.3.8 General Registers A to D (GRA to GRD)

Each general register is a 16-bit readable/writable register that can function as either an output-compare register or an input-capture register. The function is selected by settings in TIOR0 and TIOR1.

When a general register is used as an input-compare register, its value is constantly compared with the TCNT value. When the two values match (a compare match), the corresponding flag (IMFA, IMFB, IMFC, or IMFD) in TSRW is set to 1. An interrupt request is generated at this time, when IMIEA, IMIEB, IMIEC, or IMIED is set to 1. Compare match output can be selected in TIOR.

When a general register is used as an input-capture register, an external input-capture signal is detected and the current TCNT value is stored in the general register. The corresponding flag (IMFA, IMFB, IMFC, or IMFD) in TSRW is set to 1. If the corresponding interrupt-enable bit (IMIEA, IMIEB, IMIEC, or IMIED) in TSRW is set to 1 at this time, an interrupt request is generated. The edge of the input-capture signal is selected in TIOR.

GRC and GRD can be used as buffer registers of GRA and GRB, respectively, by setting BUFEA and BUFEB in TMRW.

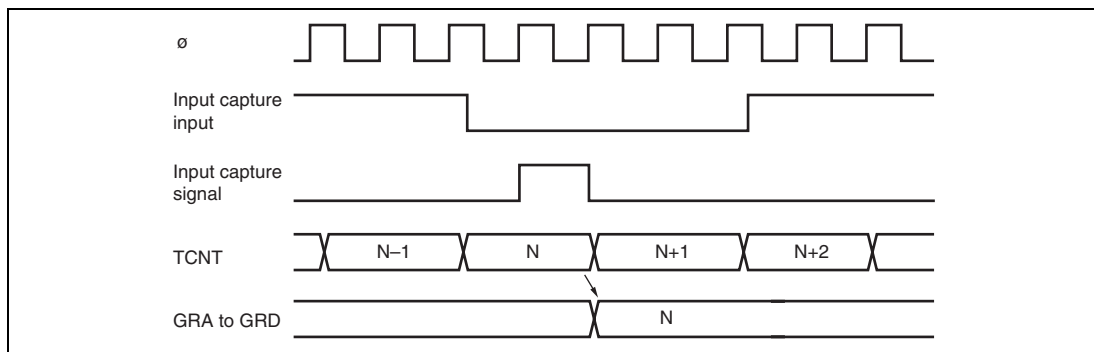
For example, when GRA is set as an output-compare register and GRC is set as the buffer register for GRA, the value in the buffer register GRC is sent to GRA whenever compare match A is generated.

When GRA is set as an input-capture register and GRC is set as the buffer register for GRA, the value in TCNT is transferred to GRA and the value in the buffer register GRC is transferred to GRA whenever an input capture is generated.

GRA to GRD must be written or read in 16-bit units; 8-bit access is not allowed. GRA to GRD are initialized to H'FFFF by a reset.

### 11.5.3 Input Capture Timing

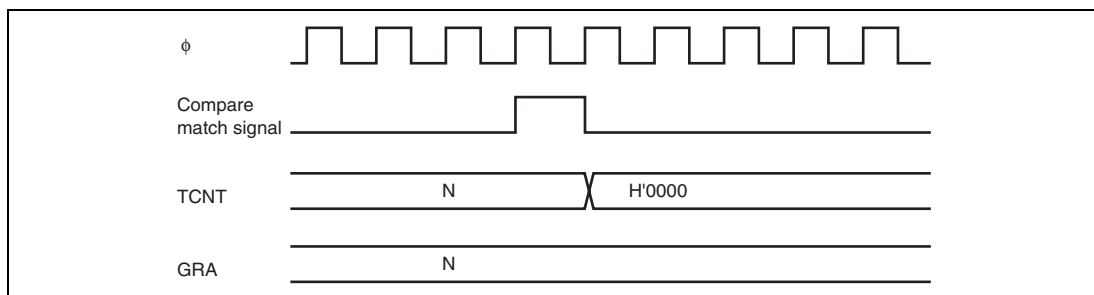
Input capture on the rising edge, falling edge, or both edges can be selected through settings in TIOR0 and TIOR1. Figure 11.17 shows the timing when the falling edge is selected. The pulse width of the input capture signal must be at least two system clock ( $\phi$ ) cycles; shorter pulses will not be detected correctly.



**Figure 11.17 Input Capture Input Signal Timing**

### 11.5.4 Timing of Counter Clearing by Compare Match

Figure 11.18 shows the timing when the counter is cleared by compare match A. When the GRA value is N, the counter counts from 0 to N, and its cycle is  $N + 1$ .



**Figure 11.18 Timing of Counter Clearing by Compare Match**

Bit	Bit Name	Initial Value	R/W	Description
3	PER	0	R/W	Parity Error [Setting condition] <ul style="list-style-type: none"> <li>When a parity error is detected during reception</li> </ul> [Clearing condition] <ul style="list-style-type: none"> <li>When 0 is written to PER after reading PER = 1</li> </ul>
2	TEND	1	R	Transmit End [Setting conditions] <ul style="list-style-type: none"> <li>When the TE bit in SCR3 is 0</li> <li>When TDRE = 1 at transmission of the last bit of a 1-frame serial transmit character</li> </ul> [Clearing conditions] <ul style="list-style-type: none"> <li>When 0 is written to TDRE after reading TDRE = 1</li> <li>When the transmit data is written to TDR</li> </ul>
1	MPBR	0	R	Multiprocessor Bit Receive MPBR stores the multiprocessor bit in the receive character data. When the RE bit in SCR3 is cleared to 0, its state is retained.
0	MPBT	0	R/W	Multiprocessor Bit Transfer MPBT stores the multiprocessor bit to be added to the transmit character data.

**Table 13.3 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode) (1)**

Bit Rate (bits/s)	Operating Frequency $\phi$ (MHz)											
	2			2.097152			2.4576			3		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	1	141	0.03	1	148	-0.04	1	174	-0.26	1	212	0.03
150	1	103	0.16	1	108	0.21	1	127	0.00	1	155	0.16
300	0	207	0.16	0	217	0.21	0	255	0.00	1	77	0.16
600	0	103	0.16	0	108	0.21	0	127	0.00	0	155	0.16
1200	0	51	0.16	0	54	-0.70	0	63	0.00	0	77	0.16
2400	0	25	0.16	0	26	1.14	0	31	0.00	0	38	0.16
4800	0	12	0.16	0	13	-2.48	0	15	0.00	0	19	-2.34
9600	0	6	-6.99	0	6	-2.48	0	7	0.00	0	9	-2.34
19200	0	2	8.51	0	2	13.78	0	3	0.00	0	4	-2.34
31250	0	1	0.00	0	1	4.86	0	1	22.88	0	2	0.00
38400	0	1	-18.62	0	1	-14.67	0	1	0.00	—	—	—

Bit Rate (bits/s)	Operating Frequency $\phi$ (MHz)											
	3.6864			4			4.9152			5		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	64	0.70	2	70	0.03	2	86	0.31	2	88	-0.25
150	1	191	0.00	1	207	0.16	1	255	0.00	2	64	0.16
300	1	95	0.00	1	103	0.16	1	127	0.00	1	129	0.16
600	0	191	0.00	0	207	0.16	0	255	0.00	1	64	0.16
1200	0	95	0.00	0	103	0.16	0	127	0.00	0	129	0.16
2400	0	47	0.00	0	51	0.16	0	63	0.00	0	64	0.16
4800	0	23	0.00	0	25	0.16	0	31	0.00	0	32	-1.36
9600	0	11	0.00	0	12	0.16	0	15	0.00	0	15	1.73
19200	0	5	0.00	0	6	-6.99	0	7	0.00	0	7	1.73
31250	—	—	—	0	3	0.00	0	4	-1.70	0	4	0.00
38400	0	2	0.00	0	2	8.51	0	3	0.00	0	3	1.73

Legend

—: A setting is available but error occurs

**Table 13.3 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode) (3)**

Bit Rate (bit/s)	Operating Frequency $\phi$ (MHz)											
	12.888			14			14.7456			16		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	217	0.08	2	248	-0.17	3	64	0.70	3	70	0.03
150	2	159	0.00	2	181	0.16	2	191	0.00	2	207	0.16
300	2	79	0.00	2	90	0.16	2	95	0.00	2	103	0.16
600	1	159	0.00	1	181	0.16	1	191	0.00	1	207	0.16
1200	1	79	0.00	1	90	0.16	1	95	0.00	1	103	0.16
2400	0	159	0.00	0	181	0.16	0	191	0.00	0	207	0.16
4800	0	79	0.00	0	90	0.16	0	95	0.00	0	103	0.16
9600	0	39	0.00	0	45	-0.93	0	47	0.00	0	51	0.16
19200	0	19	0.00	0	22	-0.93	0	23	0.00	0	25	0.16
31250	0	11	2.40	0	13	0.00	0	14	-1.70	0	15	0.00
38400	0	9	0.00	—	—	—	0	11	0.00	0	12	0.16

Bit Rate (bit/s)	Operating Frequency $\phi$ (MHz)					
	18			20		
	n	N	Error (%)	n	N	Error (%)
110	3	79	-0.12	3	88	-0.25
150	2	233	0.16	3	64	0.16
300	2	116	0.16	2	129	0.16
600	1	233	0.16	2	64	0.16
1200	1	116	0.16	1	129	0.16
2400	0	233	0.16	1	64	0.16
4800	0	116	0.16	0	129	0.16
9600	0	58	-0.96	0	64	0.16
19200	0	28	1.02	0	32	-1.36
31250	0	17	0.00	0	19	0.00
38400	0	14	-2.34	0	15	1.73

Legend

—: A setting is available but error occurs.

## Section 14 A/D Converter

This LSI includes a successive approximation type 10-bit A/D converter that allows up to four analog input channels to be selected. The block diagram of the A/D converter is shown in figure 14.1.

### 14.1 Features

- 10-bit resolution
- Four input channels
- Conversion time: at least 3.5  $\mu$ s per channel (at 20 MHz operation)
- Two operating modes
  - Single mode: Single-channel A/D conversion
  - Scan mode: Continuous A/D conversion on 1 to 4 channels
- Four data registers
  - Conversion results are held in a 16-bit data register for each channel
- Sample and hold function
- Two conversion start methods
  - Software
  - External trigger signal
- Interrupt request
  - An A/D conversion end interrupt request (ADI) can be generated

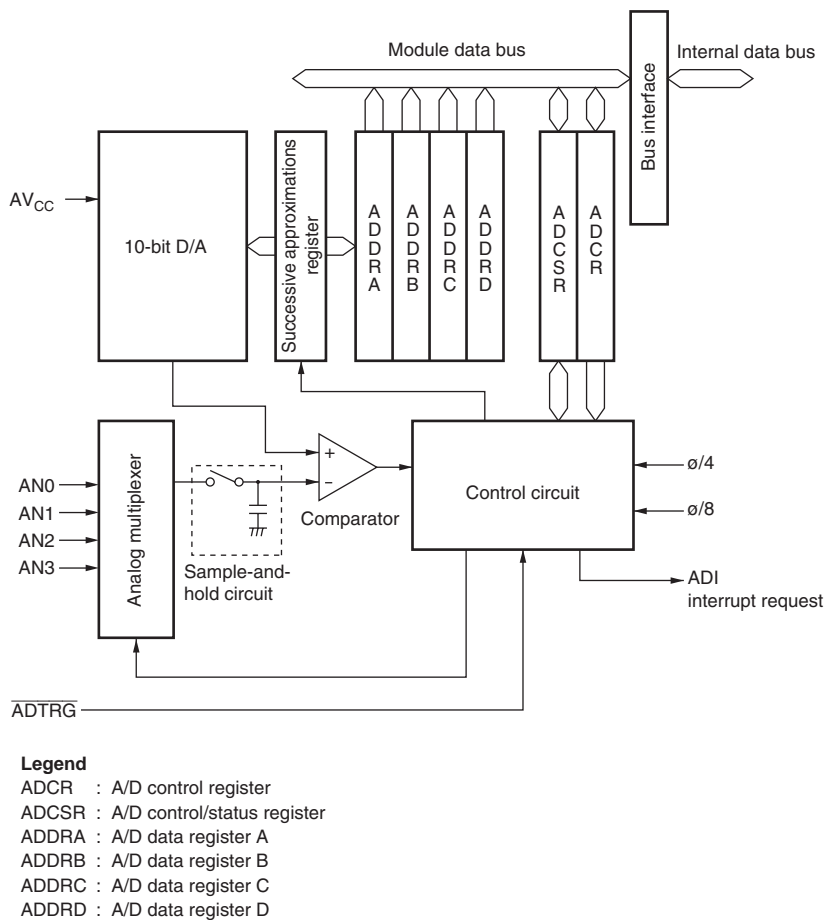
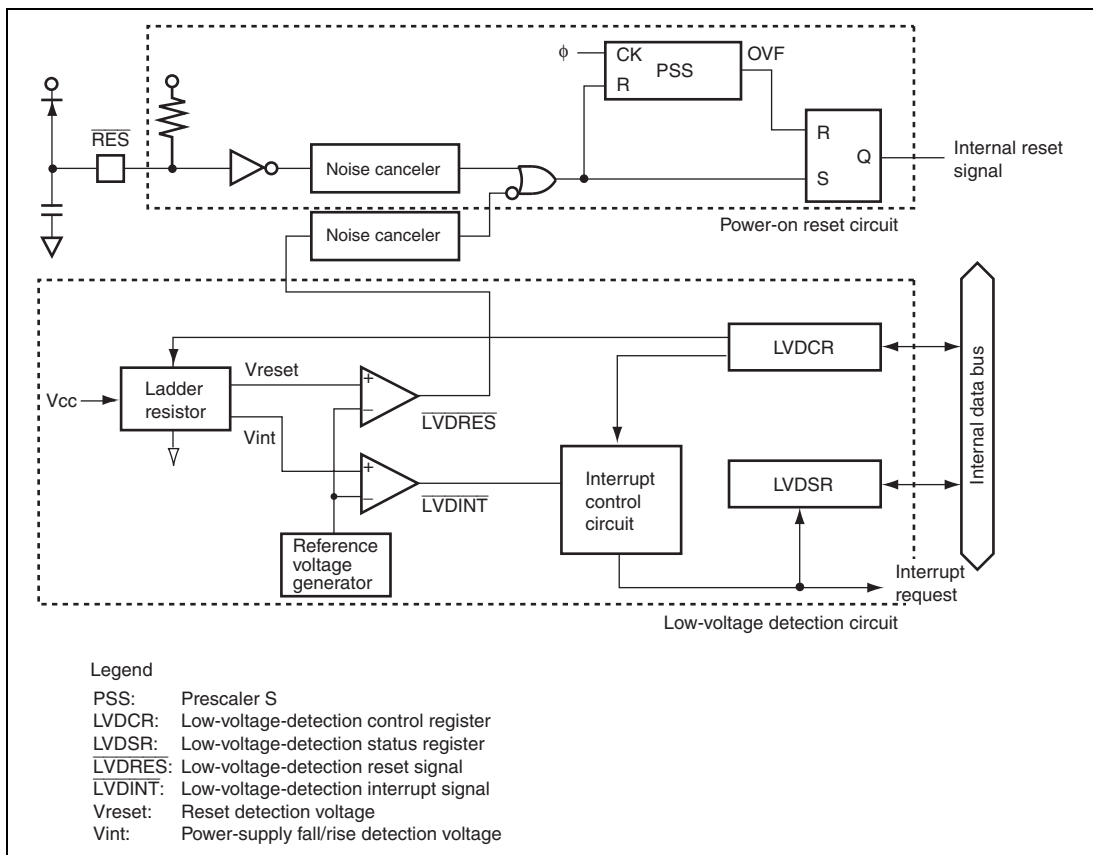


Figure 14.1 Block Diagram of A/D Converter



**Figure 15.1 Block Diagram of Power-On Reset Circuit and Low-Voltage Detection Circuit**

## 15.2 Register Descriptions

The low-voltage detection circuit has the following registers.

- Low-voltage-detection control register (LVDCR)
- Low-voltage-detection status register (LVDSR)

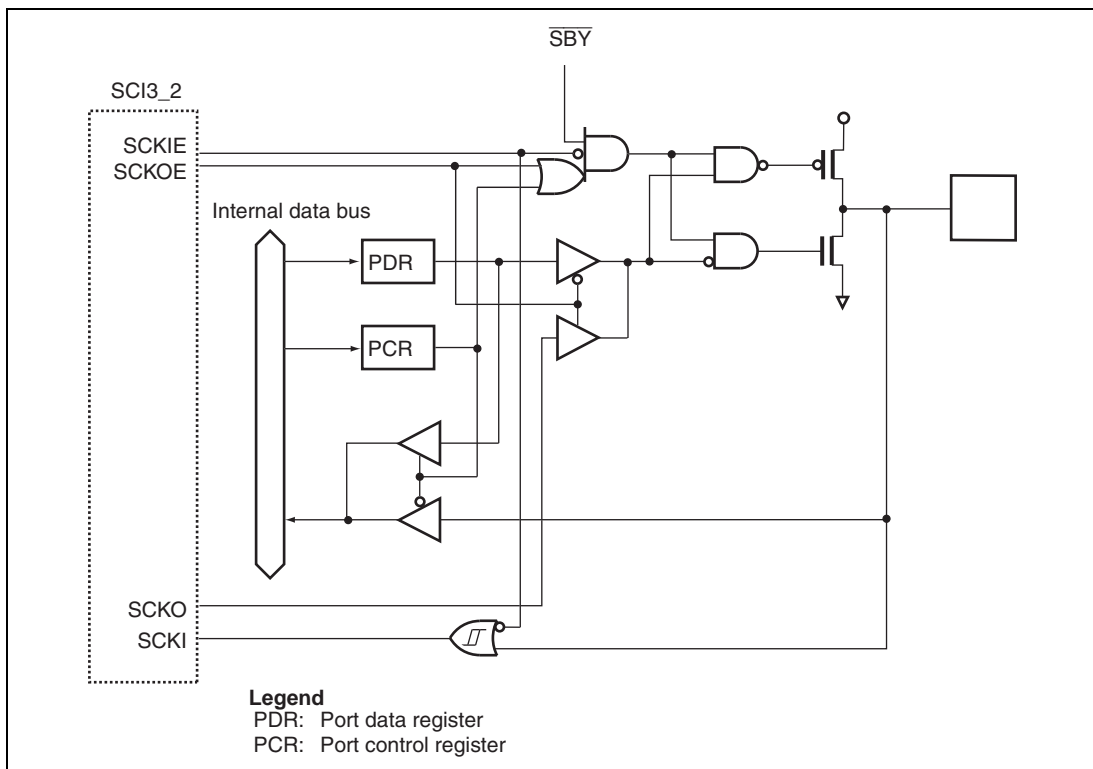


Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Notes
				Min	Typ	Max		
RAM data retaining voltage	$V_{\text{RAM}}$	$V_{\text{CC}}$		2.0	—	—	V	

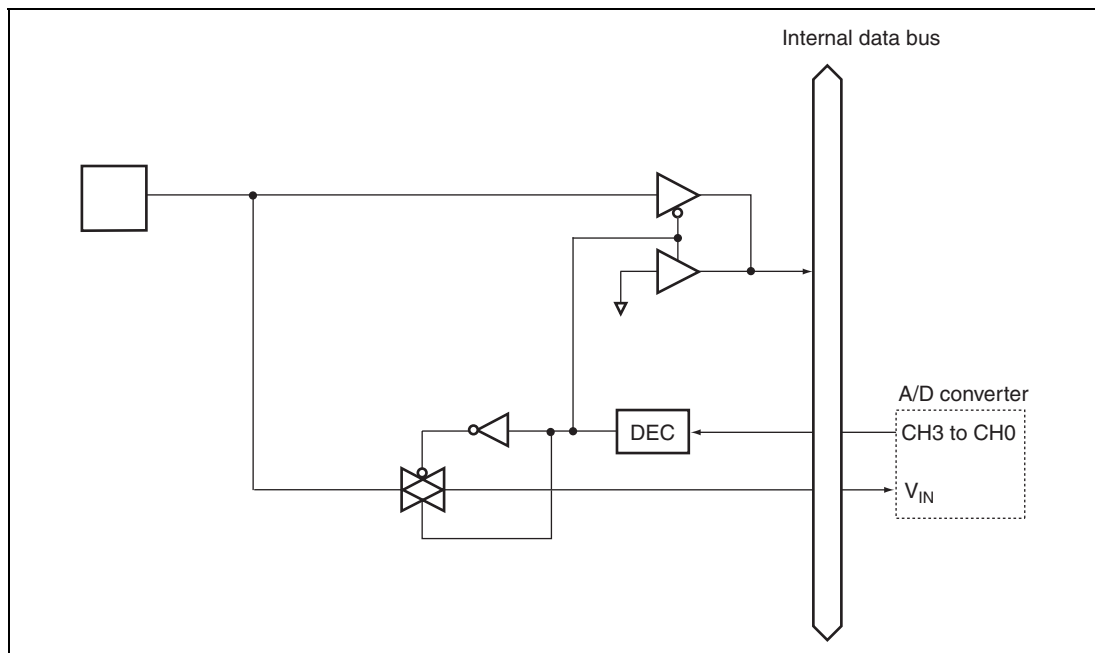
- Notes: 1. The SCK3\_3 and RXD\_3 pins are not available in the H8/36014.  
 2. Pin states during current consumption measurement are given below (excluding current in the pull-up MOS transistors and output buffers).

Mode	$\overline{\text{RES}}$ Pin	Internal State	Other Pins	Oscillator Pins
Active mode 1	$V_{\text{CC}}$	Operates	$V_{\text{CC}}$	Main clock: ceramic or crystal resonator
Active mode 2		Operates ( $\phi\text{OSC}/64$ )		
Sleep mode 1	$V_{\text{CC}}$	Only timers operate	$V_{\text{CC}}$	
Sleep mode 2		Only timers operate ( $\phi\text{OSC}/64$ )		
Standby mode	$V_{\text{CC}}$	CPU and timers both stop	$V_{\text{CC}}$	Main clock: ceramic or crystal resonator





**Figure B.20 Port 7 Block Diagram (P70)**



**Figure B.23 Port B Block Diagram (PB3 to PB0)**

## B.2 Port States in Each Operating State

Port	Reset	Active	Sleep	Subsleep	Standby
P17 to P14, P12 to P10	High impedance	Functioning	Retained	Retained	High impedance*
P22 to P20	High impedance	Functioning	Retained	Retained	High impedance
P57 to P50	High impedance	Functioning	Retained	Retained	High impedance*
P76 to P70	High impedance	Functioning	Retained	Retained	High impedance
P84 to P80	High impedance	Functioning	Retained	Retained	High impedance
PB3 to PB0	High impedance	High impedance	High impedance	Retained	High impedance

Note: \* High level output when the pull-up MOS is in on state.

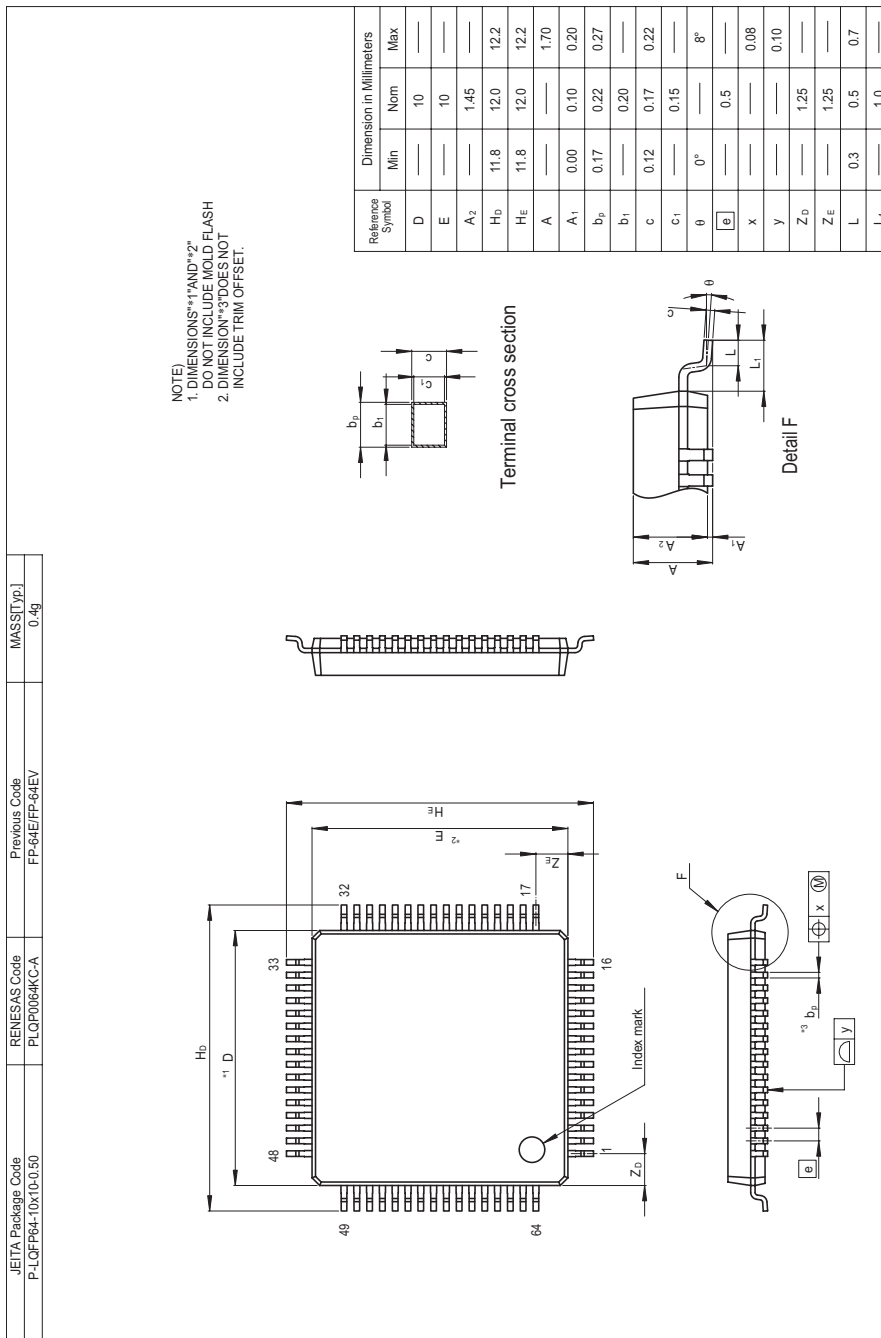


Figure D.1 FP-64E Package Dimensions