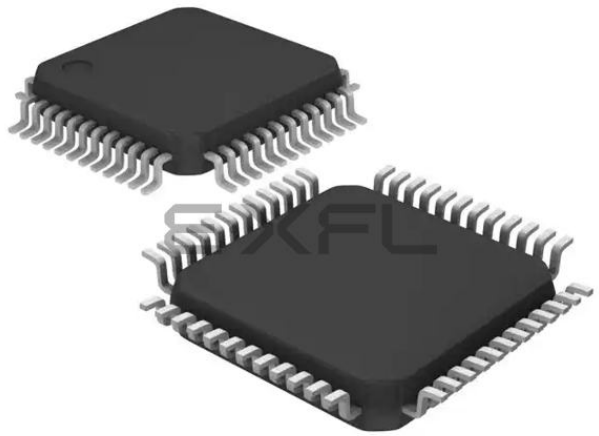

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | H8/300H |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | SCI |
| Peripherals | PWM, WDT |
| Number of I/O | 30 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 4x10b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 75°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/df36022fxv |

### (1) Register Direct—Rn

The register field of the instruction specifies an 8-, 16-, or 32-bit general register containing the operand. R0H to R7H and R0L to R7L can be specified as 8-bit registers. R0 to R7 and E0 to E7 can be specified as 16-bit registers. ER0 to ER7 can be specified as 32-bit registers.

### (2) Register Indirect—@ERn

The register field of the instruction code specifies an address register (ERn), the lower 24 bits of which contain the address of the operand on memory.

### (3) Register Indirect with Displacement—@(d:16, ERn) or @(d:24, ERn)

A 16-bit or 24-bit displacement contained in the instruction is added to an address register (ERn) specified by the register field of the instruction, and the lower 24 bits of the sum the address of a memory operand. A 16-bit displacement is sign-extended when added.

### (4) Register Indirect with Post-Increment or Pre-Decrement—@ERn+ or @-ERn

- Register indirect with post-increment—@ERn+

  The register field of the instruction code specifies an address register (ERn) the lower 24 bits of which contains the address of a memory operand. After the operand is accessed, 1, 2, or 4 is added to the address register contents (32 bits) and the sum is stored in the address register. The value added is 1 for byte access, 2 for word access, or 4 for longword access. For the word or longword access, the register value should be even.
- Register indirect with pre-decrement—@-ERn

  The value 1, 2, or 4 is subtracted from an address register (ERn) specified by the register field in the instruction code, and the lower 24 bits of the result is the address of a memory operand. The result is also stored in the address register. The value subtracted is 1 for byte access, 2 for word access, or 4 for longword access. For the word or longword access, the register value should be even.

### (5) Absolute Address—@aa:8, @aa:16, @aa:24

The instruction code contains the absolute address of a memory operand. The absolute address may be 8 bits long (@aa:8), 16 bits long (@aa:16), 24 bits long (@aa:24)

For an 8-bit absolute address, the upper 16 bits are all assumed to be 1 (H'FFFF). For a 16-bit absolute address the upper 8 bits are a sign extension. A 24-bit absolute address can access the entire address space.

### 7.2.3 Erase Block Register 1 (EBR1)

EBR1 specifies the flash memory erase area block. EBR1 is initialized to H'00 when the SWE bit in FLMCR1 is 0. Do not set more than one bit at a time, as this will cause all the bits in EBR1 to be automatically cleared to 0.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 to 5 | — | All 0 | — | Reserved<br>These bits are always read as 0. |
| 4 | EB4 | 0 | R/W | When this bit is set to 1, 28 kbytes of H'1000 to H'7FFF will be erased. |
| 3 | EB3 | 0 | R/W | When this bit is set to 1, 1 kbyte of H'0C00 to H'0FFF will be erased. |
| 2 | EB2 | 0 | R/W | When this bit is set to 1, 1 kbyte of H'0800 to H'0BFF will be erased. |
| 1 | EB1 | 0 | R/W | When this bit is set to 1, 1 kbyte of H'0400 to H'07FF will be erased. |
| 0 | EB0 | 0 | R/W | When this bit is set to 1, 1 kbyte of H'0000 to H'03FF will be erased. |

### 7.2.4 Flash Memory Enable Register (FENR)

Bit 7 (FLSHE) in FENR enables or disables the CPU access to the flash memory control registers, FLMCR1, FLMCR2, and EBR1.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | FLSHE | 0 | R/W | Flash Memory Control Register Enable<br>Flash memory control registers can be accessed when this bit is set to 1. Flash memory control registers cannot be accessed when this bit is set to 0. |
| 6 to 0 | — | All 0 | — | Reserved<br>These bits are always read as 0. |

4. After matching the bit rates, the chip transmits one H'00 byte to the host to indicate the completion of bit rate adjustment. The host should confirm that this adjustment end indication (H'00) has been received normally, and transmit one H'55 byte to the chip. If reception could not be performed normally, initiate boot mode again by a reset. Depending on the host's transfer bit rate and system clock frequency of this LSI, there will be a discrepancy between the bit rates of the host and the chip. To operate the SCI properly, set the host's transfer bit rate and system clock frequency of this LSI within the ranges listed in table 7.3.
5. In boot mode, a part of the on-chip RAM area is used by the boot program. The area H'F780 to H'FEEF is the area to which the programming control program is transferred from the host. The boot program area cannot be used until the execution state in boot mode switches to the programming control program.
6. Before branching to the programming control program, the chip terminates transfer operations by SCI3 (by clearing the RE and TE bits in SCR3 to 0), however the adjusted bit rate value remains set in BRR. Therefore, the programming control program can still use it for transfer of write data or verify data with the host. The TxD pin is high (PCR22 = 1, P22 = 1). The contents of the CPU general registers are undefined immediately after branching to the programming control program. These registers must be initialized at the beginning of the programming control program, as the stack pointer (SP), in particular, is used implicitly in subroutine calls, etc.
7. Boot mode can be cleared by a reset. End the reset after driving the reset pin low, waiting at least 20 states, and then setting the $\overline{\text{NMI}}$ pin. Boot mode is also cleared when a WDT overflow occurs.
8. Do not change the TEST pin and $\overline{\text{NMI}}$ pin input levels in boot mode.

### 9.3.5 Pin Functions

The correspondence between the register specification and the port functions is shown below.

- P57/TXD_3* pin

| Register | SMCR* | PCR5 | |
|---|---|---|---|
| **Bit Name** | **TXD_3** | **PCR57** | **Pin Function** |
| Setting Value | 0 | 0 | P57 input pin |
| | | 1 | P57 output pin |
| | 1 | X | TXD_3 output pin* |

Legend X: Don't care.
Note: * Not available in the H8/36014.

- P56/RXD_3* pin

| Register | SCR3_3* | PCR5 | |
|---|---|---|---|
| **Bit Name** | **RE** | **PCR56** | **Pin Function** |
| Setting Value | 0 | 0 | P56 input pin |
| | | 1 | P56 output pin |
| | 1 | X | RXD_3 input pin* |

Legend X: Don't care.
Note: * Not available in the H8/36014.

- P55/$\overline{\text{WKP5}}$/$\overline{\text{ADTRG}}$ pin

| Register | PMR5 | PCR5 | |
|---|---|---|---|
| **Bit Name** | **WKP5** | **PCR55** | **Pin Function** |
| Setting Value | 0 | 0 | P55 input pin |
| | | 1 | P55 output pin |
| | 1 | X | $\overline{\text{WKP5}}$/$\overline{\text{ADTRG}}$ input pin |

Legend X: Don't care.

- P83/FTIOC pin

| Register | TIOR1 | | | PCR8 | |
|---|---|---|---|---|---|
| **Bit Name** | **IOC2** | **IOC1** | **IOC0** | **PCR83** | **Pin Function** |
| Setting Value | 0 | 0 | 0 | 0 | P83 input/FTIOC input pin |
| | | | | 1 | P83 output/FTIOC input pin |
| | 0 | 0 | 1 | X | FTIOC output pin |
| | 0 | 1 | X | X | FTIOC output pin |
| | 1 | X | X | 0 | P83 input/FTIOC input pin |
| | | | | 1 | P83 output/FTIOC input pin |

Legend X: Don't care.

- P82/FTIOB pin

| Register | TIOR0 | | | PCR8 | |
|---|---|---|---|---|---|
| **Bit Name** | **IOB2** | **IOB1** | **IOB0** | **PCR82** | **Pin Function** |
| Setting Value | 0 | 0 | 0 | 0 | P82 input/FTIOB input pin |
| | | | | 1 | P82 output/FTIOB input pin |
| | 0 | 0 | 1 | X | FTIOB output pin |
| | 0 | 1 | X | X | FTIOB output pin |
| | 1 | X | X | 0 | P82 input/FTIOB input pin |
| | | | | 1 | P82 output/FTIOB input pin |

Legend X: Don't care.

- P81/FTIOA pin

| Register | TIOR0 | | | PCR8 | |
|---|---|---|---|---|---|
| **Bit Name** | **IOA2** | **IOA1** | **IOA0** | **PCR81** | **Pin Function** |
| Setting Value | 0 | 0 | 0 | 0 | P81 input/FTIOA input pin |
| | | | | 1 | P81 output/FTIOA input pin |
| | 0 | 0 | 1 | X | FTIOA output pin |
| | 0 | 1 | X | X | FTIOA output pin |
| | 1 | X | X | 0 | P81 input/FTIOA input pin |
| | | | | 1 | P81 output/FTIOA input pin |

Legend X: Don't care.

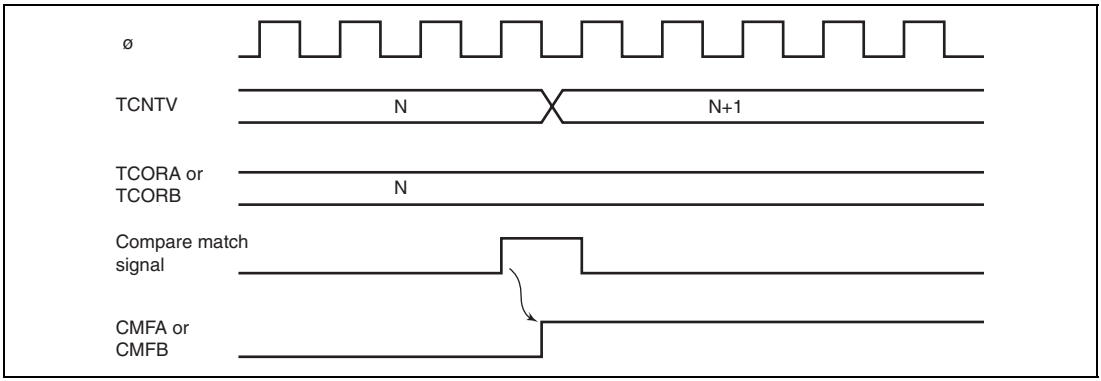



**Figure 10.5 CMFA and CMFB Set Timing**

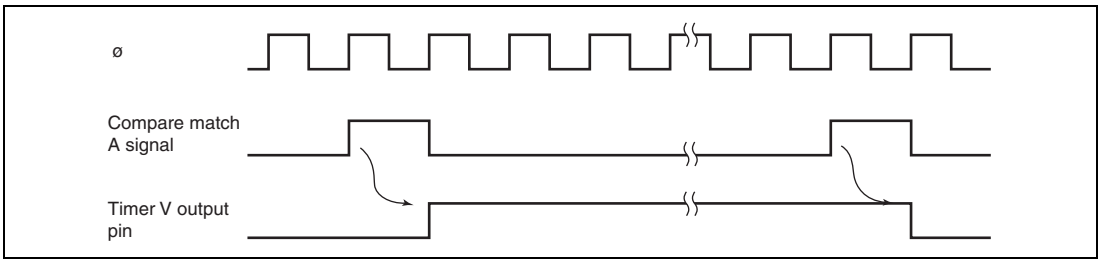



**Figure 10.6 TMOV Output Timing**

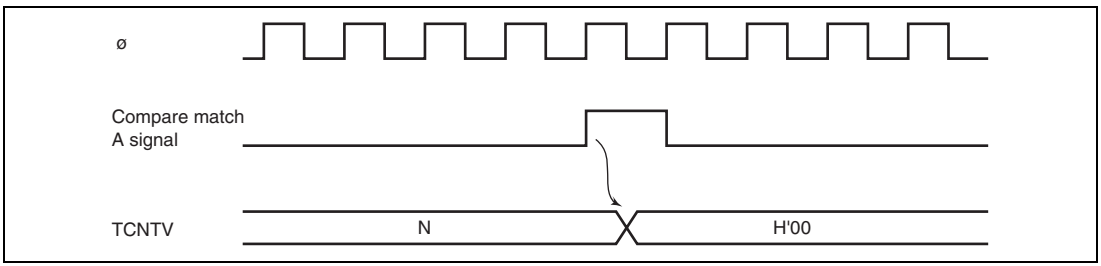



**Figure 10.7 Clear Timing by Compare Match**

## 12.3 Operation

The watchdog timer is provided with an 8-bit counter. If 1 is written to WDON while writing 0 to B2WI when the TCSRWE bit in TCSRWD is set to 1, TCWD begins counting up. (To operate the watchdog timer, two write accesses to TCSRWD are required.) When a clock pulse is input after the TCWD count value has reached H'FF, the watchdog timer overflows and an internal reset signal is generated. The internal reset signal is output for a period of 256 $\phi_{osc}$ clock cycles. TCWD is a writable counter, and when a value is set in TCWD, the count-up starts from that value. An overflow period in the range of 1 to 256 input clock cycles can therefore be set, according to the TCWD set value.

Figure 12.2 shows an example of watchdog timer operation.

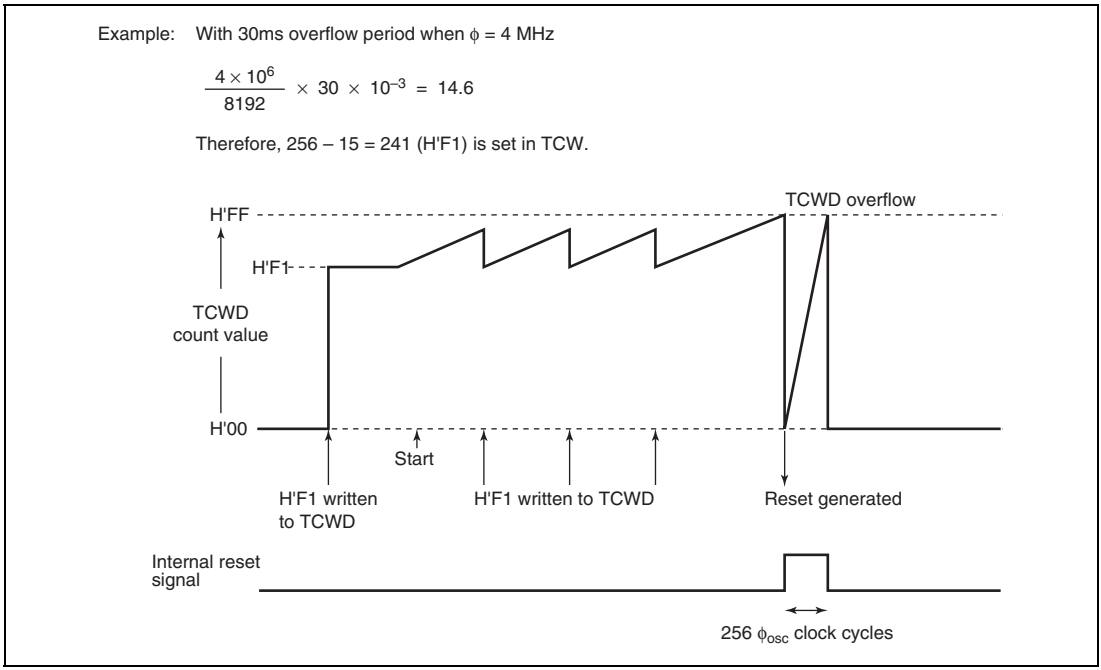



**Figure 12.2 Watchdog Timer Operation Example**

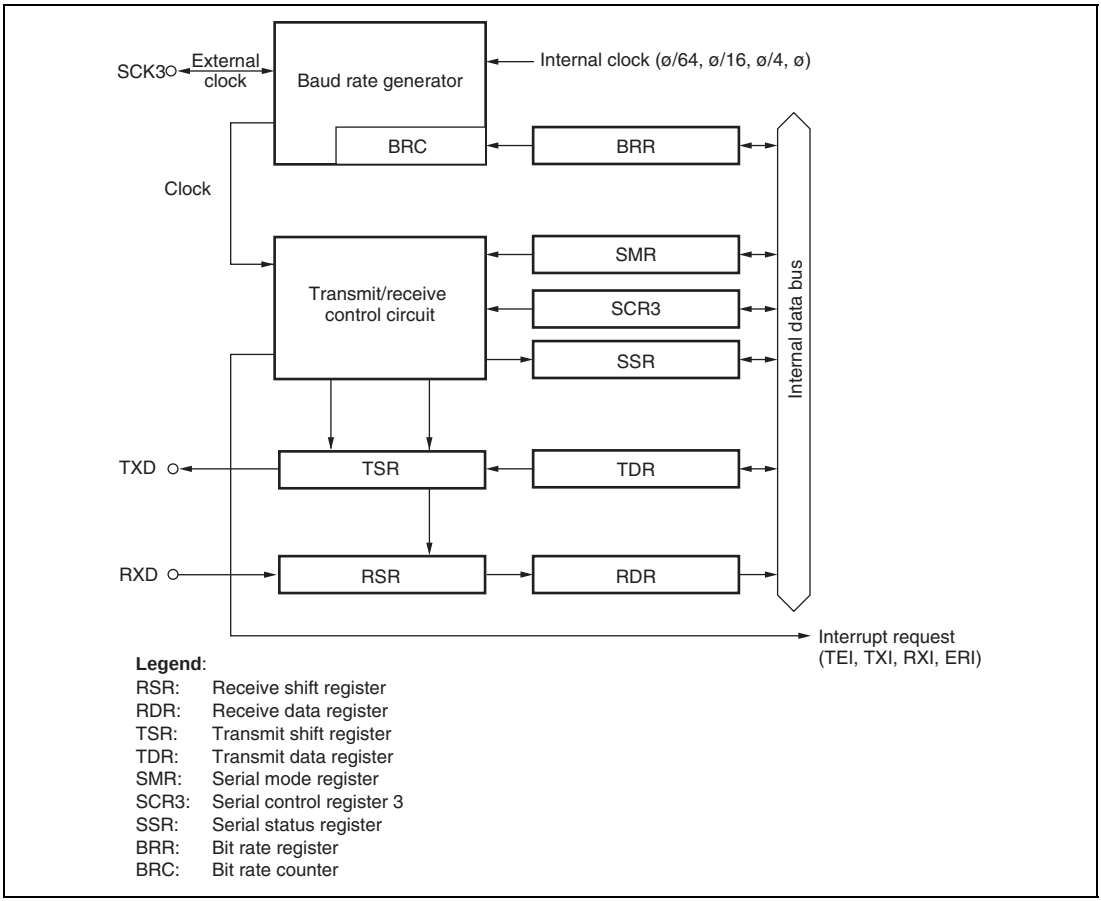
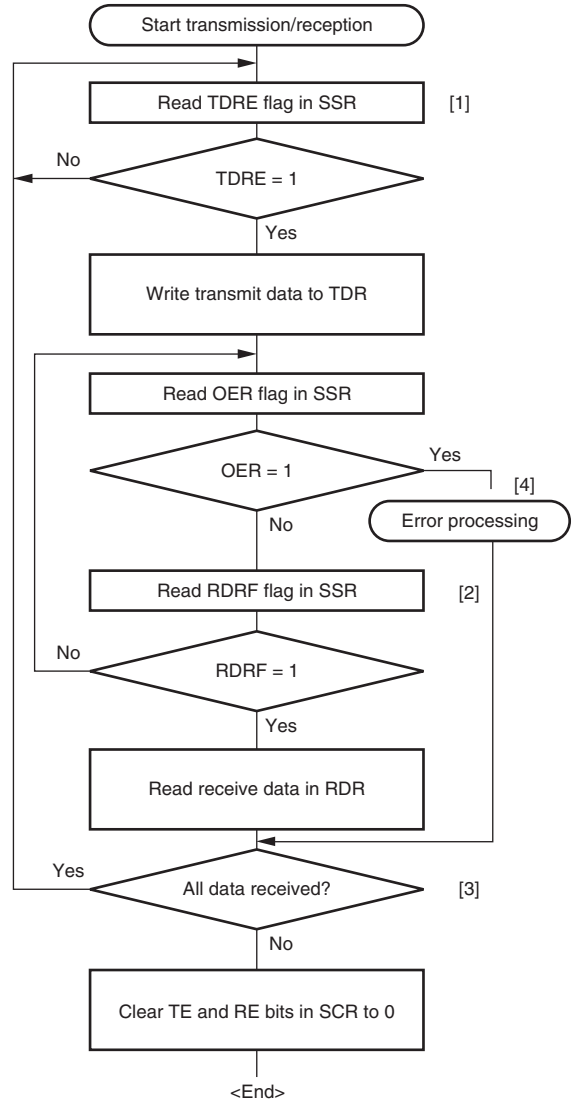



**Figure 13.1 Block Diagram of SCI3**

### 13.3.5 Serial Mode Register (SMR)

SMR is used to set the SCI3's serial transfer format and select the baud rate generator clock source.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | COM | 0 | R/W | Communication Mode<br>0: Asynchronous mode<br>1: Clocked synchronous mode |
| 6 | CHR | 0 | R/W | Character Length (enabled only in asynchronous mode)<br>0: Selects 8 bits as the data length.<br>1: Selects 7 bits as the data length. |
| 5 | PE | 0 | R/W | Parity Enable (enabled only in asynchronous mode)<br>When this bit is set to 1, the parity bit is added to transmit data before transmission, and the parity bit is checked in reception. |
| 4 | PM | 0 | R/W | Parity Mode (enabled only when the PE bit is 1 in asynchronous mode)<br>0: Selects even parity.<br>1: Selects odd parity. |
| 3 | STOP | 0 | R/W | Stop Bit Length (enabled only in asynchronous mode)<br>Selects the stop bit length in transmission.<br>0: 1 stop bit<br>1: 2 stop bits<br>For reception, only the first stop bit is checked, regardless of the value in the bit. If the second stop bit is 0, it is treated as the start bit of the next transmit character. |
| 2 | MP | 0 | R/W | Multiprocessor Mode<br>When this bit is set to 1, the multiprocessor communication function is enabled. The PE bit and PM bit settings are invalid in multiprocessor mode. In clocked synchronous mode, clear this bit to 0. |




[1] Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR.
When data is written to TDR, the TDRE flag is automatically cleared to 0.

[2] Read SSR and check that the RDRF flag is set to 1, then read the receive data in RDR.
When data is read from RDR, the RDRF flag is automatically cleared to 0.

[3] To continue serial transmission/ reception, before the MSB (bit 7) of the current frame is received, finish reading the RDRF flag, reading RDR. Also, before the MSB (bit 7) of the current frame is transmitted, read 1 from the TDRE flag to confirm that writing is possible. Then write data to TDR.
When data is written to TDR, the TDRE flag is automatically cleared to 0. When data is read from RDR, the RDRF flag is automatically cleared to 0.

[4] If an overrun error occurs, read the OER flag in SSR, and after performing the appropriate error processing, clear the OER flag to 0. Transmission/reception cannot be resumed if the OER flag is set to 1. For overrun error processing, see figure 13.13.

**Figure 13.14 Sample Flowchart of Simultaneous Serial Transmit and Receive Operations (Clocked Synchronous Mode)**

# Section 14 A/D Converter

This LSI includes a successive approximation type 10-bit A/D converter that allows up to four analog input channels to be selected. The block diagram of the A/D converter is shown in figure 14.1.

## 14.1 Features

- 10-bit resolution
- Four input channels
- Conversion time: at least 3.5 µs per channel (at 20 MHz operation)
- Two operating modes
  - — Single mode: Single-channel A/D conversion
  - — Scan mode: Continuous A/D conversion on 1 to 4 channels
- Four data registers
  - — Conversion results are held in a 16-bit data register for each channel
- Sample and hold function
- Two conversion start methods
  - — Software
  - — External trigger signal
- Interrupt request
  - — An A/D conversion end interrupt request (ADI) can be generated

## 16.2 When Not Using Internal Power Supply Step-Down Circuit

When the internal power supply step-down circuit is not used, connect the external power supply to the $V_{CL}$ pin and $V_{CC}$ pin, as shown in figure 16.2. The external power supply is then input directly to the internal power supply. The permissible range for the power supply voltage is 3.0 V to 3.6 V. Operation cannot be guaranteed if a voltage outside this range (less than 3.0 V or more than 3.6 V) is input.

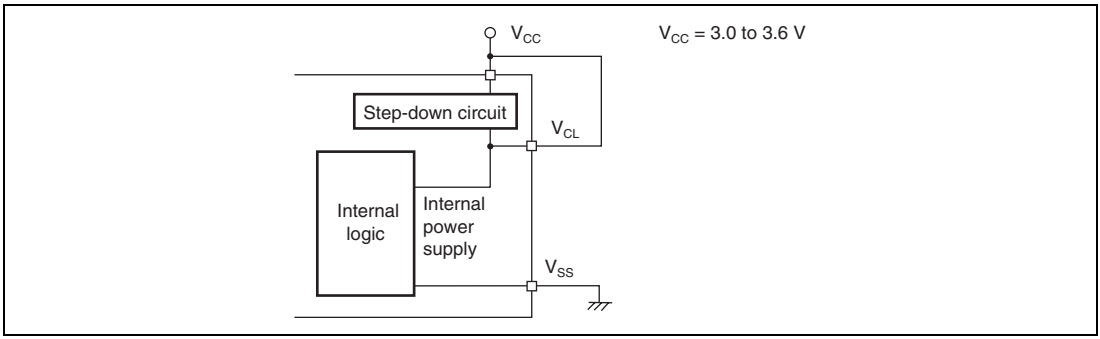



**Figure 16.2 Power Supply Connection when Internal Step-Down Circuit is Not Used**

| Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Module Name |
|---|---|---|---|---|---|---|---|---|---|
| ABRKCR | RTINTE | CSEL1 | CSEL0 | ACMP2 | ACMP1 | ACMP0 | DCMP1 | DCMP0 | Address break |
| ABRKSR | ABIF | ABIE | — | — | — | — | — | — | |
| BARH | BARH7 | BARH6 | BARH5 | BARH4 | BARH3 | BARH2 | BARH1 | BARH0 | |
| BARL | BARL7 | BARL6 | BARL5 | BARL4 | BARL3 | BARL2 | BARL1 | BARL0 | |
| BDRH | BDRH7 | BDRH6 | BDRH5 | BDRH4 | BDRH3 | BDRH2 | BDRH1 | BDRH0 | |
| BDRL | BDRL7 | BDRL6 | BDRL5 | BDRL4 | BDRL3 | BDRL2 | BDRL1 | BDRL0 | |
| PUCR1 | PUCR17 | PUCR16 | PUCR15 | PUCR14 | — | PUCR12 | PUCR11 | PUCR10 | I/O port |
| PUCR5 | — | — | PUCR55 | PUCR54 | PUCR53 | PUCR52 | PUCR51 | PUCR50 | |
| PDR1 | P17 | P16 | P15 | P14 | — | P12 | P11 | P10 | |
| PDR2 | — | — | — | — | — | P22 | P21 | P20 | |
| PDR5 | P57 | P56 | P55 | P54 | P53 | P52 | P51 | P50 | |
| PDR7 | — | P76 | P75 | P74 | P73 | P72 | P71 | P70 | |
| PDR8 | — | — | — | P84 | P83 | P82 | P81 | P80 | |
| PDRB | — | — | — | — | PB3 | PB2 | PB1 | PB0 | |
| PMR1 | IRQ3 | — | — | IRQ0 | TXD2 | — | TXD | — | |
| PMR5 | POF57 | POF56 | WKP5 | WKP4 | WKP3 | WKP2 | WKP1 | WKP0 | |
| PCR1 | PCR17 | PCR16 | PCR15 | PCR14 | — | PCR12 | PCR11 | PCR10 | |
| PCR2 | — | — | — | — | — | PCR22 | PCR21 | PCR20 | |
| PCR5 | PCR57 | PCR56 | PCR55 | PCR54 | PCR53 | PCR52 | PCR51 | PCR50 | |
| PCR7 | — | PCR76 | PCR75 | PCR74 | PCR73 | PCR72 | PCR71 | PCR70 | |
| PCR8 | — | — | — | PCR84 | PCR83 | PCR82 | PCR81 | PCR80 | |
| SYSCR1 | SSBY | STS2 | STS1 | STS0 | — | — | — | — | Power-down |
| SYSCR2 | SMSEL | — | DTON | MA2 | MA1 | MA0 | — | — | |
| IEGR1 | — | — | — | — | IEG3 | — | — | IEG0 | Interrupts |
| IEGR2 | — | — | WPEG5 | WPEG4 | WPEG3 | WPEG2 | WPEG1 | WPEG0 | |
| IENR1 | IENDT | — | IENWP | — | IEN3 | — | — | IEN0 | |
| IRR1 | IRRDT | — | — | — | IRRI3 | — | — | IRRI0 | |
| IWPR | — | — | IWPF5 | IWPF4 | IWPF3 | IWPF2 | IWPF1 | IWPF0 | |
| MSTCR1 | — | — | MSTS3 | MSTAD | MSTWD | MSTTW | MSTTV | — | Power-down |
| MSTCR2 | MSTS3_2 | — | — | — | — | — | — | — | |

Note: * WDT: Watchdog timer

### 18.2.6 Flash Memory Characteristics

**Table 18.7 Flash Memory Characteristics**

$V_{CC}$ = 3.0 V to 5.5 V, $V_{SS}$ = 0.0 V, $T_a$ = –20°C to +75°C, unless otherwise specified.

| Item | | Symbol | Test Condition | Values Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Programming time (per 128 bytes)*1*2*4 | | $t_P$ | | — | 7 | 200 | ms |
| Erase time (per block) *1*3*6 | | $t_E$ | | — | 100 | 1200 | ms |
| Reprogramming count | | $N_{WEC}$ | | 1000 | 10000 | — | Times |
| Programming | Wait time after SWE bit setting*1 | x | | 1 | — | — | µs |
| | Wait time after PSU bit setting*1 | y | | 50 | — | — | µs |
| | Wait time after P bit setting *1*4 | z1 | 1 ≤ n ≤ 6 | 28 | 30 | 32 | µs |
| | | z2 | 7 ≤ n ≤ 1000 | 198 | 200 | 202 | µs |
| | | z3 | Additional-programming | 8 | 10 | 12 | µs |
| | Wait time after P bit clear*1 | α | | 5 | — | — | µs |
| | Wait time after PSU bit clear*1 | β | | 5 | — | — | µs |
| | Wait time after PV bit setting*1 | γ | | 4 | — | — | µs |
| | Wait time after dummy write*1 | ε | | 2 | — | — | µs |
| | Wait time after PV bit clear*1 | η | | 2 | — | — | µs |
| | Wait time after SWE bit clear*1 | θ | | 100 | — | — | µs |
| | Maximum programming count*1*4*5 | N | | — | — | 1000 | Times |

| Item | Symbol | Applicable Pins | Test Condition | Values Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| Pull-up MOS current | $-I_p$ | P12 to P10, P17 to P14, P55 to P50 | $V_{CC}$ = 5.0 V, $V_{IN}$ = 0.0 V | 50.0 | — | 300.0 | µA | |
| | | | $V_{CC}$ = 3.0 V, $V_{IN}$ = 0.0 V | — | 60.0 | — | | Reference value |
| Input capacitance | $C_{in}$ | All input pins except power supply pins | f = 1 MHz, $V_{IN}$ = 0.0 V, $T_a$ = 25°C | — | — | 15.0 | pF | |
| Active mode current consumption | $I_{OPE1}$ | $V_{CC}$ | Active mode 1 $V_{CC}$ = 5.0 V, $f_{OSC}$ = 20 MHz | — | 15.0 | 30.0 | mA | *2 |
| | | | Active mode 1 $V_{CC}$ = 3.0 V, $f_{OSC}$ = 10 MHz | — | 8.0 | — | | *2 Reference value |
| | $I_{OPE2}$ | $V_{CC}$ | Active mode 2 $V_{CC}$ = 5.0 V, $f_{OSC}$ = 20 MHz | — | 1.8 | 3.0 | mA | *2 |
| | | | Active mode 2 $V_{CC}$ = 3.0 V, $f_{OSC}$ = 10 MHz | — | 1.2 | — | | *2 Reference value |
| Sleep mode current consumption | $I_{SLEEP1}$ | $V_{CC}$ | Sleep mode 1 $V_{CC}$ = 5.0 V, $f_{OSC}$ = 20 MHz | — | 11.5 | 22.5 | mA | *2 |
| | | | Sleep mode 1 $V_{CC}$ = 3.0 V, $f_{OSC}$ = 10 MHz | — | 6.5 | — | | *2 Reference value |
| | $I_{SLEEP2}$ | $V_{CC}$ | Sleep mode 2 $V_{CC}$ = 5.0 V, $f_{OSC}$ = 20 MHz | — | 1.7 | 2.7 | mA | *2 |
| | | | Sleep mode 2 $V_{CC}$ = 3.0 V, $f_{OSC}$ = 10 MHz | — | 1.1 | — | | *2 Reference value |
| Standby mode current consumption | $I_{STBY}$ | $V_{CC}$ | | — | — | 5.0 | µA | *2 |

| Mnemonic | | Operand Size | Addressing Mode and Instruction Length (bytes) | | | | | | | | | Operation | Condition Code | | | | | | No. of States*1 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | #xx | Rn | @ERn | @(d, ERn) | @–ERn/@ERn+ | @aa | @(d, PC) | @@aa | — | | I | H | N | Z | V | C | Normal | Advanced |
| MOV | MOV.W Rs, @–ERd | W | | | | | 2 | | | | | ERd32–2 → ERd32<br>Rs16 → @ERd | — | — | ↕ | ↕ | 0 | — | 6 | |
| | MOV.W Rs, @aa:16 | W | | | | | | 4 | | | | Rs16 → @aa:16 | — | — | ↕ | ↕ | 0 | — | 6 | |
| | MOV.W Rs, @aa:24 | W | | | | | | 6 | | | | Rs16 → @aa:24 | — | — | ↕ | ↕ | 0 | — | 8 | |
| | MOV.L #xx:32, Rd | L | 6 | | | | | | | | | #xx:32 → Rd32 | — | — | ↕ | ↕ | 0 | — | 6 | |
| | MOV.L ERs, ERd | L | | 2 | | | | | | | | ERs32 → ERd32 | — | — | ↕ | ↕ | 0 | — | 2 | |
| | MOV.L @ERs, ERd | L | | | 4 | | | | | | | @ERs → ERd32 | — | — | ↕ | ↕ | 0 | — | 8 | |
| | MOV.L @(d:16, ERs), ERd | L | | | | 6 | | | | | | @(d:16, ERs) → ERd32 | — | — | ↕ | ↕ | 0 | — | 10 | |
| | MOV.L @(d:24, ERs), ERd | L | | | | 10 | | | | | | @(d:24, ERs) → ERd32 | — | — | ↕ | ↕ | 0 | — | 14 | |
| | MOV.L @ERs+, ERd | L | | | | | 4 | | | | | @ERs → ERd32<br>ERs32+4 → ERs32 | — | — | ↕ | ↕ | 0 | — | 10 | |
| | MOV.L @aa:16, ERd | L | | | | | | 6 | | | | @aa:16 → ERd32 | — | — | ↕ | ↕ | 0 | — | 10 | |
| | MOV.L @aa:24, ERd | L | | | | | | 8 | | | | @aa:24 → ERd32 | — | — | ↕ | ↕ | 0 | — | 12 | |
| | MOV.L ERs, @ERd | L | | | 4 | | | | | | | ERs32 → @ERd | — | — | ↕ | ↕ | 0 | — | 8 | |
| | MOV.L ERs, @(d:16, ERd) | L | | | | 6 | | | | | | ERs32 → @(d:16, ERd) | — | — | ↕ | ↕ | 0 | — | 10 | |
| | MOV.L ERs, @(d:24, ERd) | L | | | | 10 | | | | | | ERs32 → @(d:24, ERd) | — | — | ↕ | ↕ | 0 | — | 14 | |
| | MOV.L ERs, @–ERd | L | | | | | 4 | | | | | ERd32–4 → ERd32<br>ERs32 → @ERd | — | — | ↕ | ↕ | 0 | — | 10 | |
| | MOV.L ERs, @aa:16 | L | | | | | | 6 | | | | ERs32 → @aa:16 | — | — | ↕ | ↕ | 0 | — | 10 | |
| | MOV.L ERs, @aa:24 | L | | | | | | 8 | | | | ERs32 → @aa:24 | — | — | ↕ | ↕ | 0 | — | 12 | |
| POP | POP.W Rn | W | | | | | | | | | 2 | @SP → Rn16<br>SP+2 → SP | — | — | ↕ | ↕ | 0 | — | 6 | |
| | POP.L ERn | L | | | | | | | | | 4 | @SP → ERn32<br>SP+4 → SP | — | — | ↕ | ↕ | 0 | — | 10 | |
| PUSH | PUSH.W Rn | W | | | | | | | | | 2 | SP–2 → SP<br>Rn16 → @SP | — | — | ↕ | ↕ | 0 | — | 6 | |
| | PUSH.L ERn | L | | | | | | | | | 4 | SP–4 → SP<br>ERn32 → @SP | — | — | ↕ | ↕ | 0 | — | 10 | |
| MOVFPE | MOVFPE @aa:16, Rd | B | | | | | | 4 | | | | Cannot be used in this LSI | Cannot be used in this LSI | | | | | | | |
| MOVTPE | MOVTPE Rs, @aa:16 | B | | | | | | 4 | | | | Cannot be used in this LSI | Cannot be used in this LSI | | | | | | | |

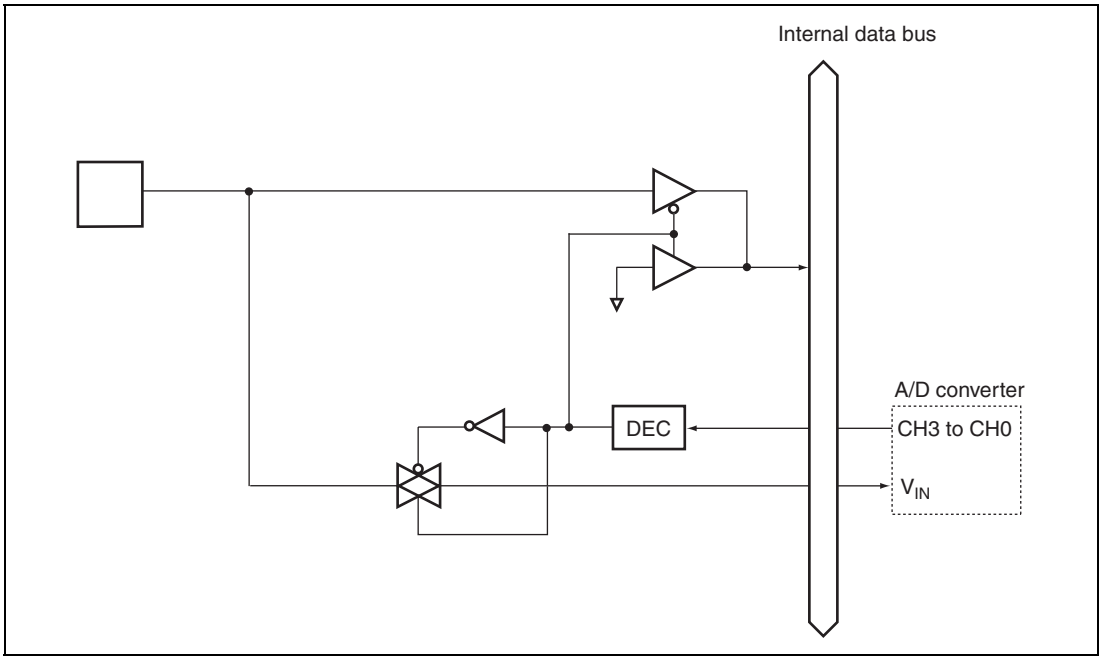



**Figure B.23 Port B Block Diagram (PB3 to PB0)**

## B.2 Port States in Each Operating State

| Port | Reset | Active | Sleep | Subsleep | Standby |
|---|---|---|---|---|---|
| P17 to P14, P12 to P10 | High impedance | Functioning | Retained | Retained | High impedance* |
| P22 to P20 | High impedance | Functioning | Retained | Retained | High impedance |
| P57 to P50 | High impedance | Functioning | Retained | Retained | High impedance* |
| P76 to P70 | High impedance | Functioning | Retained | Retained | High impedance |
| P84 to P80 | High impedance | Functioning | Retained | Retained | High impedance |
| PB3 to PB0 | High impedance | High impedance | High impedance | Retained | High impedance |

Note: * High level output when the pull-up MOS is in on state.

# H8/36024Group, H8/36014Group
# Hardware Manual

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