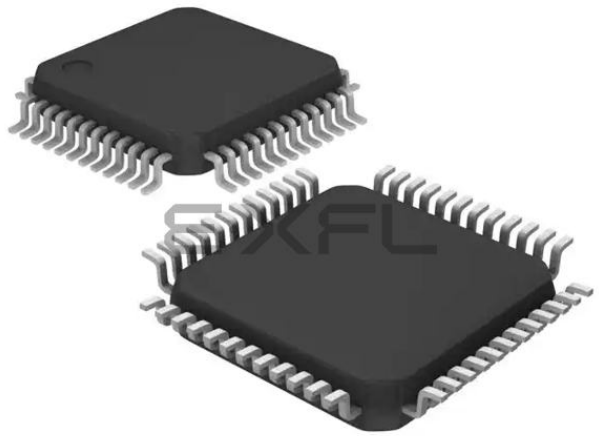

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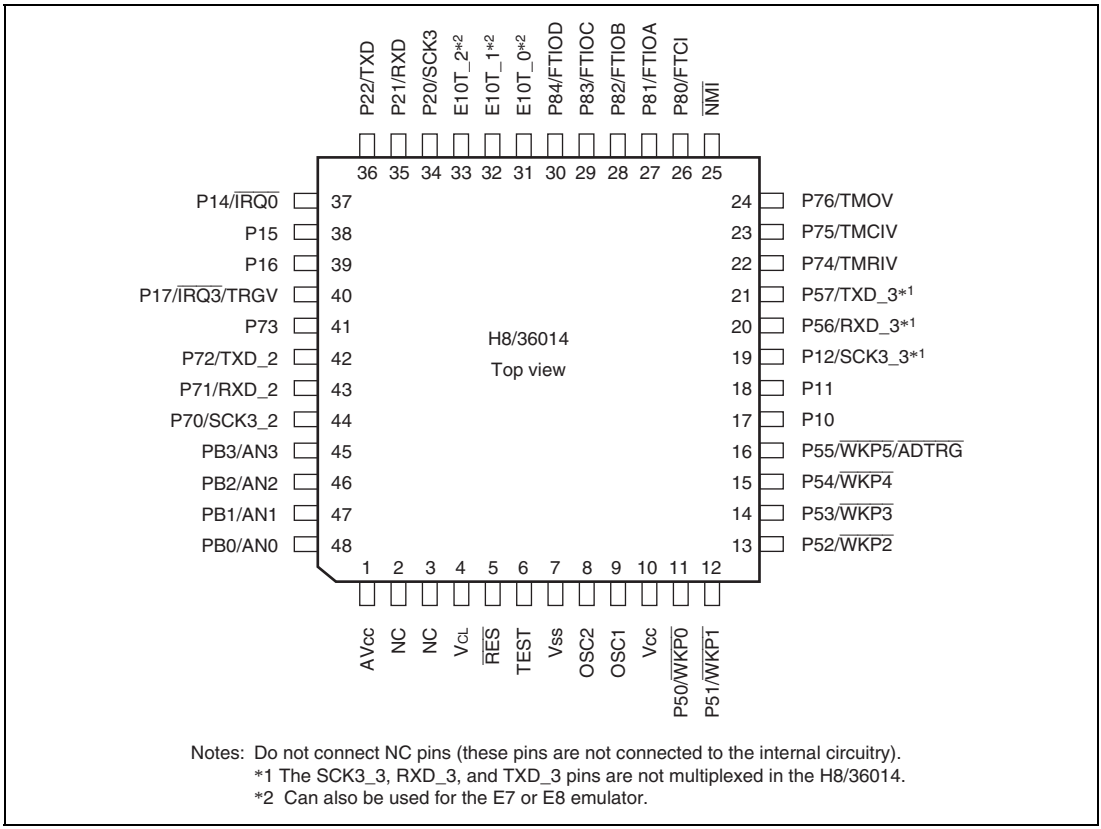
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | H8/300H |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | SCI |
| Peripherals | PWM, WDT |
| Number of I/O | 30 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 4x10b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 75°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LFQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/df36022fyv |




Notes: Do not connect NC pins (these pins are not connected to the internal circuitry).
*1 The SCK3_3, RXD_3, and TXD_3 pins are not multiplexed in the H8/36014.
*2 Can also be used for the E7 or E8 emulator.

**Figure 1.3 Pin Arrangement (FP-48F, FP-48B, TNP-48)**

### 2.3.2 Memory Data Formats

Figure 2.6 shows the data formats in memory. The H8/300H CPU can access word data and longword data in memory, however word or longword data must begin at an even address. If an attempt is made to access word or longword data at an odd address, an address error does not occur, however the least significant bit of the address is regarded as 0, so access begins the preceding address. This also applies to instruction fetches.

When ER7 (SP) is used as an address register to access the stack, the operand size should be word or longword.

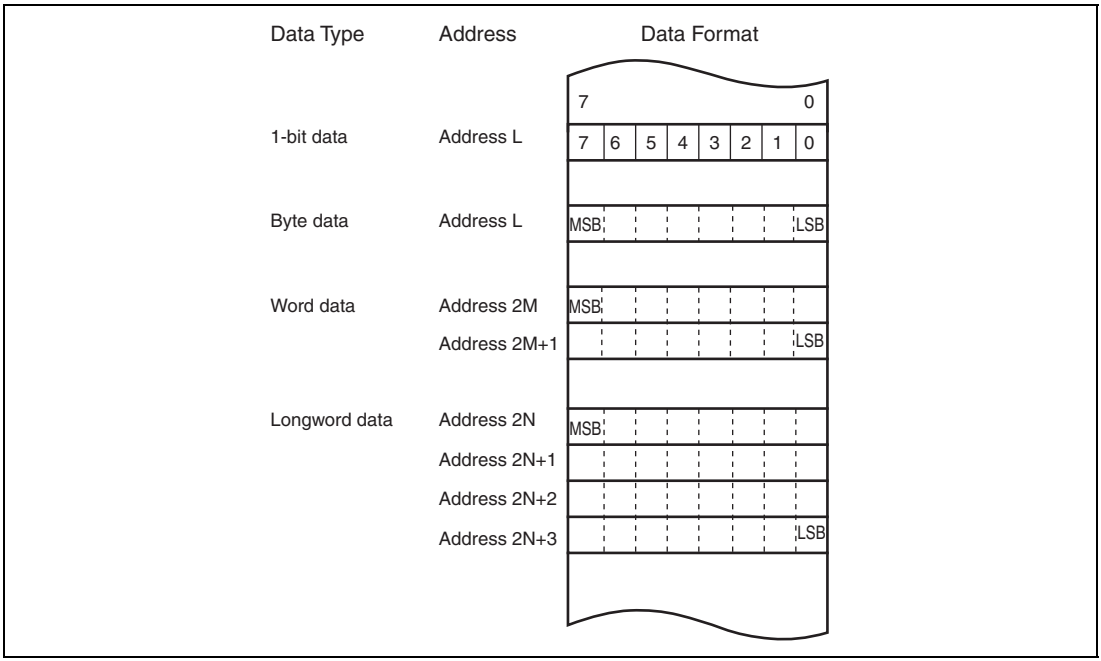



**Figure 2.6 Memory Data Formats**

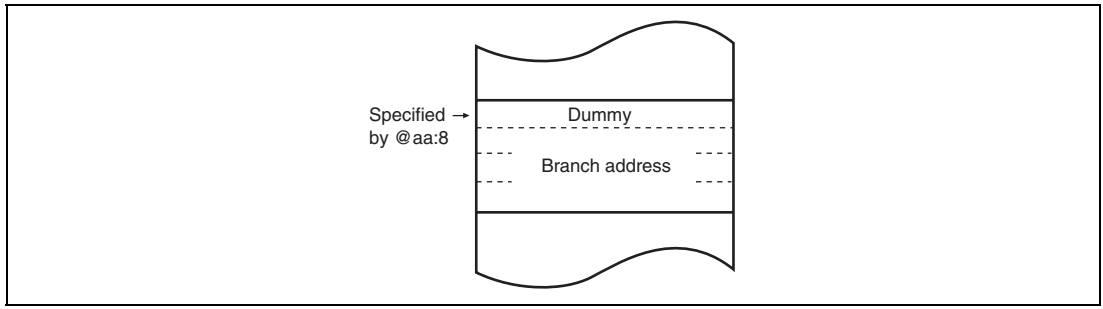



**Figure 2.8 Branch Address Specification in Memory Indirect Mode**

### 2.5.2 Effective Address Calculation

Table 2.12 indicates how effective addresses are calculated in each addressing mode. In this LSI the upper 8 bits of the effective address are ignored in order to generate a 16-bit effective address.

**Table 2.12 Effective Address Calculation (1)**

| No | Addressing Mode and Instruction Format | Effective Address Calculation | Effective Address (EA) |
|---|---|---|---|
| 1 | Register direct(Rn)<br>op \| rm \| rn | | Operand is general register contents. |
| 2 | Register indirect(@ERn)<br>op \| r | 31 … 0: General register contents | 23 … 0 |
| 3 | Register indirect with displacement<br>@(d:16,ERn) or @(d:24,ERn)<br>op \| r \| disp | 31 … 0: General register contents<br>31 … 0: Sign extension \| disp | 23 … 0 |
| 4 | Register indirect with post-increment or pre-decrement<br>•Register indirect with post-increment @ERn+<br>op \| r<br>•Register indirect with pre-decrement @-ERn<br>op \| r | 31 … 0: General register contents ± 1, 2, or 4<br>The value to be added or subtracted is 1 when the operand is byte size, 2 for word size, and 4 for longword size. | 23 … 0 |

## 2.7 CPU States

There are four CPU states: the reset state, program execution state, program halt state, and exception-handling state. The program execution state includes active mode. In the program halt state there are a sleep mode, and standby mode. These states are shown in figure 2.11. Figure 2.12 shows the state transitions. For details on program execution state and program halt state, refer to section 6, Power-Down Modes. For details on exception processing, refer to section 3, Exception Handling.

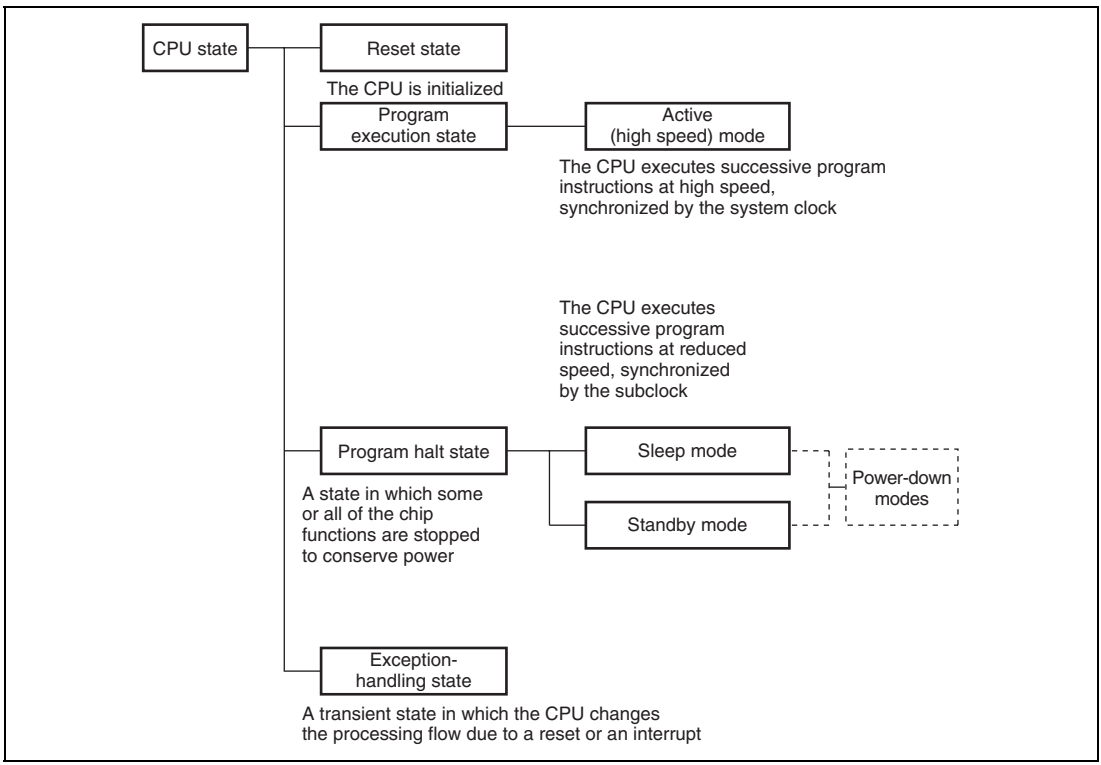



**Figure 2.11 CPU Operation States**

### 6.1.1 System Control Register 1 (SYSCR1)

SYSCR1 controls the power-down modes, as well as SYSCR2.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | SSBY | 0 | R/W | Software Standby<br>This bit selects the mode to transit after the execution of the SLEEP instruction.<br>0: a transition is made to sleep mode<br>1: a transition is made to standby mode.<br>For details, see table 6.2. |
| 6 | STS2 | 0 | R/W | Standby Timer Select 2 to 0<br>These bits designate the time the CPU and peripheral modules wait for stable clock operation after exiting from standby mode, to active mode or sleep mode due to an interrupt. The designation should be made according to the clock frequency so that the waiting time is at least 6.5 ms. The relationship between the specified value and the number of wait states is shown in table 6.1. When an external clock is to be used, the minimum value (STS2 = STS1 = STS0 =1) is recommended. |
| 5 | STS1 | 0 | R/W | |
| 4 | STS0 | 0 | R/W | |
| 3 to 0 | — | All 0 | — | Reserved<br>These bits are always read as 0. |

**Table 6.1 Operating Frequency and Waiting Time**

| Bit Name | | | | Operating Frequency | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| STS2 | STS1 | STS0 | Waiting Time | 20 MHz | 16 MHz | 10 MHz | 8 MHz | 4 MHz | 2 MHz | 1 MHz | 0.5 MHz |
| 0 | 0 | 0 | 8,192 states | 0.4 | 0.5 | 0.8 | 1.0 | 2.0 | 4.1 | 8.1 | 16.4 |
| | | 1 | 16,384 states | 0.8 | 1.0 | 1.6 | 2.0 | 4.1 | 8.2 | 16.4 | 32.8 |
| | 1 | 0 | 32,768 states | 1.6 | 2.0 | 3.3 | 4.1 | 8.2 | 16.4 | 32.8 | 65.5 |
| | | 1 | 65,536 states | 3.3 | 4.1 | 6.6 | 8.2 | 16.4 | 32.8 | 65.5 | 131.1 |
| 1 | 0 | 0 | 131,072 states | 6.6 | 8.2 | 13.1 | 16.4 | 32.8 | 65.5 | 131.1 | 262.1 |
| | | 1 | 1,024 states | 0.05 | 0.06 | 0.10 | 0.13 | 0.26 | 0.51 | 1.02 | 2.05 |
| | 1 | 0 | 128 states | 0.00 | 0.00 | 0.01 | 0.02 | 0.03 | 0.06 | 0.13 | 0.26 |
| | | 1 | 16 states | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.01 | 0.02 | 0.03 |

Note: Time unit is ms.

# Section 8 RAM

This LSI has 2 kbytes of on-chip high-speed static RAM. The RAM is connected to the CPU by a 16-bit data bus, enabling two-state access by the CPU to both byte data and word data.

| Product Classification | | RAM Size | RAM Address |
|---|---|---|---|
| Flash memory version | H8/36024F, H8/36014F | 2 kbytes | H'F780 to H'FF7F* |
| | H8/36022F, H8/36012F | 2 kbytes | H'F780 to H'FF7F* |
| Masked ROM version | H8/36024, H8/36014 | 1 kbyte | H'FB80 to H'FF7F |
| | H8/36023, H8/36013 | 1 kbyte | H'FB80 to H'FF7F |
| | H8/36022, H8/36012 | 512 bytes | H'FD80 to H'FF7F |
| | H8/36011 | 512 bytes | H'FD80 to H'FF7F |
| | H8/36010 | 512 bytes | H'FD80 to H'FF7F |

Note: * When the E7 or E8 is used, area H'F780 to H'FB7F must not be accessed.

## 9.5 Port 8

Port 8 is a general I/O port also functioning as a timer W I/O pin. Each pin of the port 8 is shown in figure 9.5. The register setting of the timer W has priority for functions of the pins P84/FTIOD, P83/FTIOC, P82/FTIOB, and P81/FTIOA. The P80/FTCI pin also functions as a timer W input port that is connected to the timer W regardless of the register setting of port 8.

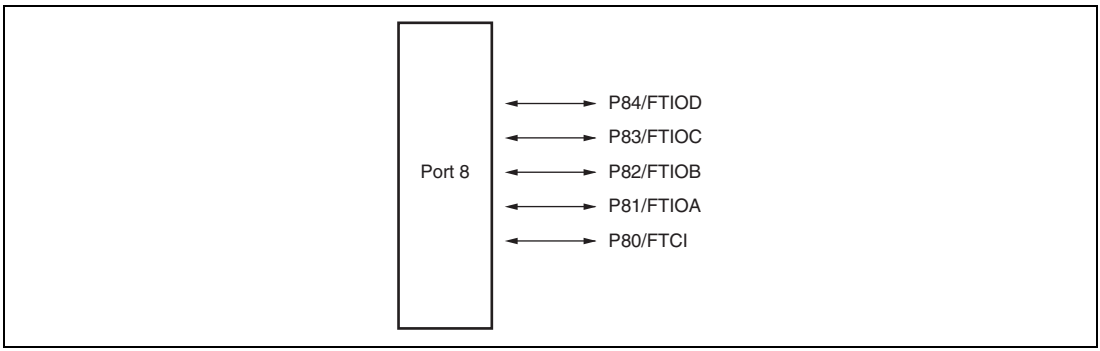



**Figure 9.5 Port 8 Pin Configuration**

Port 8 has the following registers.

- Port control register 8 (PCR8)
- Port data register 8 (PDR8)

### 9.5.1 Port Control Register 8 (PCR8)

PCR8 selects inputs/outputs in bit units for pins to be used as general I/O ports of port 8.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 to 5 | — | — | — | Reserved |
| 4 | PCR84 | 0 | W | When each of the port 8 pins P84 to P80 functions as an general I/O port, setting a PCR8 bit to 1 makes the corresponding pin an output port, while clearing the bit to 0 makes the pin an input port. |
| 3 | PCR83 | 0 | W | |
| 2 | PCR82 | 0 | W | |
| 1 | PCR81 | 0 | W | |
| 0 | PCR80 | 0 | W | |

### 10.3.5 Timer Control Register V1 (TCRV1)

TCRV1 selects the edge at the TRGV pin, enables TRGV input, and selects the clock input to TCNTV.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 to 5 | — | All 1 | — | Reserved<br>These bits are always read as 1. |
| 4 | TVEG1 | 0 | R/W | TRGV Input Edge Select |
| 3 | TVEG0 | 0 | R/W | These bits select the TRGV input edge.<br>00: TRGV trigger input is prohibited<br>01: Rising edge is selected<br>10: Falling edge is selected<br>11: Rising and falling edges are both selected |
| 2 | TRGE | 0 | R/W | TCNT starts counting up by the input of the edge which is selected by TVEG1 and TVEG0.<br>0: Disables starting counting-up TCNTV by the input of the TRGV pin and halting counting-up TCNTV when TCNTV is cleared by a compare match.<br>1: Enables starting counting-up TCNTV by the input of the TRGV pin and halting counting-up TCNTV when TCNTV is cleared by a compare match. |
| 1 | — | 1 | — | Reserved<br>This bit is always read as 1. |
| 0 | ICKS0 | 0 | R/W | Internal Clock Select 0<br>This bit selects clock signals to input to TCNTV in combination with CKS2 to CKS0 in TCRV0.<br>Refer to table 10.2. |

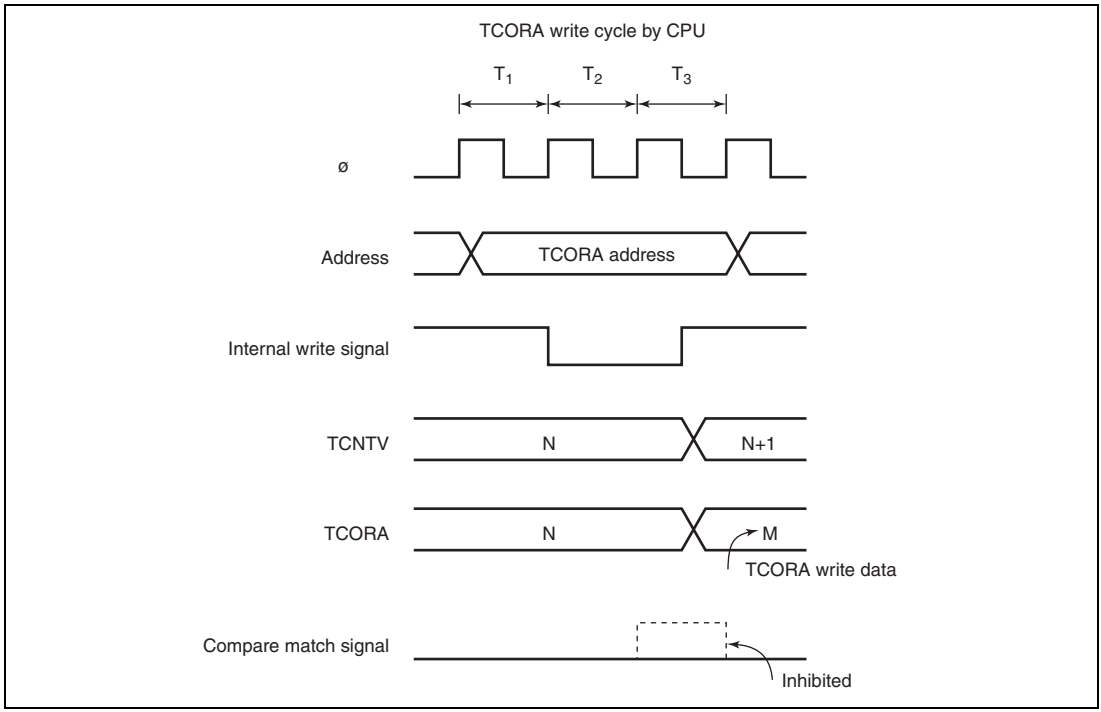



**Figure 10.12 Contention between TCORA Write and Compare Match**

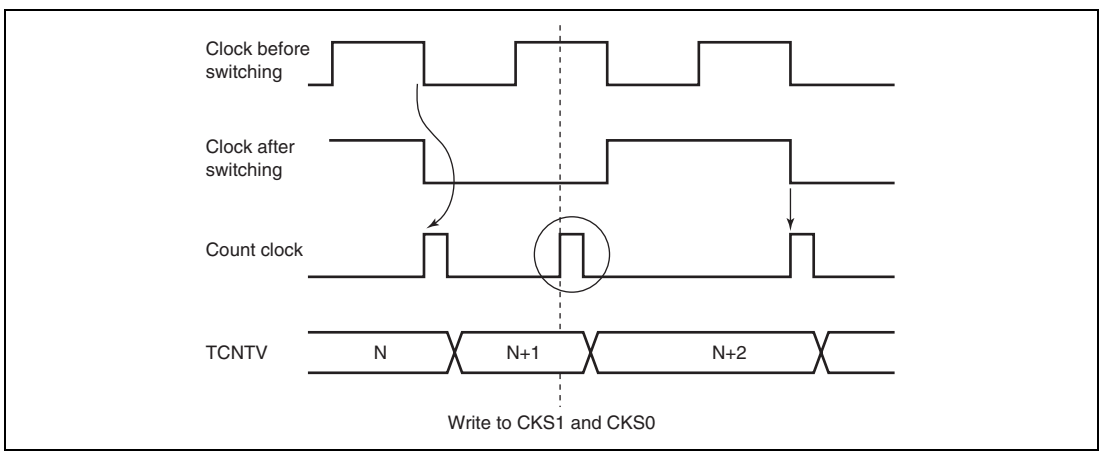



**Figure 10.13 Internal Clock Switching and TCNTV Operation**

### 11.5.3 Input Capture Timing

Input capture on the rising edge, falling edge, or both edges can be selected through settings in TIOR0 and TIOR1. Figure 11.17 shows the timing when the falling edge is selected. The pulse width of the input capture signal must be at least two system clock (ϕ) cycles; shorter pulses will not be detected correctly.

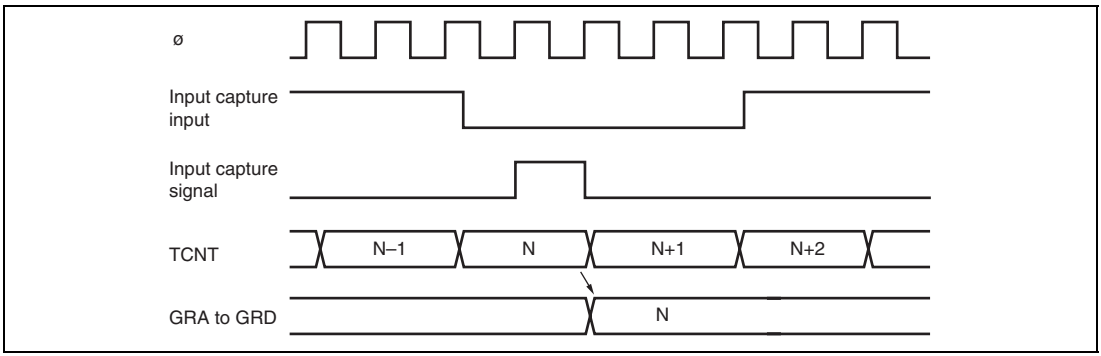



**Figure 11.17 Input Capture Input Signal Timing**

### 11.5.4 Timing of Counter Clearing by Compare Match

Figure 11.18 shows the timing when the counter is cleared by compare match A. When the GRA value is N, the counter counts from 0 to N, and its cycle is N + 1.

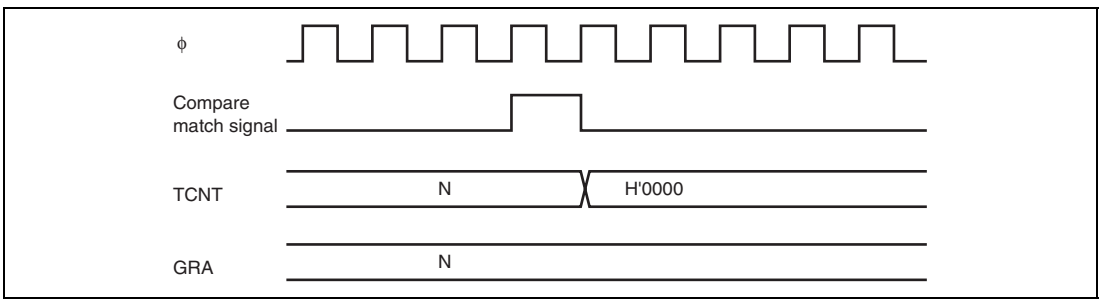



**Figure 11.18 Timing of Counter Clearing by Compare Match**

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 2 | WDON | 0 | R/W | Watchdog Timer On<br>TCWD starts counting up when WDON is set to 1 and halts when WDON is cleared to 0.<br>[Setting condition]<br>When 1 is written to the WDON bit while writing 0 to the B2WI bit when the TCSRWE bit=1<br>[Clearing condition]<br>• Reset by $\overline{RES}$ pin<br>• When 0 is written to the WDON bit while writing 0 to the B2WI when the TCSRWE bit=1 |
| 1 | B0WI | 1 | R/W | Bit 0 Write Inhibit<br>This bit can be written to the WRST bit only when the write value of the B0WI bit is 0. This bit is always read as 1. |
| 0 | WRST | 0 | R/W | Watchdog Timer Reset<br>[Setting condition]<br>When TCWD overflows and an internal reset signal is generated<br>[Clearing condition]<br>• Reset by $\overline{RES}$ pin<br>• When 0 is written to the WRST bit while writing 0 to the B0WI bit when the TCSRWE bit=1 |

### 12.2.2 Timer Counter WD (TCWD)

TCWD is an 8-bit readable/writable up-counter. When TCWD overflows from H'FF to H'00, the internal reset signal is generated and the WRST bit in TCSRWD is set to 1. TCWD is initialized to H'00.

## 13.8 Usage Notes

### 13.8.1 Break Detection and Processing

When framing error detection is performed, a break can be detected by reading the RXD pin value directly. In a break, the input from the RXD pin becomes all 0s, setting the FER flag, and possibly the PER flag. Note that as the SCI3 continues the receive operation after receiving a break, even if the FER flag is cleared to 0, it will be set to 1 again.

### 13.8.2 Mark State and Break Sending

When TE is 0, the TXD pin is used as an I/O port whose direction (input or output) and level are determined by PCR and PDR. This can be used to set the TXD pin to mark state (high level) or send a break during serial data transmission. To maintain the communication line at mark state until TE is set to 1, set both PCR and PDR to 1. As TE is cleared to 0 at this point, the TXD pin becomes an I/O port, and 1 is output from the TXD pin. To send a break during serial transmission, first set PCR to 1 and clear PDR to 0, and then clear TE to 0. When TE is cleared to 0, the transmitter is initialized regardless of the current transmission state, the TXD pin becomes an I/O port, and 0 is output from the TXD pin.

### 13.8.3 Receive Error Flags and Transmit Operations (Clocked Synchronous Mode Only)

Transmission cannot be started when a receive error flag (OER, PER, or FER) is set to 1, even if the TDRE flag is cleared to 0. Be sure to clear the receive error flags to 0 before starting transmission. Note also that receive error flags cannot be cleared to 0 even if the RE bit is cleared to 0.

| Item | | Symbol | Test Condition | Values Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Erase | Wait time after SWE bit setting*[1] | x | | 1 | — | — | µs |
| | Wait time after ESU bit setting*[1] | y | | 100 | — | — | µs |
| | Wait time after E bit setting*[1]*[6] | z | | 10 | — | 100 | ms |
| | Wait time after E bit clear*[1] | $\alpha$ | | 10 | — | — | µs |
| | Wait time after ESU bit clear*[1] | $\beta$ | | 10 | — | — | µs |
| | Wait time after EV bit setting*[1] | $\gamma$ | | 20 | — | — | µs |
| | Wait time after dummy write*[1] | $\varepsilon$ | | 2 | — | — | µs |
| | Wait time after EV bit clear*[1] | $\eta$ | | 4 | — | — | µs |
| | Wait time after SWE bit clear*[1] | $\theta$ | | 100 | — | — | µs |
| | Maximum erase count*[1]*[6]*[7] | N | | — | — | 120 | Times |

Notes:
1. Make the time settings in accordance with the program/erase algorithms.
2. The programming time for 128 bytes. (Indicates the total time for which the P bit in flash memory control register 1 (FLMCR1) is set. The program-verify time is not included.)
3. The time required to erase one block. (Indicates the time for which the E bit in flash memory control register 1 (FLMCR1) is set. The erase-verify time is not included.)
4. Programming time maximum value ($t_P$ (max.)) = wait time after P bit setting (z) × maximum programming count (N)
5. Set the maximum programming count (N) according to the actual set values of z1, z2, and z3, so that it does not exceed the programming time maximum value ($t_P$ (max.)). The wait time after P bit setting (z1, z2) should be changed as follows according to the value of the programming count (n).

   Programming count (n)

   $1 \leq n \leq 6$ z1 = 30 µs

   $7 \leq n \leq 1000$ z2 = 200 µs
6. Erase time maximum value ($t_E$ (max.)) = wait time after E bit setting (z) × maximum erase count (N)
7. Set the maximum erase count (N) according to the actual set value of (z), so that it does not exceed the erase time maximum value ($t_E$ (max.)).

### Table 18.10 DC Characteristics (2)

$V_{CC}$ = 2.7 V to 5.5 V, $V_{SS}$ = 0.0 V, $T_a$ = –20°C to +75°C, unless otherwise specified.

| Item | Symbol | Applicable Pins | Test Condition | Values Min | Values Typ | Values Max | Unit |
|---|---|---|---|---|---|---|---|
| Allowable output low current (per pin) | $I_{OL}$ | Output pins except port 8 | $V_{CC}$ = 4.0 V to 5.5 V | — | — | 2.0 | mA |
| | | Port 8 | | — | — | 20.0 | mA |
| | | Output pins except port 8 | | — | — | 0.5 | mA |
| | | Port 8 | | — | — | 10.0 | mA |
| Allowable output low current (total) | $\Sigma I_{OL}$ | Output pins except port 8 | $V_{CC}$ = 4.0 V to 5.5 V | — | — | 40.0 | mA |
| | | Port 8 | | — | — | 80.0 | mA |
| | | Output pins except port 8 | | — | — | 20.0 | mA |
| | | Port 8 | | — | — | 40.0 | mA |
| Allowable output high current (per pin) | $\lvert -I_{OH} \rvert$ | All output pins | $V_{CC}$ = 4.0 V to 5.5 V | — | — | 2.0 | mA |
| | | | | — | — | 0.2 | mA |
| Allowable output high current (total) | $\lvert -\Sigma I_{OH} \rvert$ | All output pins | $V_{CC}$ = 4.0 V to 5.5 V | — | — | 30.0 | mA |
| | | | | — | — | 8.0 | mA |

| Item | Symbol | Applicable Pins | Test Condition | Values Min | Typ | Max | Unit | Reference Figure |
|---|---|---|---|---|---|---|---|---|
| Conversion time (single mode) | | | $AV_{CC}$ = 4.0 V to 5.5 V | 134 | — | — | $t_{cyc}$ | |
| Nonlinearity error | | | | — | — | ±3.5 | LSB | |
| Offset error | | | | — | — | ±3.5 | LSB | |
| Full-scale error | | | | — | — | ±3.5 | LSB | |
| Quantization error | | | | — | — | ±0.5 | LSB | |
| Absolute accuracy | | | | — | — | ±4.0 | LSB | |

Notes: 1. Set $AV_{CC} = V_{CC}$ when the A/D converter is not used.
2. $AI_{STOP1}$ is the current in active and sleep modes while the A/D converter is idle.
3. $AI_{STOP2}$ is the current at reset and in standby and subsleep modes while the A/D converter is idle.

### 18.3.5 Watchdog Timer Characteristics

**Table 18.14 Watchdog Timer Characteristics**

$V_{CC}$ = 2.7 V to 5.5 V, $V_{SS}$ = 0.0 V, $T_a$ = –20°C to +75°C, unless otherwise specified.

| Item | Symbol | Applicable Pins | Test Condition | Values Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| On-chip oscillator overflow time | $t_{OVF}$ | | | 0.2 | 0.4 | — | s | * |

Note: * Shows the time to count from 0 to 255, at which point an internal reset is generated, when the internal oscillator is selected.

## 6. Branching instructions

| Mnemonic | | Operand Size | Addressing Mode and Instruction Length (bytes) | | | | | | | | | Operation | Condition Code | | | | | | No. of States*1 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | #xx | Rn | @ERn | @(d, ERn) | @–ERn/@ERn+ | @aa | @(d, PC) | @@aa | — | Branch Condition | I | H | N | Z | V | C | Normal | Advanced |
| Bcc | BRA d:8 (BT d:8) | — | | | | | | | 2 | | | If condition is true then PC ← PC+d else next; Always | — | — | — | — | — | — | 4 | |
| | BRA d:16 (BT d:16) | — | | | | | | | 4 | | | | — | — | — | — | — | — | 6 | |
| | BRN d:8 (BF d:8) | — | | | | | | | 2 | | | Never | — | — | — | — | — | — | 4 | |
| | BRN d:16 (BF d:16) | — | | | | | | | 4 | | | | — | — | — | — | — | — | 6 | |
| | BHI d:8 | — | | | | | | | 2 | | | C/Z = 0 | — | — | — | — | — | — | 4 | |
| | BHI d:16 | — | | | | | | | 4 | | | | — | — | — | — | — | — | 6 | |
| | BLS d:8 | — | | | | | | | 2 | | | C/Z = 1 | — | — | — | — | — | — | 4 | |
| | BLS d:16 | — | | | | | | | 4 | | | | — | — | — | — | — | — | 6 | |
| | BCC d:8 (BHS d:8) | — | | | | | | | 2 | | | C = 0 | — | — | — | — | — | — | 4 | |
| | BCC d:16 (BHS d:16) | — | | | | | | | 4 | | | | — | — | — | — | — | — | 6 | |
| | BCS d:8 (BLO d:8) | — | | | | | | | 2 | | | C = 1 | — | — | — | — | — | — | 4 | |
| | BCS d:16 (BLO d:16) | — | | | | | | | 4 | | | | — | — | — | — | — | — | 6 | |
| | BNE d:8 | — | | | | | | | 2 | | | Z = 0 | — | — | — | — | — | — | 4 | |
| | BNE d:16 | — | | | | | | | 4 | | | | — | — | — | — | — | — | 6 | |
| | BEQ d:8 | — | | | | | | | 2 | | | Z = 1 | — | — | — | — | — | — | 4 | |
| | BEQ d:16 | — | | | | | | | 4 | | | | — | — | — | — | — | — | 6 | |
| | BVC d:8 | — | | | | | | | 2 | | | V = 0 | — | — | — | — | — | — | 4 | |
| | BVC d:16 | — | | | | | | | 4 | | | | — | — | — | — | — | — | 6 | |
| | BVS d:8 | — | | | | | | | 2 | | | V = 1 | — | — | — | — | — | — | 4 | |
| | BVS d:16 | — | | | | | | | 4 | | | | — | — | — | — | — | — | 6 | |
| | BPL d:8 | — | | | | | | | 2 | | | N = 0 | — | — | — | — | — | — | 4 | |
| | BPL d:16 | — | | | | | | | 4 | | | | — | — | — | — | — | — | 6 | |
| | BMI d:8 | — | | | | | | | 2 | | | N = 1 | — | — | — | — | — | — | 4 | |
| | BMI d:16 | — | | | | | | | 4 | | | | — | — | — | — | — | — | 6 | |
| | BGE d:8 | — | | | | | | | 2 | | | N⊕V = 0 | — | — | — | — | — | — | 4 | |
| | BGE d:16 | — | | | | | | | 4 | | | | — | — | — | — | — | — | 6 | |
| | BLT d:8 | — | | | | | | | 2 | | | N⊕V = 1 | — | — | — | — | — | — | 4 | |
| | BLT d:16 | — | | | | | | | 4 | | | | — | — | — | — | — | — | 6 | |
| | BGT d:8 | — | | | | | | | 2 | | | Z/(N⊕V) = 0 | — | — | — | — | — | — | 4 | |
| | BGT d:16 | — | | | | | | | 4 | | | | — | — | — | — | — | — | 6 | |
| | BLE d:8 | — | | | | | | | 2 | | | Z/(N⊕V) = 1 | — | — | — | — | — | — | 4 | |
| | BLE d:16 | — | | | | | | | 4 | | | | — | — | — | — | — | — | 6 | |

**Table A.3 Number of Cycles in Each Instruction**

| Execution Status (Instruction Cycle) | | Access Location | |
|---|---|---|---|
| | | On-Chip Memory | On-Chip Peripheral Module |
| Instruction fetch | $S_I$ | 2 | — |
| Branch address read | $S_J$ | | |
| Stack operation | $S_K$ | | |
| Byte data access | $S_L$ | | 2 or 3* |
| Word data access | $S_M$ | | 2 or 3* |
| Internal operation | $S_N$ | 1 | |

Note: * Depends on which on-chip peripheral module is accessed. See section 17.1, Register Addresses (Address Order).

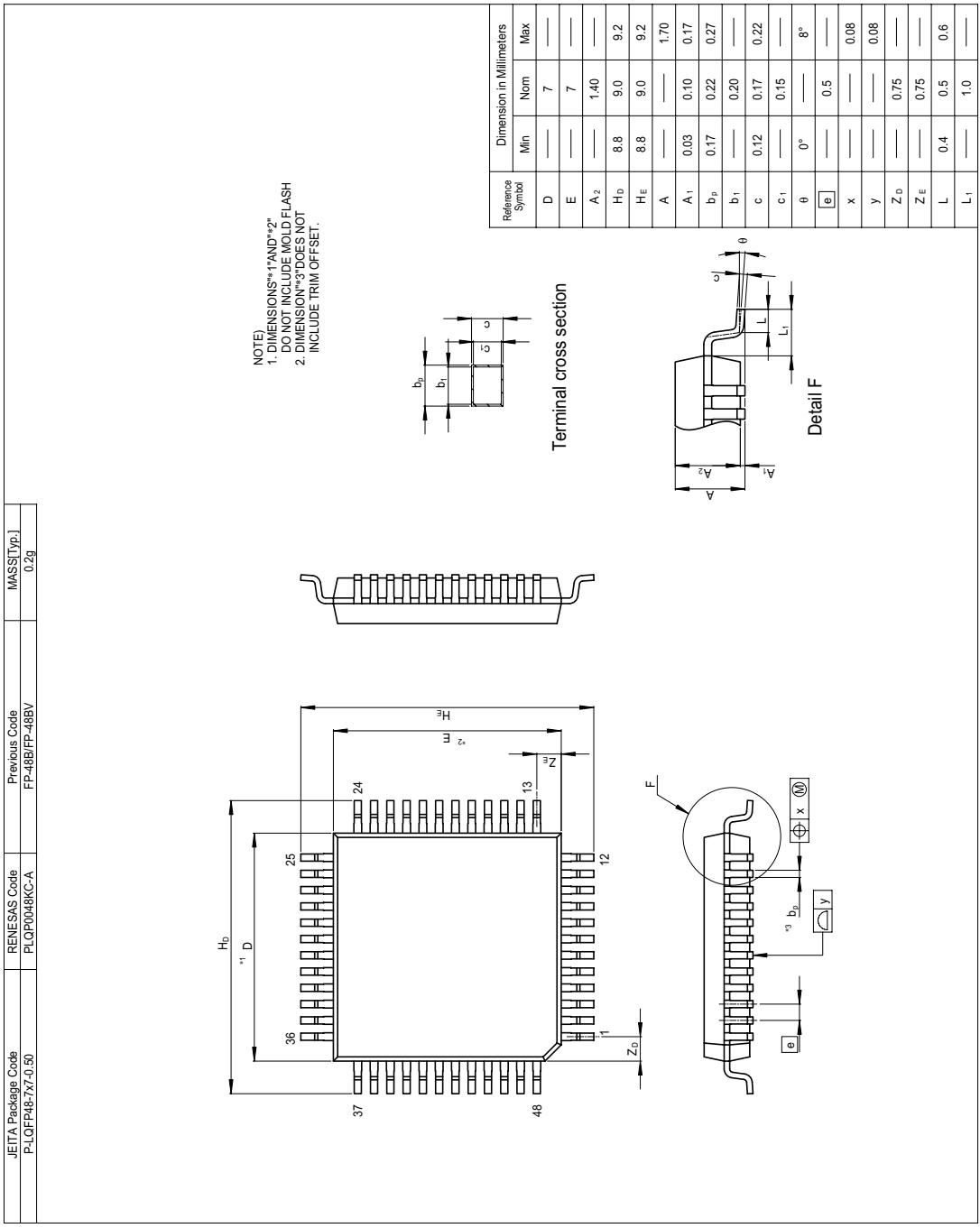



**Figure D.3 FP-48B Package Dimensions**

| Item | Page | Revision (See Manual for Details) |
|---|---|---|
| Table 18.10 DC Characteristics (1) | 270 | |

| Item | Symbol | Applicable Pins | Test Condition | Values Min |
|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | PB3 to PB0 | $V_{CC}$ = 4.0 V to 5.5 V | $V_{CC}$ × 0.7 |
| | | | | $V_{CC}$ × 0.8 |
| Input low voltage | $V_{IL}$ | RXD, RXD_2, RXD_3*[1], P12 to P10, P17 to P14, : PB3 to PB0 | $V_{CC}$ = 4.0 V to 5.5 V | –0.3 |

| Table 18.10 DC Characteristics (1) | 273 | |
|---|---|---|

| Mode | $\overline{RES}$ Pin | Internal State |
|---|---|---|
| Active mode 1 | $V_{CC}$ | Operates |
| Active mode 2 | | Operates (φOSC/64) |
| Sleep mode 1 | $V_{CC}$ | Only timers operate |
| Sleep mode 2 | | Only timers operate (φOSC/64) |

| | | |
|---|---|---|
| Appendix D Package Dimensions<br>Figure D.1 FP-64E Package Dimensions | 343 | Swapped with new one. |
| Figure D.2 FP-48F Package Dimensions | 344 | Swapped with new one. |
| Figure D.3 FP-48B Package Dimensions | 345 | Swapped with new one. |
| Figure D.4 TNP-48 Package Dimensions | 346 | Swapped with new one. |