



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	SCI
Peripherals	PWM, WDT
Number of I/O	30
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN
Supplier Device Package	48-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36024ftv

Section 15	Power-On Reset and Low-Voltage Detection Circuits (Optional).....	229
15.1	Features.....	229
15.2	Register Descriptions.....	230
15.2.1	Low-Voltage-Detection Control Register (LVDCR).....	231
15.2.2	Low-Voltage-Detection Status Register (LVDSR).....	232
15.3	Operation.....	233
15.3.1	Power-On Reset Circuit.....	233
15.3.2	Low-Voltage Detection Circuit.....	234
Section 16	Power Supply Circuit.....	237
16.1	When Using Internal Power Supply Step-Down Circuit.....	237
16.2	When Not Using Internal Power Supply Step-Down Circuit.....	238
Section 17	List of Registers.....	225
17.1	Register Addresses (Address Order).....	226
17.2	Register Bits.....	230
17.3	Register States in Each Operating Mode.....	233
Section 18	Electrical Characteristics.....	251
18.1	Absolute Maximum Ratings.....	251
18.2	Electrical Characteristics (F-ZTAT™ Version).....	251
18.2.1	Power Supply Voltage and Operating Ranges.....	251
18.2.2	DC Characteristics.....	254
18.2.3	AC Characteristics.....	259
18.2.4	A/D Converter Characteristics.....	262
18.2.5	Watchdog Timer Characteristics.....	263
18.2.6	Flash Memory Characteristics.....	264
18.2.7	Power-Supply-Voltage Detection Circuit Characteristics (Optional).....	266
18.2.8	Power-On Reset Circuit Characteristics (Optional).....	267
18.3	Electrical Characteristics (Masked ROM Version).....	267
18.3.1	Power Supply Voltage and Operating Ranges.....	267
18.3.2	DC Characteristics.....	270
18.3.3	AC Characteristics.....	275
18.3.4	A/D Converter Characteristics.....	278
18.3.5	Watchdog Timer Characteristics.....	279
18.3.6	Power-Supply-Voltage Detection Circuit Characteristics (Optional).....	280
18.3.7	Power-On Reset Circuit Characteristics (Optional).....	281
18.4	Operation Timing.....	281

Figures

Section 1 Overview

Figure 1.1	Internal Block Diagram	3
Figure 1.2	Pin Arrangement (FP-64E)	4
Figure 1.3	Pin Arrangement (FP-48F, FP-48B, TNP-48)	5

Section 2 CPU

Figure 2.1	Memory Map (1)	10
Figure 2.1	Memory Map (2)	11
Figure 2.2	CPU Registers	12
Figure 2.3	Usage of General Registers	13
Figure 2.4	Relationship between Stack Pointer and Stack Area	14
Figure 2.5	General Register Data Formats (1)	16
Figure 2.5	General Register Data Formats (2)	17
Figure 2.6	Memory Data Formats	18
Figure 2.7	Instruction Formats	29
Figure 2.8	Branch Address Specification in Memory Indirect Mode	33
Figure 2.9	On-Chip Memory Access Cycle	35
Figure 2.10	On-Chip Peripheral Module Access Cycle (3-State Access)	36
Figure 2.11	CPU Operation States	37
Figure 2.12	State Transitions	38
Figure 2.13	Example of Timer Configuration with Two Registers Allocated to Same Address	39

Section 3 Exception Handling

Figure 3.1	Reset Sequence	54
Figure 3.2	Stack Status after Exception Handling	56
Figure 3.3	Interrupt Sequence	57
Figure 3.4	Port Mode Register Setting and Interrupt Request Flag Clearing Procedure	58

Section 4 Address Break

Figure 4.1	Block Diagram of Address Break	59
Figure 4.2	Address Break Interrupt Operation Example (1)	63
Figure 4.2	Address Break Interrupt Operation Example (2)	63

Section 5 Clock Pulse Generators

Figure 5.1	Block Diagram of Clock Pulse Generators	65
Figure 5.2	Block Diagram of System Clock Generator	65
Figure 5.3	Typical Connection to Crystal Resonator	66
Figure 5.4	Equivalent Circuit of Crystal Resonator	66

Table 7.4	Reprogram Data Computation Table	88
Table 7.5	Additional-Program Data Computation Table	88
Table 7.6	Programming Time	88
Section 10 Timer V		
Table 10.1	Pin Configuration.....	119
Table 10.2	Clock Signals to Input to TCNTV and Counting Conditions	122
Section 11 Timer W		
Table 11.1	Timer W Functions	136
Table 11.2	Pin Configuration.....	138
Section 13 Serial Communication Interface 3 (SCI3)		
Table 13.1	Channel Configuration.....	175
Table 13.2	Pin Configuration.....	177
Table 13.3	Examples of BRR Settings for Various Bit Rates (Asynchronous Mode) (1)	185
Table 13.3	Examples of BRR Settings for Various Bit Rates (Asynchronous Mode) (2)	186
Table 13.3	Examples of BRR Settings for Various Bit Rates (Asynchronous Mode) (3)	187
Table 13.4	Maximum Bit Rate for Each Frequency (Asynchronous Mode)	188
Table 13.5	Examples of BRR Settings for Various Bit Rates (Clocked Synchronous Mode) (1)	189
Table 13.5	Examples of BRR Settings for Various Bit Rates (Clocked Synchronous Mode) (2)	190
Table 13.6	SSR Status Flags and Receive Data Handling	197
Table 13.7	SCI3 Interrupt Requests.....	214
Section 14 A/D Converter		
Table 14.1	Pin Configuration.....	219
Table 14.2	Analog Input Channels and Corresponding ADDR Registers	220
Table 14.3	A/D Conversion Time (Single Mode).....	225
Section 15 Power-On Reset and Low-Voltage Detection Circuits (Optional)		
Table 15.1	LVDCR Settings and Select Functions.....	232
Section 18 Electrical Characteristics		
Table 18.1	Absolute Maximum Ratings	251
Table 18.2	DC Characteristics (1)	254
Table 18.2	DC Characteristics (2)	258
Table 18.3	AC Characteristics	259
Table 18.4	Serial Interface (SCI3) Timing	261
Table 18.5	A/D Converter Characteristics.....	262
Table 18.6	Watchdog Timer Characteristics.....	263
Table 18.7	Flash Memory Characteristics	264

Type	Symbol	Pin No.		I/O	Functions
		FP-64E	FP-48F, FP-48B, TNP-48		
Timer V	TMOV	30	24	Output	This is an output pin for waveforms generated by the output compare function.
	TMCIV	29	23	Input	External event input pin.
	TMRIV	28	22	Input	Counter reset input pin.
	TRGV	54	40	Input	Counter start trigger input pin.
Timer W	FTCI	36	26	Input	External event input pin.
	FTIOA to FTIOD	37 to 40	27 to 30	I/O	Output compare output/ input capture input/ PWM output pin
Serial communication interface (SCI)	TXD, TXD_2, TXD_3*	46, 56, 27	36, 42, 21	Output	Transmit data output pin
	RXD, RXD_2, RXD_3*	45, 57, 26	35, 43, 20	Input	Receive data input pin
	SCK3, SCK3_2, SCK3_3*	44, 58, 25	34, 44, 19	I/O	Clock I/O pin
A/D converter	AN3 to AN0	59 to 62	45 to 48	Input	Analog input pin
	ADTRG	22	16	Input	A/D converter trigger input pin.
I/O ports	PB3 to PB0	59 to 62	45 to 48	Input	4-bit input port.
	P17 to P14, P12 to P10	54 to 51, 25 to 23	40 to 37, 19 to 17	I/O	7-bit I/O port.
	P22 to P20	46 to 44	36 to 34	I/O	3-bit I/O port.
	P57 to P50	27, 26, 22 to 19, 14, 13	21, 20, 16 to 11	I/O	8-bit I/O port
	P76 to P70	30 to 28, 55 to 58	24 to 22, 41 to 44	I/O	7-bit I/O port
	P84 to P80	40 to 36	30 to 26	I/O	5-bit I/O port.
E10T	E10T_0, E10T_1, E10T_2	41, 42, 43	31, 32, 33		Interface pin for the E10T, E8, or E7 emulator

Note: * The SCK3_3, RXD_3, and TXD_3 pins are not multiplexed in the H8/36014.

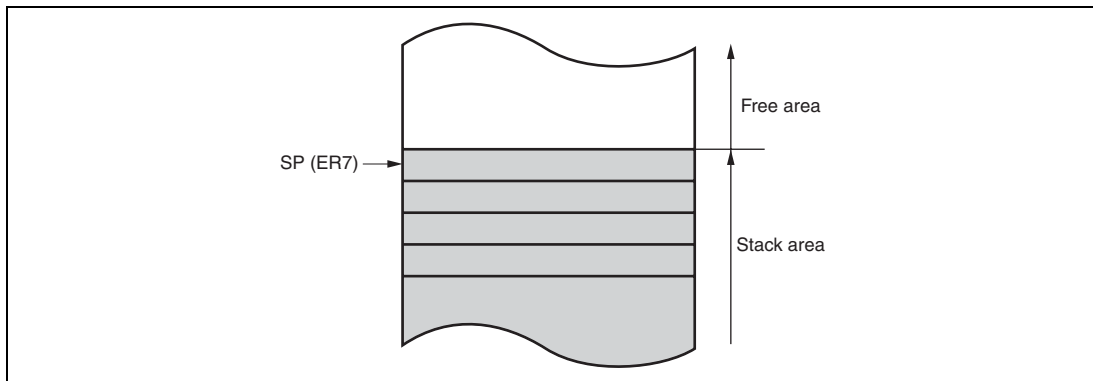


Figure 2.4 Relationship between Stack Pointer and Stack Area

2.2.2 Program Counter (PC)

This 24-bit counter indicates the address of the next instruction the CPU will execute. The length of all CPU instructions is 2 bytes (one word), so the least significant PC bit is ignored. (When an instruction is fetched, the least significant PC bit is regarded as 0). The PC is initialized when the start address is loaded by the vector address generated during reset exception-handling sequence.

2.2.3 Condition-Code Register (CCR)

This 8-bit register contains internal CPU status information, including an interrupt mask bit (I) and half-carry (H), negative (N), zero (Z), overflow (V), and carry (C) flags. The I bit is initialized to 1 by reset exception-handling sequence, but other bits are not initialized.

Some instructions leave flag bits unchanged. Operations can be performed on the CCR bits by the LDC, STC, ANDC, ORC, and XORC instructions. The N, Z, V, and C flags are used as branching conditions for conditional branch (Bcc) instructions.

For the action of each instruction on the flag bits, see Appendix A.1, Instruction List.

Note: * Refers to the operand size.

B: Byte

W: Word

L: Longword

Table 2.5 Shift Instructions

Instruction	Size*	Function
SHAL SHAR	B/W/L	Rd (shift) → Rd Performs an arithmetic shift on general register contents.
SHLL SHLR	B/W/L	Rd (shift) → Rd Performs a logical shift on general register contents.
ROTL ROTR	B/W/L	Rd (rotate) → Rd Rotates general register contents.
ROTXL ROTXR	B/W/L	Rd (rotate) → Rd Rotates general register contents through the carry flag.

Note: * Refers to the operand size.

B: Byte

W: Word

L: Longword

As a result of the BSET instruction, bit 0 in PDR5 becomes 1, and P50 outputs a high-level signal. However, bits 7 and 6 of PDR5 end up with different values. To prevent this problem, store a copy of the PDR5 data in a work area in memory. Perform the bit manipulation on the data in the work area, then write this data to PDR5.

- Prior to executing BSET

```
MOV.B  #80,  R0L
MOV.B  R0L,  @RAM0
MOV.B  R0L,  @PDR5
```

The PDR5 value (H'80) is written to a work area in memory (RAM0) as well as to PDR5.

	P57	P56	P55	P54	P53	P52	P51	P50
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1	1
PDR5	1	0	0	0	0	0	0	0
RAM0	1	0	0	0	0	0	0	0

- BSET instruction executed

```
BSET  #0,  @RAM0
```

The BSET instruction is executed designating the PDR5 work area (RAM0).

- After executing BSET

```
MOV.B  @RAM0, R0L
MOV.B  R0L,  @PDR5
```

The work area (RAM0) value is written to PDR5.

	P57	P56	P55	P54	P53	P52	P51	P50
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	High level
PCR5	0	0	1	1	1	1	1	1
PDR5	1	0	0	0	0	0	0	1
RAM0	1	0	0	0	0	0	0	1

7.1 Block Configuration

Figure 7.1 shows the block configuration of 32-kbyte flash memory. The thick lines indicate erasing units, the narrow lines indicate programming units, and the values are addresses. The flash memory is divided into 1 kbyte $\times$ 4 blocks and 28 kbytes $\times$ 1 block. Erasing is performed in these units. Programming is performed in 128-byte units starting from an address with lower eight bits H'00 or H'80.

Erase unit 1kbyte	H'0000	H'0001	H'0002	← Programming unit: 128 bytes →	H'007F
	H'0080	H'0081	H'0082		H'00FF
Erase unit 1kbyte	H'0380	H'0381	H'0382		H'03FF
	H'0400	H'0401	H'0402	← Programming unit: 128 bytes →	H'047F
	H'0480	H'0481	H'0481		H'04FF
Erase unit 1kbyte					
	H'0780	H'0781	H'0782		H'07FF
	H'0800	H'0801	H'0802	← Programming unit: 128 bytes →	H'087F
Erase unit 1kbyte	H'0880	H'0881	H'0882		H'08FF
	H'0B80	H'0B81	H'0B82		H'0BFF
Erase unit 1kbyte	H'0C00	H'0C01	H'0C02	← Programming unit: 128 bytes →	H'0C7F
	H'0C80	H'0C81	H'0C82		H'0CFF
Erase unit 28 kbytes	H'0F80	H'0F81	H'0F82		H'0FFF
	H'1000	H'1001	H'1002	← Programming unit: 128 bytes →	H'107F
	H'1080	H'1081	H'1082		H'10FF
	H'7F80	H'7F81	H'7F82		H'7FFF

Figure 7.1 Flash Memory Block Configuration

10.2 Input/Output Pins

Table 10.1 shows the timer V pin configuration.

Table 10.1 Pin Configuration

Name	Abbreviation	I/O	Function
Timer V output	TMOV	Output	Timer V waveform output
Timer V clock input	TMCIV	Input	Clock input to TCNTV
Timer V reset input	TMRIV	Input	External input to reset TCNTV
Trigger input	TRGV	Input	Trigger input to initiate counting

10.3 Register Descriptions

Time V has the following registers.

- Timer counter V (TCNTV)
- Timer constant register A (TCORA)
- Timer constant register B (TCORB)
- Timer control register V0 (TCRV0)
- Timer control/status register V (TCSRv)
- Timer control register V1 (TCRV1)

10.3.1 Timer Counter V (TCNTV)

TCNTV is an 8-bit up-counter. The clock source is selected by bits CKS2 to CKS0 in timer control register V0 (TCRV0). The TCNTV value can be read and written by the CPU at any time. TCNTV can be cleared by an external reset input signal, or by compare match A or B. The clearing signal is selected by bits CCLR1 and CCLR0 in TCRV0.

When TCNTV overflows, OVF is set to 1 in timer control/status register V (TCSRv).

TCNTV is initialized to H'00.

11.3.4 Timer Status Register W (TSRW)

TSRW shows the status of interrupt requests.

Bit	Bit Name	Initial Value	R/W	Description
7	OVF	0	R/W	Timer Overflow Flag [Setting condition] When TCNT overflows from H'FFFF to H'0000 [Clearing condition] Read OVF when OVF = 1, then write 0 in OVF
6 to 4	—	All 1	—	Reserved These bits are always read as 1.
3	IMFD	0	R/W	Input Capture/Compare Match Flag D [Setting conditions] • TCNT = GRD when GRD functions as an output compare register • The TCNT value is transferred to GRD by an input capture signal when GRD functions as an input capture register [Clearing condition] Read IMFD when IMFD = 1, then write 0 in IMFD
2	IMFC	0	R/W	Input Capture/Compare Match Flag C [Setting conditions] • TCNT = GRC when GRC functions as an output compare register • The TCNT value is transferred to GRC by an input capture signal when GRC functions as an input capture register [Clearing condition] Read IMFC when IMFC = 1, then write 0 in IMFC

Figure 11.8 shows an example of buffer operation when the GRA is set as an input-capture register and GRC is set as the buffer register for GRA. TCNT operates as a free-running counter, and FTIOA captures both rising and falling edge of the input signal. Due to the buffer operation, the GRA value is transferred to GRC by input-capture A and the TCNT value is stored in GRA.

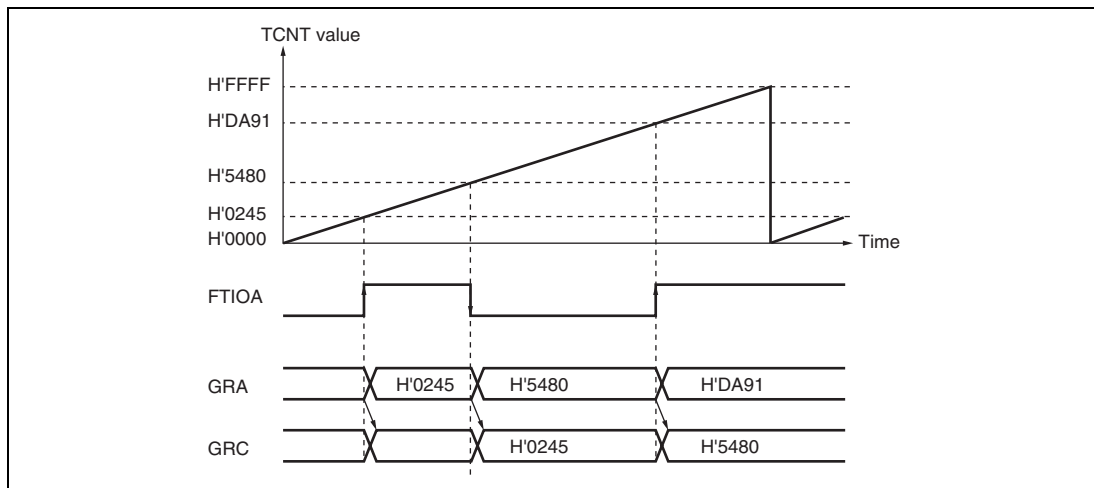


Figure 11.8 Buffer Operation Example (Input Capture)

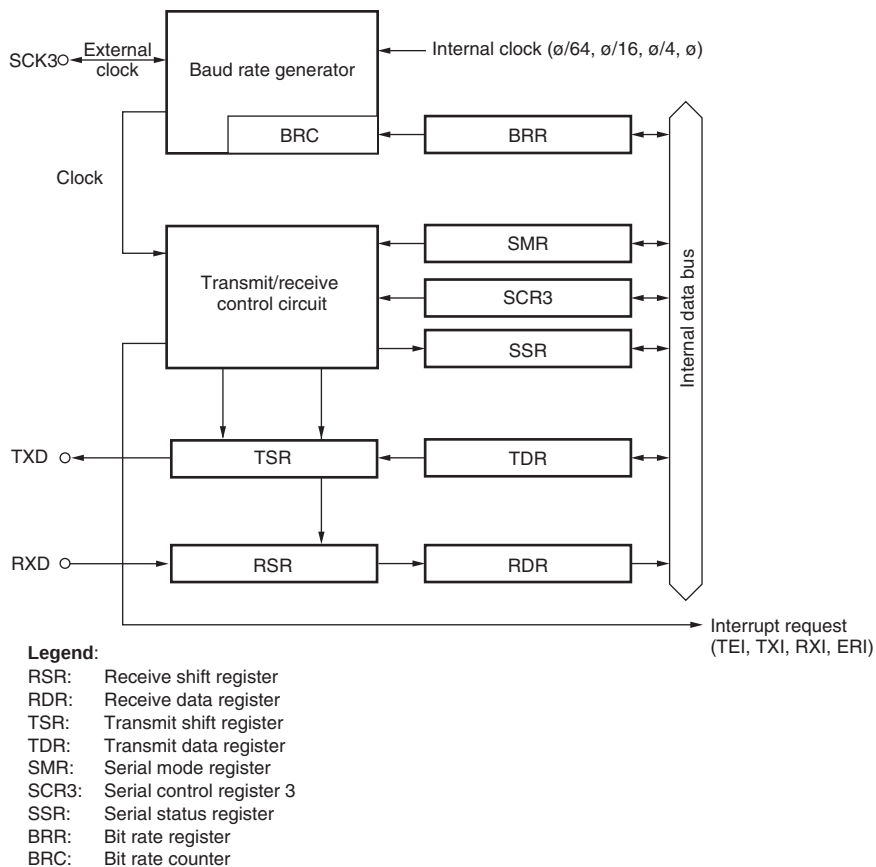


Figure 13.1 Block Diagram of SCI3

Bit	Bit Name	Initial Value	R/W	Description
3	PER	0	R/W	Parity Error [Setting condition] - When a parity error is detected during reception [Clearing condition] - When 0 is written to PER after reading PER = 1
2	TEND	1	R	Transmit End [Setting conditions] - When the TE bit in SCR3 is 0 - When TDRE = 1 at transmission of the last bit of a 1-frame serial transmit character [Clearing conditions] - When 0 is written to TDRE after reading TDRE = 1 - When the transmit data is written to TDR
1	MPBR	0	R	Multiprocessor Bit Receive MPBR stores the multiprocessor bit in the receive character data. When the RE bit in SCR3 is cleared to 0, its state is retained.
0	MPBT	0	R/W	Multiprocessor Bit Transfer MPBT stores the multiprocessor bit to be added to the transmit character data.

13.5 Operation in Clocked Synchronous Mode

Figure 13.9 shows the general format for clocked synchronous communication. In clocked synchronous mode, data is transmitted or received synchronous with clock pulses. A single character in the transmit data consists of the 8-bit data starting from the LSB. In clocked synchronous serial communication, data on the transmission line is output from one falling edge of the synchronization clock to the next. In clocked synchronous mode, the SCI3 receives data in synchronous with the rising edge of the synchronization clock. After 8-bit data is output, the transmission line holds the MSB state. In clocked synchronous mode, no parity or multiprocessor bit is added. Inside the SCI3, the transmitter and receiver are independent units, enabling full-duplex communication through the use of a common clock. Both the transmitter and the receiver also have a double-buffered structure, so data can be read or written during transmission or reception, enabling continuous data transfer.

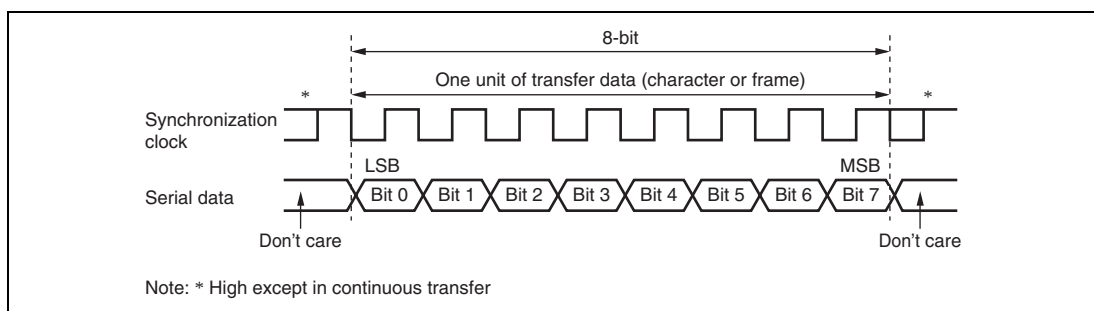


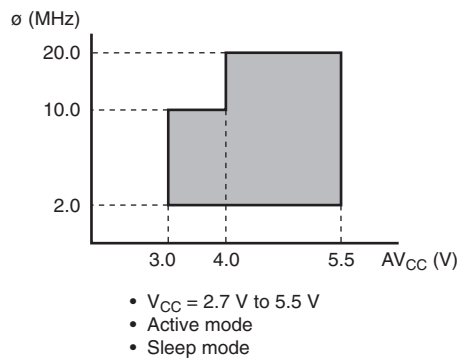
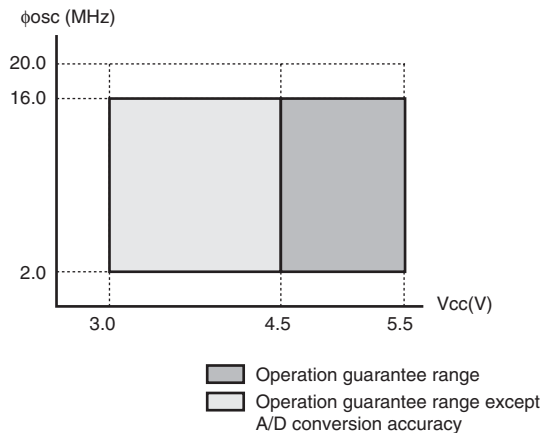
Figure 13.9 Data Format in Clocked Synchronous Communication

13.5.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCK3 pin can be selected, according to the setting of the COM bit in SMR and CKE0 and CKE1 bits in SCR3. When the SCI3 is operated on an internal clock, the synchronization clock is output from the SCK3 pin. Eight synchronization clock pulses are output in the transfer of one character, and when no transfer is performed the clock is fixed high.

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Reference Figure
				Min	Typ	Max		
RES pin low width	t_{REL}	RES	At power-on and in modes other than those below	t_{rc}	—	—	ms	Figure 18.2
			In active mode and sleep mode operation	200	—	—	ns	
Input pin high width	t_{IH}	NMI, IRQ0, IRQ3, WKP0 to WKP5, TMCIV, TMRIV, TRGV, ADTRG, FTCI, FTIOA to FTIOD		2	—	—	t_{cyc}	Figure 18.3
Input pin low width	t_{IL}	NMI, IRQ0, IRQ3, WKP0 to WKP5, TMCIV, TMRIV, TRGV, ADTRG, FTCI, FTIOA to FTIOD		2	—	—	t_{cyc}	

- Notes: 1. When an external clock is input, the minimum system clock oscillator frequency is 1.0 MHz.
2. Determined by MA2 to MA0 in system control register 2 (SYSCR2).

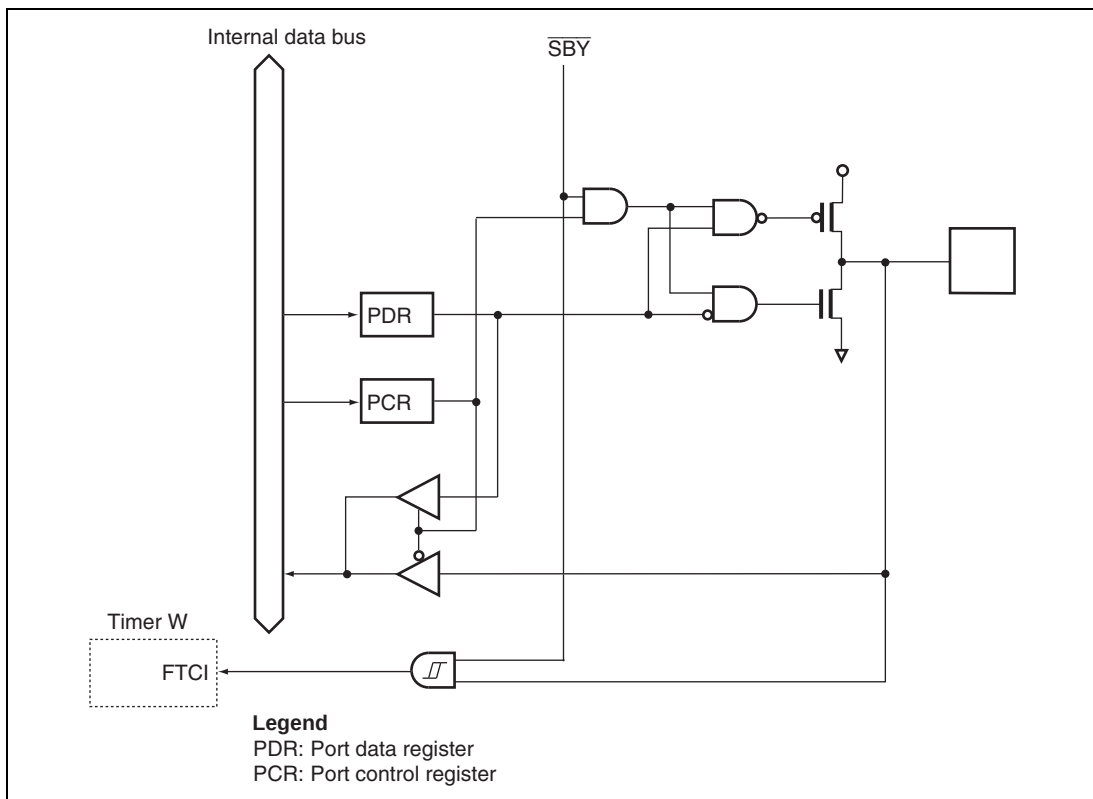
(3) Analog Power Supply Voltage and A/D Converter Accuracy Guarantee Range**(4) Range of Power Supply Voltage and Oscillation Frequency when Low-Voltage Detection Circuit is Used**

Mnemonic		Operand Size	Addressing Mode and Instruction Length (bytes)								Operation	Condition Code						No. of States ^{*1}	
			#xx	Rn	@ERn	@ (d, ERn)	@-ERn/@ERn+	@aa	@ (d, PC)	@@aa								I	Normal
												I	H	N	Z	V	C		
JMP	JMP @ERn	—			2						PC ← ERn	—	—	—	—	—	—	4	
	JMP @aa:24	—						4			PC ← aa:24	—	—	—	—	—	—	6	
	JMP @@aa:8	—								2	PC ← @aa:8	—	—	—	—	—	—	8	10
BSR	BSR d:8	—							2		PC → @-SP PC ← PC+d:8	—	—	—	—	—	—	6	8
	BSR d:16	—							4		PC → @-SP PC ← PC+d:16	—	—	—	—	—	—	8	10
JSR	JSR @ERn	—			2						PC → @-SP PC ← ERn	—	—	—	—	—	—	6	8
	JSR @aa:24	—						4			PC → @-SP PC ← aa:24	—	—	—	—	—	—	8	10
	JSR @@aa:8	—								2	PC → @-SP PC ← @aa:8	—	—	—	—	—	—	8	12
RTS	RTS	—								2	PC ← @SP+	—	—	—	—	—	—	8	10

8. Block transfer instructions

Mnemonic		Operand Size	Addressing Mode and Instruction Length (bytes)								Operation	Condition Code						No. of States ^{*1}		
			#xx	Rn	@ERn	@{d, ERn}	@-ERn/@ERn+	@aa	@{d, PC}	@@aa			I	H	N	Z	V	C	Normal	Advanced
EEPMOV	EEPMOV. B	—									4	if R4L ≠ 0 then repeat @R5 → @R6 R5+1 → R5 R6+1 → R6 R4L-1 → R4L until R4L=0 else next	—	—	—	—	—	—	8+4n ²	
	EEPMOV. W	—									4	if R4 ≠ 0 then repeat @R5 → @R6 R5+1 → R5 R6+1 → R6 R4-1 → R4 until R4=0 else next	—	—	—	—	—	—	8+4n ²	

- Notes: 1. The number of states in cases where the instruction code and its operands are located in on-chip memory is shown here. For other cases see Appendix A.3, Number of Execution States.
2. n is the value set in register R4L or R4.
- (1) Set to 1 when a carry or borrow occurs at bit 11; otherwise cleared to 0.
 - (2) Set to 1 when a carry or borrow occurs at bit 27; otherwise cleared to 0.
 - (3) Retains its previous value when the result is zero; otherwise cleared to 0.
 - (4) Set to 1 when the adjustment produces a carry; otherwise retains its previous value.
 - (5) The number of states required for execution of an instruction that transfers data in synchronization with the E clock is variable.
 - (6) Set to 1 when the divisor is negative; otherwise cleared to 0.
 - (7) Set to 1 when the divisor is zero; otherwise cleared to 0.
 - (8) Set to 1 when the quotient is negative; otherwise cleared to 0.

**Figure B.22 Port 8 Block Diagram (P80)**