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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	SCI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	30
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN
Supplier Device Package	48-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36024gftv

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Contents

2.3 Data Formats

The H8/300H CPU can process 1-bit, 4-bit (BCD), 8-bit (byte), 16-bit (word), and 32-bit (longword) data. Bit-manipulation instructions operate on 1-bit data by accessing bit n (n = 0, 1, 2, …, 7) of byte operand data. The DAA and DAS decimal-adjust instructions treat byte data as two digits of 4-bit BCD data.

2.3.1 General Register Data Formats

Figure 2.5 shows the data formats in general registers.

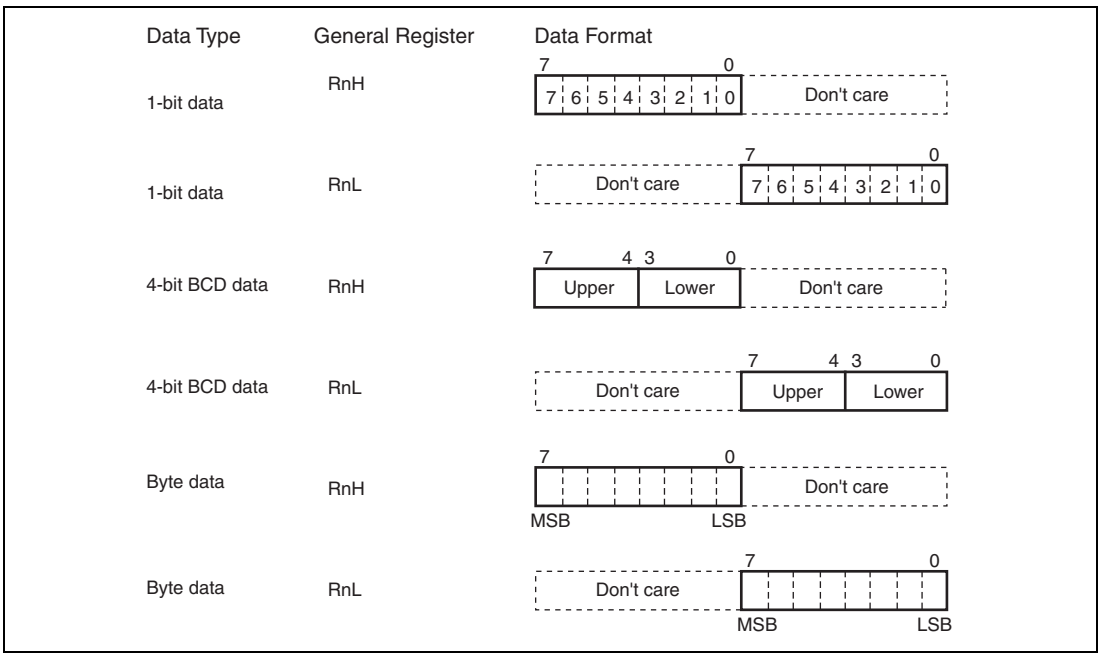


Figure 2.5 General Register Data Formats (1)

(1) Bit manipulation for two registers assigned to the same address

Example: Bit manipulation for the timer load register and timer counter

(Applicable for timer B and timer C, not for the group of this LSI.)

Figure 2.13 shows an example of a timer in which two timer registers are assigned to the same address. When a bit manipulation instruction accesses the timer load register and timer counter of a reloadable timer, since these two registers share the same address, the following operations takes place.

1. Data is read in byte units.
2. The CPU sets or resets the bit to be manipulated with the bit manipulation instruction.
3. The written data is written again in byte units to the timer load register.

The timer is counting, so the value read is not necessarily the same as the value in the timer load register. As a result, bits other than the intended bit in the timer counter may be modified and the modified value may be written to the timer load register.

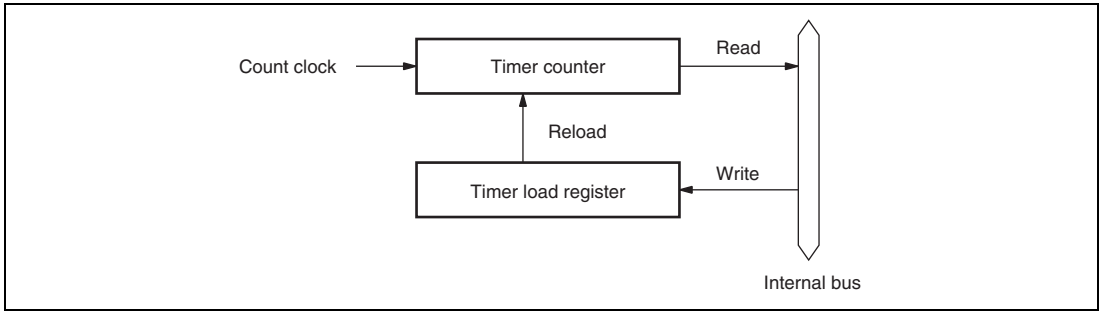


Figure 2.13 Example of Timer Configuration with Two Registers Allocated to Same Address

(2) Bit Manipulation in a Register Containing a Write-Only Bit

Example 3: BCLR instruction executed designating port 5 control register PCR5

P57 and P56 are input pins, with a low-level signal input at P57 and a high-level signal input at P56. P55 to P50 are output pins that output low-level signals. An example of setting the P50 pin as an input pin by the BCLR instruction is shown below. It is assumed that a high-level signal will be input to this input pin.

- Prior to executing BCLR

	P57	**P56**	**P55**	**P54**	**P53**	**P52**	**P51**	**P50**
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1	1
PDR5	1	0	0	0	0	0	0	0

- BCLR instruction executed

```
BCLR    #0,     @PCR5
```

The BCLR instruction is executed for PCR5.

- After executing BCLR

	P57	**P56**	**P55**	**P54**	**P53**	**P52**	**P51**	**P50**
Input/output	Output	Output	Output	Output	Output	Output	Output	Input
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	High level
PCR5	1	1	1	1	1	1	1	0
PDR5	1	0	0	0	0	0	0	0

- Description on operation

1. When the BCLR instruction is executed, first the CPU reads PCR5. Since PCR5 is a write-only register, the CPU reads a value of H'FF, even though the PCR5 value is actually H'3F.
2. Next, the CPU clears bit 0 in the read data to 0, changing the data to H'FE.
3. Finally, H'FE is written to PCR5 and BCLR instruction execution ends.

   As a result of this operation, bit 0 in PCR5 becomes 0, making P50 an input port. However, bits 7 and 6 in PCR5 change to 1, so that P57 and P56 change from input pins to output pins. To prevent this problem, store a copy of the PCR5 data in a work area in memory and manipulate data of the bit in the work area, then write this data to PCR5.

3.2.2 Interrupt Edge Select Register 2 (IEGR2)

IEGR2 selects the direction of an edge that generates interrupt requests of the pins $\overline{\text{ADTRG}}$ and $\overline{\text{WKP5}}$ to $\overline{\text{WKP0}}$.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 1	—	Reserved These bits are always read as 1.
5	WPEG5	0	R/W	WKP5 Edge Select 0: Falling edge of $\overline{\text{WKP5}}$ ($\overline{\text{ADTRG}}$) pin input is detected 1: Rising edge of $\overline{\text{WKP5}}$ ($\overline{\text{ADTRG}}$) pin input is detected
4	WPEG4	0	R/W	WKP4 Edge Select 0: Falling edge of $\overline{\text{WKP4}}$ pin input is detected 1: Rising edge of $\overline{\text{WKP4}}$ pin input is detected
3	WPEG3	0	R/W	WKP3 Edge Select 0: Falling edge of $\overline{\text{WKP3}}$ pin input is detected 1: Rising edge of $\overline{\text{WKP3}}$ pin input is detected
2	WPEG2	0	R/W	WKP2 Edge Select 0: Falling edge of $\overline{\text{WKP2}}$ pin input is detected 1: Rising edge of $\overline{\text{WKP2}}$ pin input is detected
1	WPEG1	0	R/W	WKP1Edge Select 0: Falling edge of $\overline{\text{WKP1}}$ pin input is detected 1: Rising edge of $\overline{\text{WKP1}}$ pin input is detected
0	WPEG0	0	R/W	WKP0 Edge Select 0: Falling edge of $\overline{\text{WKP0}}$ pin input is detected 1: Rising edge of $\overline{\text{WKP0}}$ pin input is detected

11.4 Operation

The timer W has the following operating modes.

- Normal Operation
- PWM Operation

11.4.1 Normal Operation

TCNT performs free-running or periodic counting operations. After a reset, TCNT is set as a free-running counter. When the CTS bit in TMRW is set to 1, TCNT starts incrementing the count. When the count overflows from H'FFFF to H'0000, the OVF flag in TSRW is set to 1. If the OVIE in TIERW is set to 1, an interrupt request is generated. Figure 11.2 shows free-running counting.

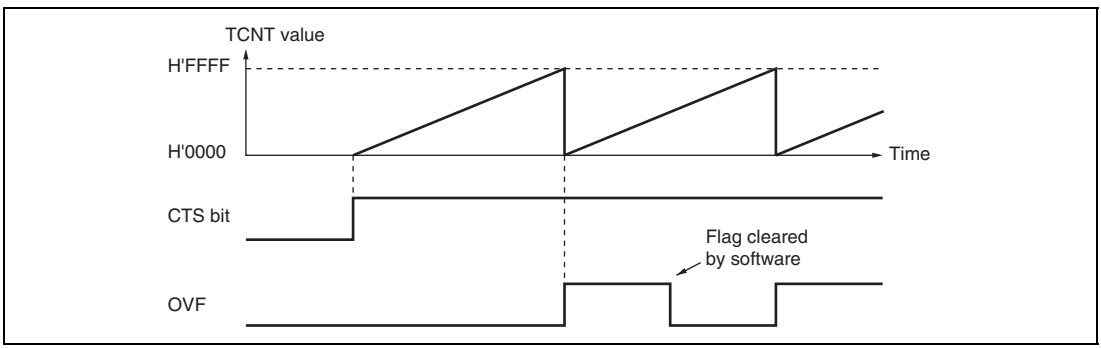


Figure 11.2 Free-Running Counter Operation

11.4.2 PWM Operation

In PWM mode, PWM waveforms are generated by using GRA as the period register and GRB, GRC, and GRD as duty registers. PWM waveforms are output from the FTIOB, FTIOC, and FTIOD pins. Up to three-phase PWM waveforms can be output. In PWM mode, a general register functions as an output compare register automatically. The output level of each pin depends on the corresponding timer output level set bit (TOB, TOC, and TOD) in TCRW. When TOB is 1, the FTIOB output goes to 1 at compare match A and to 0 at compare match B. When TOB is 0, the FTIOB output goes to 0 at compare match A and to 1 at compare match B. Thus the compare match output level settings in TIOR0 and TIOR1 are ignored for the output pin set to PWM mode. If the same value is set in the cycle register and the duty register, the output does not change when a compare match occurs.

Figure 11.9 shows an example of operation in PWM mode. The output signals go to 1 and TCNT is cleared at compare match A, and the output signals go to 0 at compare match B, C, and D (TOB, TOC, and TOD = 1: initial output values are set to 1).

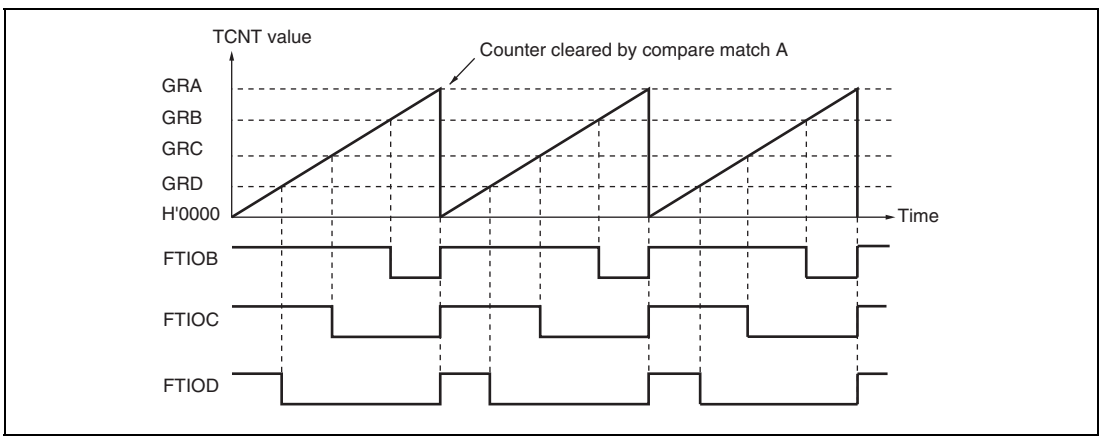
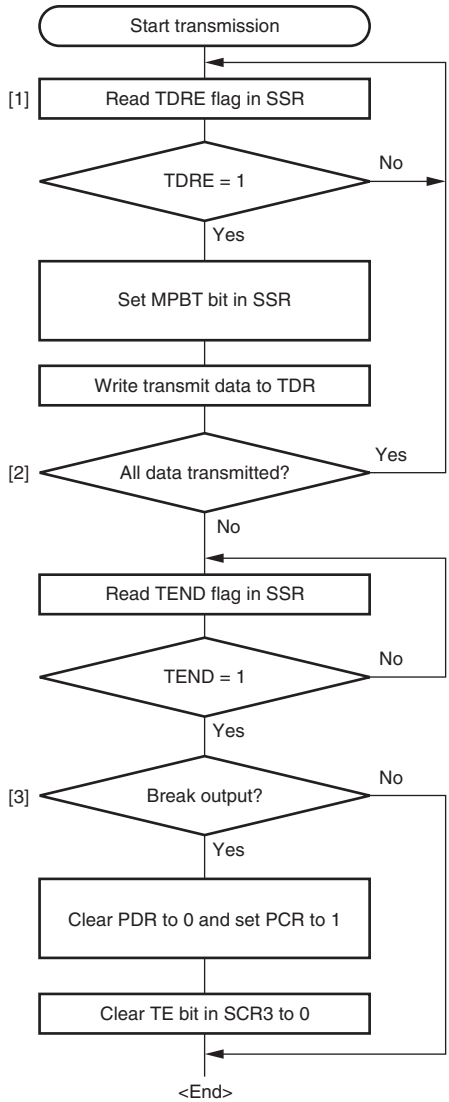


Figure 11.9 PWM Mode Example (1)



[1] Read SSR and check that the TDRE flag is set to 1, set the MPBT bit in SSR to 0 or 1, then write transmit data to TDR. When data is written to TDR, the TDRE flag is automatically cleared to 0.

[2] To continue serial transmission, be sure to read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR. When data is written to TDR, the TDRE flag is automatically cleared to 0.

[3] To output a break in serial transmission, set the port PCR to 1, clear PDR to 0, then clear the TE bit in SCR3 to 0.

Figure 13.16 Sample Multiprocessor Serial Transmission Flowchart

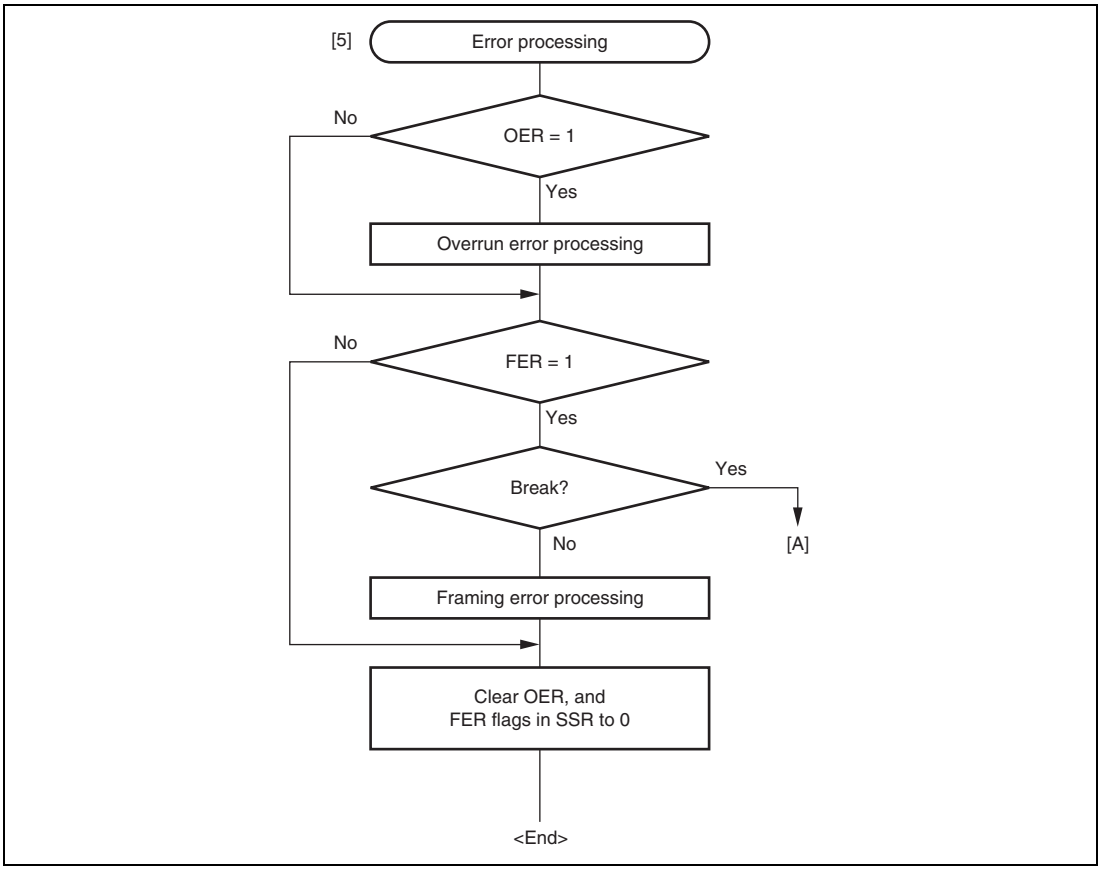


Figure 13.17 Sample Multiprocessor Serial Reception Flowchart (2)

13.8.4 Receive Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCI3 operates on a basic clock with a frequency of 16 times the transfer rate. In reception, the SCI3 samples the falling edge of the start bit using the basic clock, and performs internal synchronization. Receive data is latched internally at the rising edge of the 8th pulse of the basic clock as shown in figure 13.19. Thus, the reception margin in asynchronous mode is given by formula (1) below.

$$M = \left\{ (0.5 - \frac{1}{2N}) - \frac{D - 0.5}{N} - (L - 0.5)\,F \right\} \times 100(\%)$$

... Formula (1)

[Legend\
N: Ratio of bit rate to clock (N = 16)
D: Clock duty (D = 0.5 to 1.0)
L: Frame length (L = 9 to 12)
F: Absolute value of clock rate deviation

Assuming values of F (absolute value of clock rate deviation) = 0 and D (clock duty) = 0.5 in formula (1), the reception margin can be given by the formula.

$$M = \{0.5 - 1/(2 \times 16)\} \times 100\ [\%] = 46.875\%$$

However, this is only the computed value, and a margin of 20% to 30% should be allowed for in system design.

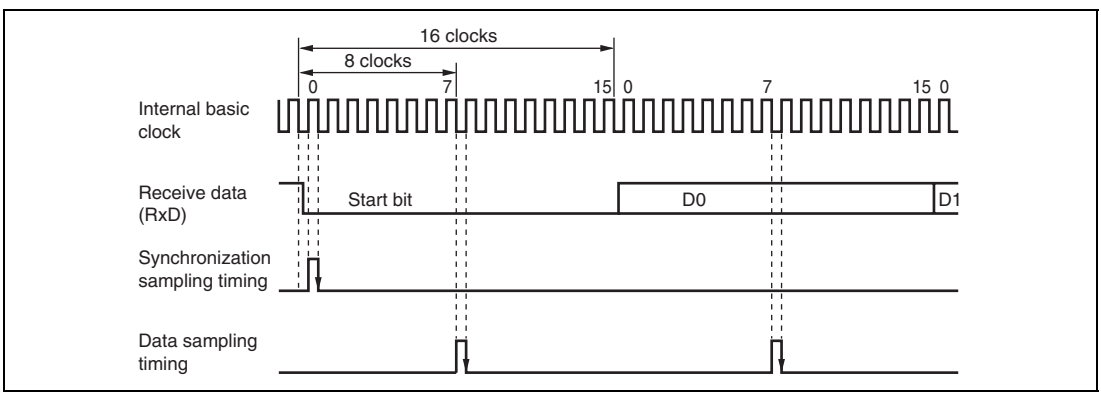


Figure 13.19 Receive Data Sampling Timing in Asynchronous Mode

17.2 Register Bits

Register bit names of the on-chip peripheral modules are described below.

Each line covers eight bits, and 16-bit registers are shown as 2 lines.

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name
SMR_3	COM	CHR	PE	PM	STOP	MP	CKS1	CKS0	SCI3_3
BRR_3	BRR7	BRR6	BRR5	BRR4	BRR3	BRR2	BRR1	BRR0	
SCR3_3	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
TDR_3	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0	
SSR_3	TDRE	RDRF	OER	FER	PER	TEND	MPBR	MPBT	
RDR_3	RDR7	RDR6	RDR5	RDR4	RDR3	RDR2	RDR1	RDR0	
SMCR	–	–	–	–	–	–	TXD_3	MSTS3_3	
LVDCR	LVDE	–	–	–	LVDSEL	LVDRE	LVDDE	LVDUE	LVDC (optional)
LVDSR	–	–	–	–	–	–	LVDDF	LVDUF	
SMR_2	COM	CHR	PE	PM	STOP	MP	CKS1	CKS0	SCI3_2
BRR_2	BRR7	BRR6	BRR5	BRR4	BRR3	BRR2	BRR1	BRR0	
SCR3_2	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
TDR_2	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0	
SSR_2	TDRE	RDRF	OER	FER	PER	TEND	MPBR	MPBT	
RDR_2	RDR7	RDR6	RDR5	RDR4	RDR3	RDR2	RDR1	RDR0	
TMRW	CTS	—	BUFEB	BUFEA	—	PWMD	PWMC	PWMB	Timer W
TCRW	CCLR	CKS2	CKS1	CKS0	TOD	TOC	TOB	TOA	
TIERW	OVIE	—	—	—	IMIED	IMIEC	IMIEB	IMIEA	
TSRW	OVF	—	—	—	IMFD	IMFC	IMFB	IMFA	
TIOR0	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0	
TIOR1	—	IOD2	IOD1	IOD0	—	IOC2	IOC1	IOC0	
TCNT	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8	
	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0	
GRA	GRA15	GRA14	GRA13	GRA12	GRA11	GRA10	GRA9	GRA8	
	GRA7	GRA6	GRA5	GRA4	GRA3	GRA2	GRA1	GRA0	
GRB	GRB15	GRB14	GRB13	GRB12	GRB11	GRB10	GRB9	GRB8	
	GRB7	GRB6	GRB5	GRB4	GRB3	GRB2	GRB1	GRB0	

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name
ABRKCR	RTINTE	CSEL1	CSEL0	ACMP2	ACMP1	ACMP0	DCMP1	DCMP0	Address break
ABRKSR	ABIF	ABIE	—	—	—	—	—	—	
BARH	BARH7	BARH6	BARH5	BARH4	BARH3	BARH2	BARH1	BARH0	
BARL	BARL7	BARL6	BARL5	BARL4	BARL3	BARL2	BARL1	BARL0	
BDRH	BDRH7	BDRH6	BDRH5	BDRH4	BDRH3	BDRH2	BDRH1	BDRH0	
BDRL	BDRL7	BDRL6	BDRL5	BDRL4	BDRL3	BDRL2	BDRL1	BDRL0	
PUCR1	PUCR17	PUCR16	PUCR15	PUCR14	—	PUCR12	PUCR11	PUCR10	I/O port
PUCR5	—	—	PUCR55	PUCR54	PUCR53	PUCR52	PUCR51	PUCR50	
PDR1	P17	P16	P15	P14	—	P12	P11	P10	
PDR2	—	—	—	—	—	P22	P21	P20	
PDR5	P57	P56	P55	P54	P53	P52	P51	P50	
PDR7	—	P76	P75	P74	P73	P72	P71	P70	
PDR8	—	—	—	P84	P83	P82	P81	P80	
PDRB	—	—	—	—	PB3	PB2	PB1	PB0	
PMR1	IRQ3	—	—	IRQ0	TXD2	—	TXD	—	
PMR5	POF57	POF56	WKP5	WKP4	WKP3	WKP2	WKP1	WKP0	
PCR1	PCR17	PCR16	PCR15	PCR14	—	PCR12	PCR11	PCR10	
PCR2	—	—	—	—	—	PCR22	PCR21	PCR20	
PCR5	PCR57	PCR56	PCR55	PCR54	PCR53	PCR52	PCR51	PCR50	
PCR7	—	PCR76	PCR75	PCR74	PCR73	PCR72	PCR71	PCR70	
PCR8	—	—	—	PCR84	PCR83	PCR82	PCR81	PCR80	
SYSCR1	SSBY	STS2	STS1	STS0	—	—	—	—	Power-down
SYSCR2	SMSEL	—	DTON	MA2	MA1	MA0	—	—	
IEGR1	—	—	—	—	IEG3	—	—	IEG0	Interrupts
IEGR2	—	—	WPEG5	WPEG4	WPEG3	WPEG2	WPEG1	WPEG0	
IENR1	IENDT	—	IENWP	—	IEN3	—	—	IEN0	
IRR1	IRRDT	—	—	—	IRRI3	—	—	IRRI0	
IWPR	—	—	IWPF5	IWPF4	IWPF3	IWPF2	IWPF1	IWPF0	
MSTCR1	—	—	MSTS3	MSTAD	MSTWD	MSTTW	MSTTV	—	Power-down
MSTCR2	MSTS3_2	—	—	—	—	—	—	—	

Note: * WDT: Watchdog timer

18.2.4 A/D Converter Characteristics

Table 18.5 A/D Converter Characteristics

V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C, unless otherwise specified.

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Notes
				Min	Typ	Max		
Analog power supply voltage	AV_{CC}	AV_{CC}		3.3	V_{CC}	5.5	V	*1
Analog input voltage	AV_{IN}	AN3 to AN0		V_{SS} – 0.3	—	AV_{CC} + 0.3	V	
Analog power supply current	AI_{OPE}	AV_{CC}	AV_{CC} = 5.0 V f_{OSC} = 20 MHz	—	—	2.0	mA	
	AI_{STOP1}	AV_{CC}		—	50	—	µA	*2 Reference value
	AI_{STOP2}	AV_{CC}		—	—	5.0	µA	*3
Analog input capacitance	C_{AIN}	AN3 to AN0		—	—	30.0	pF	
Allowable signal source impedance	R_{AIN}	AN3 to AN0		—	—	5.0	kΩ	
Resolution (data length)				10	10	10	bit	
Conversion time (single mode)			AV_{CC} = 3.3 V to 5.5 V	134	—	—	t_{cyc}	
Nonlinearity error				—	—	±7.5	LSB	
Offset error				—	—	±7.5	LSB	
Full-scale error				—	—	±7.5	LSB	
Quantization error				—	—	±0.5	LSB	
Absolute accuracy				—	—	±8.0	LSB	
Conversion time (single mode)			AV_{CC} = 4.0 V to 5.5 V	70	—	—	t_{cyc}	
Nonlinearity error				—	—	±7.5	LSB	
Offset error				—	—	±7.5	LSB	
Full-scale error				—	—	±7.5	LSB	
Quantization error				—	—	±0.5	LSB	
Absolute accuracy				—	—	±8.0	LSB	

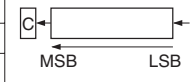
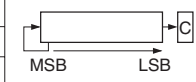
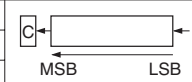
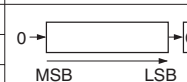
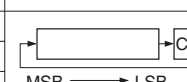
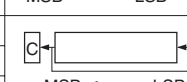
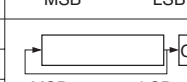
18.3.3 AC Characteristics

Table 18.11 AC Characteristics

V_{CC} = 2.7 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C, unless otherwise specified.

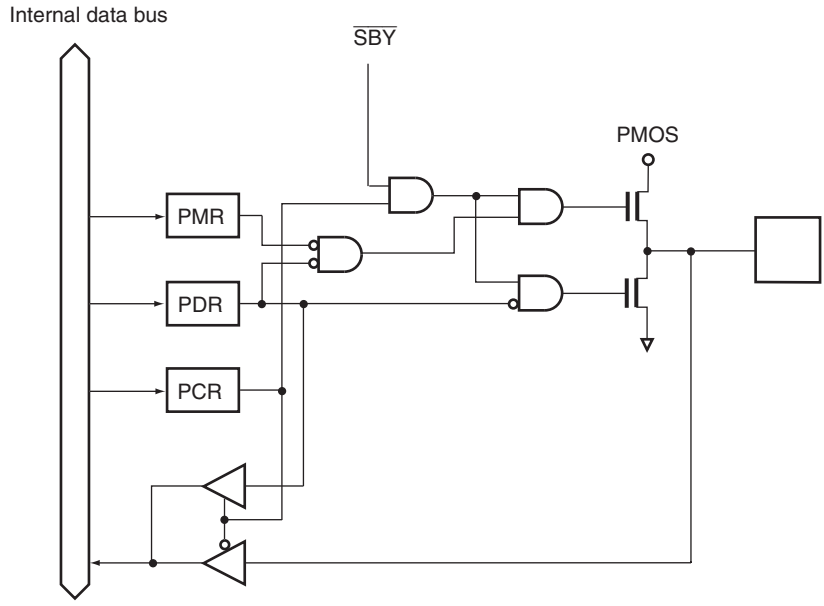
Item	Symbol	Applicable Pins	Test Condition	Values Min	Values Typ	Values Max	Unit	Reference Figure
System clock oscillation frequency	f_{OSC}	OSC1, OSC2	V_{CC} = 4.0 V to 5.5 V	2.0	—	20.0	MHz	*[1]
				2.0	—	10.0	MHz	
System clock (ϕ) cycle time	t_{cyc}			1	—	64	t_{OSC}	*[2]
				—	—	12.8	µs	
Instruction cycle time				2	—	—	t_{cyc}	
Oscillation stabilization time (crystal resonator)	t_{rc}	OSC1, OSC2		—	—	10.0	ms	
Oscillation stabilization time (ceramic resonator)	t_{rc}	OSC1, OSC2		—	—	5.0	ms	
External clock high width	t_{CPH}	OSC1	V_{CC} = 4.0 V to 5.5 V	20.0	—	—	ns	Figure 18.1
				40.0	—	—	ns	
External clock low width	t_{CPL}	OSC1	V_{CC} = 4.0 V to 5.5 V	20.0	—	—	ns	
				40.0	—	—	ns	
External clock rise time	t_{CPr}	OSC1	V_{CC} = 4.0 V to 5.5 V	—	—	10.0	ns	
				—	—	15.0	ns	
External clock fall time	t_{CPf}	OSC1	V_{CC} = 4.0 V to 5.5 V	—	—	10.0	ns	
				—	—	15.0	ns	
$\overline{RES}$ pin low width	t_{REL}	$\overline{RES}$	At power-on and in modes other than those below	t_{rc}	—	—	ms	Figure 18.2
			In active mode and sleep mode operation	200	—	—	ns	

4. Shift instructions

Mnemonic		Operand Size	Addressing Mode and Instruction Length (bytes)									Operation	Condition Code						No. of States*1	
			#xx	Rn	@ERn	@(d, ERn)	@–ERn/@ERn+	@aa	@(d, PC)	@@aa	—		I	H	N	Z	V	C	Normal	Advanced
SHAL	SHAL.B Rd	B		2									—	—	↕	↕	↕	↕	2	
	SHAL.W Rd	W		2									—	—	↕	↕	↕	↕	2	
	SHAL.L ERd	L		2									—	—	↕	↕	↕	↕	2	
SHAR	SHAR.B Rd	B		2									—	—	↕	↕	0	↕	2	
	SHAR.W Rd	W		2									—	—	↕	↕	0	↕	2	
	SHAR.L ERd	L		2									—	—	↕	↕	0	↕	2	
SHLL	SHLL.B Rd	B		2									—	—	↕	↕	0	↕	2	
	SHLL.W Rd	W		2									—	—	↕	↕	0	↕	2	
	SHLL.L ERd	L		2									—	—	↕	↕	0	↕	2	
SHLR	SHLR.B Rd	B		2									—	—	↕	↕	0	↕	2	
	SHLR.W Rd	W		2									—	—	↕	↕	0	↕	2	
	SHLR.L ERd	L		2									—	—	↕	↕	0	↕	2	
ROTXL	ROTXL.B Rd	B		2									—	—	↕	↕	0	↕	2	
	ROTXL.W Rd	W		2									—	—	↕	↕	0	↕	2	
	ROTXL.L ERd	L		2									—	—	↕	↕	0	↕	2	
ROTXR	ROTXR.B Rd	B		2									—	—	↕	↕	0	↕	2	
	ROTXR.W Rd	W		2									—	—	↕	↕	0	↕	2	
	ROTXR.L ERd	L		2									—	—	↕	↕	0	↕	2	
ROTL	ROTL.B Rd	B		2									—	—	↕	↕	0	↕	2	
	ROTL.W Rd	W		2									—	—	↕	↕	0	↕	2	
	ROTL.L ERd	L		2									—	—	↕	↕	0	↕	2	
ROTR	ROTR.B Rd	B		2									—	—	↕	↕	0	↕	2	
	ROTR.W Rd	W		2									—	—	↕	↕	0	↕	2	
	ROTR.L ERd	L		2									—	—	↕	↕	0	↕	2	

6. Branching instructions

Mnemonic		Operand Size	Addressing Mode and Instruction Length (bytes)									Operation	Condition Code						No. of States*1	
			#xx	Rn	@ERn	@(d, ERn)	@–ERn/@ERn+	@aa	@(d, PC)	@@aa	—	Branch Condition	I	H	N	Z	V	C	Normal	Advanced
Bcc	BRA d:8 (BT d:8)	—							2			If condition is true then PC ← PC+d else next; Always	—	—	—	—	—	—	4	
	BRA d:16 (BT d:16)	—							4				—	—	—	—	—	—	6	
	BRN d:8 (BF d:8)	—							2			Never	—	—	—	—	—	—	4	
	BRN d:16 (BF d:16)	—							4				—	—	—	—	—	—	6	
	BHI d:8	—							2			C/Z = 0	—	—	—	—	—	—	4	
	BHI d:16	—							4				—	—	—	—	—	—	6	
	BLS d:8	—							2			C/Z = 1	—	—	—	—	—	—	4	
	BLS d:16	—							4				—	—	—	—	—	—	6	
	BCC d:8 (BHS d:8)	—							2			C = 0	—	—	—	—	—	—	4	
	BCC d:16 (BHS d:16)	—							4				—	—	—	—	—	—	6	
	BCS d:8 (BLO d:8)	—							2			C = 1	—	—	—	—	—	—	4	
	BCS d:16 (BLO d:16)	—							4				—	—	—	—	—	—	6	
	BNE d:8	—							2			Z = 0	—	—	—	—	—	—	4	
	BNE d:16	—							4				—	—	—	—	—	—	6	
	BEQ d:8	—							2			Z = 1	—	—	—	—	—	—	4	
	BEQ d:16	—							4				—	—	—	—	—	—	6	
	BVC d:8	—							2			V = 0	—	—	—	—	—	—	4	
	BVC d:16	—							4				—	—	—	—	—	—	6	
	BVS d:8	—							2			V = 1	—	—	—	—	—	—	4	
	BVS d:16	—							4				—	—	—	—	—	—	6	
	BPL d:8	—							2			N = 0	—	—	—	—	—	—	4	
	BPL d:16	—							4				—	—	—	—	—	—	6	
	BMI d:8	—							2			N = 1	—	—	—	—	—	—	4	
	BMI d:16	—							4				—	—	—	—	—	—	6	
	BGE d:8	—							2			N⊕V = 0	—	—	—	—	—	—	4	
	BGE d:16	—							4				—	—	—	—	—	—	6	
	BLT d:8	—							2			N⊕V = 1	—	—	—	—	—	—	4	
	BLT d:16	—							4				—	—	—	—	—	—	6	
	BGT d:8	—							2			Z/(N⊕V) = 0	—	—	—	—	—	—	4	
	BGT d:16	—							4				—	—	—	—	—	—	6	
	BLE d:8	—							2			Z/(N⊕V) = 1	—	—	—	—	—	—	4	
	BLE d:16	—							4				—	—	—	—	—	—	6	



Legend
PMR: Port mode register
PDR: Port data register
PCR: Port control register

Figure B.9 Port 5 Block Diagram (P57, P56) (H8/36014)

Main Revisions and Additions in this Edition

Item	Page	Revision (See Manual for Details)
Preface	vi, vii	When using the on-chip emulator (E7, E8) for H8/36014 program development and debugging, the following restrictions must be noted. 1. The $\overline{\text{NMI}}$ pin is reserved for the E7 or E8, and cannot be used. 2. Area H'7000 to H'7FFF is used by the E7 or E8, and is not available to the user. 4. When the E7 or E8 is used, address breaks can be set as either available to the user or for use by the E7 or E8. If address breaks are set as being used by the E7 or E8, the address break control registers must not be accessed. 5. When the E7 or E8 is used, $\overline{\text{NMI}}$ is an input/output pin (open-drain in output mode). 6. Use channel 1 of the SCI3 (P21/RXD, P22/TXD) in on-board programming mode by boot mode. Note has been deleted.
Section 1 Overview 1.2 Internal Block Diagram Figure 1.1 Internal Block Diagram	3	3 Can also be used for the E7 or E8 emulator.
Figure 1.2 Pin Arrangement (FP-64E)	4	2 Can also be used for the E7 or E8 emulator.
Figure 1.3 Pin Arrangement (FP-48F, FP-48B, TNP-48)	5	2 Can also be used for the E7 or E8 emulator.
Table 1.1 Pin Functions	7	**Type** : **Functions** E10T : Interface pin for the E10T, E8, or E7 emulator
Section 7 ROM	77	The features of the 32-kbyte (4 kbytes of them are the control program area for E7 or E8) flash memory built into the HD64F36024 and HD64F36014 are summarized below.
Section 8 RAM	93	Note: When the E7 or E8 is used, area H'F780 to H'FB7F must not be accessed.

Item	Page	Revision (See Manual for Details)
Table 18.10 DC Characteristics (1)	270	

Item	Symbol	Applicable Pins	Test Condition	Values Min
Input high voltage	V_{IH}	PB3 to PB0	V_{CC} = 4.0 V to 5.5 V	V_{CC} × 0.7
				V_{CC} × 0.8
Input low voltage	V_{IL}	RXD, RXD_2, RXD_3*[1], P12 to P10, P17 to P14, : PB3 to PB0	V_{CC} = 4.0 V to 5.5 V	–0.3

Table 18.10 DC Characteristics (1)	273	

Mode	$\overline{RES}$ Pin	Internal State
Active mode 1	V_{CC}	Operates
Active mode 2		Operates (φOSC/64)
Sleep mode 1	V_{CC}	Only timers operate
Sleep mode 2		Only timers operate (φOSC/64)

Appendix D Package Dimensions Figure D.1 FP-64E Package Dimensions	343	Swapped with new one.
Figure D.2 FP-48F Package Dimensions	344	Swapped with new one.
Figure D.3 FP-48B Package Dimensions	345	Swapped with new one.
Figure D.4 TNP-48 Package Dimensions	346	Swapped with new one.