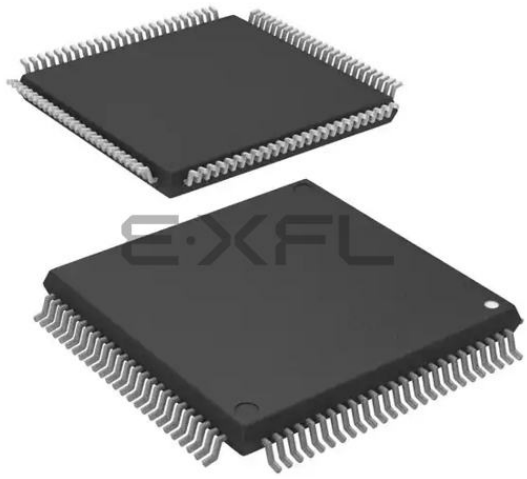
Renesas Electronics America Inc - M30620FCPGP#U7C Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	I²C, IEBus, UART/USART
Peripherals	DMA, WDT
Number of I/O	85
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30620fcpgp-u7c

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Table 1.9 Product Code of Flash Memory version for M16C/62PT

		Product Code	Package	Internal ROM (User ROM Area Without Block A, Block 1)		Internal ROM (Block A, Block 1)		Operating Ambient Temperature
				Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
Flash memory Version	T Version	B	Lead-included	100	0°C to 60°C	100	0°C to 60°C	-40°C to 85°C
	V Version							-40°C to 125°C
	T Version	B7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
	V Version						-40°C to 125°C	-40°C to 125°C
	T Version	U	Lead-free	100		100	0°C to 60°C	-40°C to 85°C
	V Version							-40°C to 125°C
	T Version	U7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
	V Version						-40°C to 125°C	-40°C to 125°C

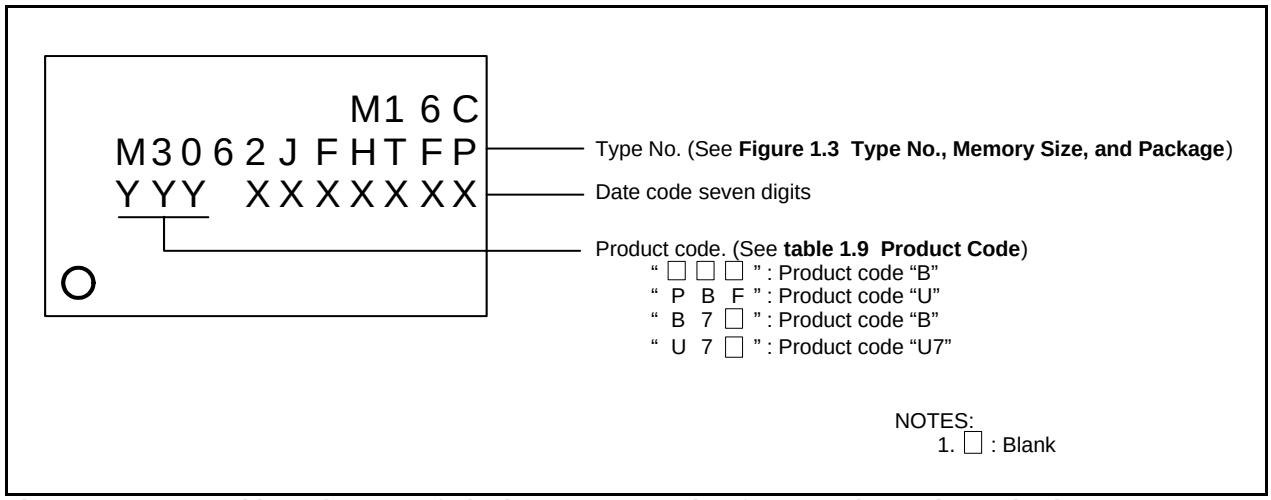


Figure 1.5 Marking Diagram of Flash Memory version for M16C/62PT (Top View)

Table 1.15 Pin Characteristics for 80-Pin Package (1)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
1		P9_5			CLK4	ANEX0	
2		P9_4		TB4IN		DA1	
3		P9_3		TB3IN		DA0	
4		P9_2		TB2IN	SOUT3		
5		P9_0		TB0IN	CLK3		
6	CNVSS (BYTE)						
7	XCIN	P8_7					
8	XCOUT	P8_6					
9	$\overline{\text{RESET}}$						
10	XOUT						
11	VSS						
12	XIN						
13	VCC1						
14		P8_5	$\overline{\text{NMI}}$				
15		P8_4	$\overline{\text{INT2}}$	ZP			
16		P8_3	$\overline{\text{INT1}}$				
17		P8_2	$\overline{\text{INT0}}$				
18		P8_1		TA4IN			
19		P8_0		TA4OUT			
20		P7_7		TA3IN			
21		P7_6		TA3OUT			
22		P7_1		TA0IN/TB5IN	RXD2/SCL2		
23		P7_0		TA0OUT	TXD2/SDA2		
24		P6_7			TXD1/SDA1		
25		P6_6			RXD1/SCL1		
26		P6_5			CLK1		
27		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/CLKS1		
28		P6_3			TXD0/SDA0		
29		P6_2			RXD0/SCL0		
30		P6_1			CLK0		
31		P6_0			$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$		
32		P5_7					CLKOUT
33		P5_6					
34		P5_5					
35		P5_4					
36		P5_3					
37		P5_2					
38		P5_1					
39		P5_0					
40		P4_3					
41		P4_2					
42		P4_1					
43		P4_0					
44		P3_7					
45		P3_6					
46		P3_5					
47		P3_4					
48		P3_3					
49		P3_2					
50		P3_1					

1.6 Pin Description

Table 1.17 Pin Description (100-pin and 128-pin Version) (1)

Signal Name	Pin Name	I/O Type	Power Supply(3)	Description
Power supply input	VCC1,VCC2 VSS	I	–	Apply 2.7 to 5.5 V to the VCC1 and VCC2 pins and 0 V to the VSS pin. The VCC apply condition is that VCC1 ≥ VCC2. (1, 2)
Analog power supply input	AVCC AVSS	I	VCC1	Applies the power supply for the A/D converter. Connect the AVCC pin to VCC1. Connect the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	VCC1	The microcomputer is in a reset state when applying “L” to the this pin.
CNVSS	CNVSS	I	VCC1	Switches processor mode. Connect this pin to VSS to when after a reset to start up in single-chip mode. Connect this pin to VCC1 to start up in microprocessor mode.
External data bus width select input	BYTE	I	VCC1	Switches the data bus in external memory space. The data bus is 16 bits long when the this pin is held "L" and 8 bits long when the this pin is held "H". Set it to either one. Connect this pin to VSS when an single-chip mode.
Bus control pins (4)	D0 to D7	I/O	VCC2	Inputs and outputs data (D0 to D7) when these pins are set as the separate bus.
	D8 to D15	I/O	VCC2	Inputs and outputs data (D8 to D15) when external 16-bit data bus is set as the separate bus.
	A0 to A19	O	VCC2	Output address bits (A0 to A19).
	A0/D0 to A7/D7	I/O	VCC2	Input and output data (D0 to D7) and output address bits (A0 to A7) by timesharing when external 8-bit data bus are set as the multiplexed bus.
	A1/D0 to A8/D7	I/O	VCC2	Input and output data (D0 to D7) and output address bits (A1 to A8) by timesharing when external 16-bit data bus are set as the multiplexed bus.
	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	VCC2	Output $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ signals. $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ are chip-select signals to specify an external space.
	$\overline{\text{WRL}}$/$\overline{\text{WR}}$ $\overline{\text{WRH}}$/$\overline{\text{BHE}}$ $\overline{\text{RD}}$	O	VCC2	Output $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, ($\overline{\text{WR}}$, $\overline{\text{BHE}}$), $\overline{\text{RD}}$ signals. $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ or $\overline{\text{BHE}}$ and $\overline{\text{WR}}$ can be switched by program. • $\overline{\text{WRL}}$, $\overline{\text{WRH}}$ and $\overline{\text{RD}}$ are selected The $\overline{\text{WRL}}$ signal becomes "L" by writing data to an even address in an external memory space. The $\overline{\text{WRH}}$ signal becomes "L" by writing data to an odd address in an external memory space. The $\overline{\text{RD}}$ pin signal becomes "L" by reading data in an external memory space. • $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ are selected The $\overline{\text{WR}}$ signal becomes "L" by writing data in an external memory space. The $\overline{\text{RD}}$ signal becomes "L" by reading data in an external memory space. The $\overline{\text{BHE}}$ signal becomes "L" by accessing an odd address. Select $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ for an external 8-bit data bus.
	ALE	O	VCC2	ALE is a signal to latch the address.
	$\overline{\text{HOLD}}$	I	VCC2	While the $\overline{\text{HOLD}}$ pin is held "L", the microcomputer is placed in a hold state.
	$\overline{\text{HLDA}}$	O	VCC2	In a hold state, $\overline{\text{HLDA}}$ outputs a "L" signal.
	$\overline{\text{RDY}}$	I	VCC2	While applying a "L" signal to the $\overline{\text{RDY}}$ pin, the microcomputer is placed in a wait state.

I : Input O : Output I/O : Input and output

Power Supply : Power supplies which relate to the external bus pins are separated as VCC2, thus they can be interfaced using the different voltage as VCC1.

NOTES:

1. In this manual, hereafter, VCC refers to VCC1 unless otherwise noted.
2. In M16C/62PT, apply 4.0 to 5.5 V to the VCC1 and VCC2 pins. Also the apply condition is that VCC1 = VCC2.
3. When use VCC1 > VCC2, contacts due to some points or restrictions to be checked.
4. Bus control pins in M16C/62PT cannot be used.

Table 1.18 Pin Description (100-pin and 128-pin Version) (2)

Signal Name	Pin Name	I/O Type	Power Supply(1)	Description
Main clock input	XIN	I	VCC1	I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT (3). To use the external clock, input the clock from XIN and leave XOUT open.
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT (3). To use the external clock, input the clock from XCIN and leave XCOUT open.
Sub clock output	XCOUT	O	VCC1	
BCLK output (2)	BCLK	O	VCC2	Outputs the BCLK signal.
Clock output	CLKOUT	O	VCC2	The clock of the same cycle as fC, f8, or f32 is outputted.
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT2}}$	I	VCC1	Input pins for the $\overline{\text{INT}}$ interrupt.
	$\overline{\text{NT3}}$ to $\overline{\text{INT5}}$	I	VCC2	
$\overline{\text{NMI}}$ interrupt input	$\overline{\text{NMI}}$	I	VCC1	Input pin for the $\overline{\text{NMI}}$ interrupt. Pin states can be read by the P8_5 bit in the P8 register.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	VCC1	Input pins for the key input interrupt.
Timer A	TA0OUT to TA4OUT	I/O	VCC1	These are timer A0 to timer A4 I/O pins. (however, output of TA0OUT for the N-channel open drain output.)
	TA0IN to TA4IN	I	VCC1	These are timer A0 to timer A4 input pins.
	ZP	I	VCC1	Input pin for the Z-phase.
Timer B	TB0IN to TB5IN	I	VCC1	These are timer B0 to timer B5 input pins.
Three-phase motor control output	U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$	O	VCC1	These are Three-phase motor control output pins.
Serial interface	$\overline{\text{CTS0}}$ to $\overline{\text{CTS2}}$	I	VCC1	These are send control input pins.
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS2}}$	O	VCC1	These are receive control output pins.
	CLK0 to CLK4	I/O	VCC1	These are transfer clock I/O pins.
	RXD0 to RXD2	I	VCC1	These are serial data input pins.
	SIN3, SIN4	I	VCC1	These are serial data input pins.
	TXD0 to TXD2	O	VCC1	These are serial data output pins. (however, output of TXD2 for the N-channel open drain output.)
	SOUT3, SOUT4	O	VCC1	These are serial data output pins.
	CLKS1	O	VCC1	This is output pin for transfer clock output from multiple pins function.
I^2C mode	SDA0 to SDA2	I/O	VCC1	These are serial data I/O pins. (however, output of SDA2 for the N-channel open drain output.)
	SCL0 to SCL2	I/O	VCC1	These are transfer clock I/O pins. (however, output of SCL2 for the N-channel open drain output.)

I : Input O : Output I/O : Input and output

NOTES:
1. When use VCC1 > VCC2, contacts due to some points or restrictions to be checked.
2. This pin function in M16C/62PT cannot be used.
3. Ask the oscillator maker the oscillation characteristic.

4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.6 list the SFR information.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0 (2)	PM0	00000000b(CNVSS pin is "L") 00000011b(CNVSS pin is "H")
0005h	Processor Mode Register 1	PM1	00001000b
0006h	System Clock Control Register 0	CM0	01001000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Chip Select Control Register (6)	CSR	00000001b
0009h	Address Match Interrupt Enable Register	AIER	XXXXXX00b
000Ah	Protect Register	PRCR	XX000000b
000Bh	Data Bank Register (6)	DBR	00h
000Ch	Oscillation Stop Detection Register (3)	CM2	0X000000b
000Dh			
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00XXXXXXb (4)
0010h 0011h 0012h	Address Match Interrupt Register 0	RMAD0	00h 00h X0h
0013h			
0014h 0015h 0016h	Address Match Interrupt Register 1	RMAD1	00h 00h X0h
0017h			
0018h			
0019h	Voltage Detection Register 1 (5, 6)	VCR1	00001000b
001Ah	Voltage Detection Register 2 (5, 6)	VCR2	00h
001Bh	Chip Select Expansion Control Register (6)	CSE	00h
001Ch	PLL Control Register 0	PLC0	0001X010b
001Dh			
001Eh	Processor Mode Register 2	PM2	XXX00000b
001Fh	Low Voltage Detection Interrupt Register (6)	D4INT	00h
0020h 0021h 0022h	DMA0 Source Pointer	SAR0	XXh XXh XXh
0023h			
0024h 0025h 0026h	DMA0 Destination Pointer	DAR0	XXh XXh XXh
0027h			
0028h 0029h	DMA0 Transfer Counter	TCR0	XXh XXh
002Ah			
002Bh			
002Ch	DMA0 Control Register	DM0CON	00000X00b
002Dh			
002Eh			
002Fh			
0030h 0031h 0032h	DMA1 Source Pointer	SAR1	XXh XXh XXh
0033h			
0034h 0035h 0036h	DMA1 Destination Pointer	DAR1	XXh XXh XXh
0037h			
0038h 0039h	DMA1 Transfer Counter	TCR1	XXh XXh
003Ah			
003Bh			
003Ch	DMA1 Control Register	DM1CON	00000X00b
003Dh			
003Eh			
003Fh			

NOTES:
1. The blank areas are reserved and cannot be accessed by users.
2. The PM00 and PM01 bits do not change at software reset, watchdog timer reset and oscillation stop detection reset.
3. The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.
4. The WDC5 bit is "0" (cold start) immediately after power-on. I t can only be set to "1" in a program.
5. This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.
6. This register in M16C/62PT cannot be used.

X : Nothing is mapped to this bit

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After Reset
03C0h 03C1h	A/D Register 0	AD0	XXh XXh
03C2h 03C3h	A/D Register 1	AD1	XXh XXh
03C4h 03C5h	A/D Register 2	AD2	XXh XXh
03C6h 03C7h	A/D Register 3	AD3	XXh XXh
03C8h 03C9h	A/D Register 4	AD4	XXh XXh
03CAh 03CBh	A/D Register 5	AD5	XXh XXh
03CCh 03CDh	A/D Register 6	AD6	XXh XXh
03CEh 03CFh	A/D Register 7	AD7	XXh XXh
03D0h			
03D1h			
03D2h			
03D3h			
03D4h	A/D Control Register 2	ADCON2	00h
03D5h			
03D6h	A/D Control Register 0	ADCON0	00000XXXb
03D7h	A/D Control Register 1	ADCON1	00h
03D8h	D/A Register 0	DA0	00h
03D9h			
03DAh	D/A Register 1	DA1	00h
03DBh			
03DCh	D/A Control Register	DACON	00h
03DDh			
03DEh	Port P14 Control Register (3)	PC14	XX00XXXXb
03DFh	Pull-Up Control Register 3 (3)	PUR3	00h
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00X00000b
03F3h	Port P9 Direction Register	PD9	00h
03F4h	Port P10 Register	P10	XXh
03F5h	Port P11 Register (3)	P11	XXh
03F6h	Port P10 Direction Register	PD10	00h
03F7h	Port P11 Direction Register (3)	PD11	00h
03F8h	Port P12 Register (3)	P12	XXh
03F9h	Port P13 Register (3)	P13	XXh
03FAh	Port P12 Direction Register (3)	PD12	00h
03FBh	Port P13 Direction Register (3)	PD13	00h
03FCh	Pull-Up Control Register 0	PUR0	00h
03FDh	Pull-Up Control Register 1	PUR1	00000000b (2) 00000010b (2)
03FEh	Pull-Up Control Register 2	PUR2	00h
03FFh	Port Control Register	PCR	00h

NOTES:
1. The blank areas are reserved and cannot be accessed by users.
2. At hardware reset 1 or hardware reset 2, the register is as follows:
   - "00000000b" where "L" is inputted to the CNVSS pin
   - "00000010b" where "H" is inputted to the CNVSS pin

   At software reset, watchdog timer reset and oscillation stop detection reset, the register is as follows:
   - "00000000b" where the PM01 to PM00 bits in the PM0 register are "00b" (single-chip mode).
   - "00000010b" where the PM01 to PM00 bits in the PM0 register are "01b" (memory expansion mode) or "11b" (microprocessor mode).
3. These registers do not exist in M16C/62P (80-pin version), and M16C/62PT (80-pin version).

X : Nothing is mapped to this bit

5. Electrical Characteristics

5.1 Electrical Characteristics (M16C/62P)

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC1}, V_{CC2}	Supply Voltage		V_{CC1}=AVcc	–0.3 to 6.5	V
V_{CC2}	Supply Voltage		V_{CC2}	–0.3 to V_{CC1}+0.1	V
AVcc	Analog Supply Voltage		V_{CC1}=AVcc	–0.3 to 6.5	V
V_I	Input Voltage	$\overline{\text{RESET}}$, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, VREF, XIN		–0.3 to V_{CC1}+0.3 (1)	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		–0.3 to V_{CC2}+0.3 (1)	V
		P7_0, P7_1		–0.3 to 6.5	V
V_O	Output Voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XOUT		–0.3 to V_{CC1}+0.3 (1)	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		–0.3 to V_{CC2}+0.3 (1)	V
		P7_0, P7_1		–0.3 to 6.5	V
P_d	Power Dissipation		–40°C<T_{opr}≤85°C	300	mW
T_{opr}	Operating Ambient Temperature	When the Microcomputer is Operating		–20 to 85 / –40 to 85	°C
		Flash Program Erase		0 to 60	
T_{stg}	Storage Temperature			–65 to 150	°C

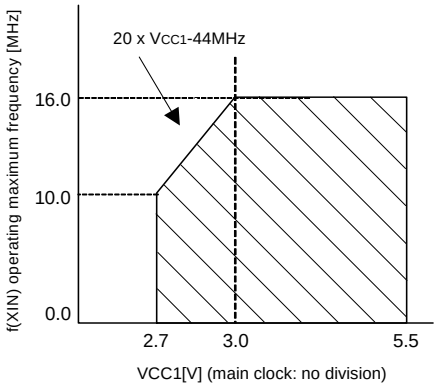
NOTES:
1. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

Table 5.3 Recommended Operating Conditions (2) (1)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
f(XIN)	Main Clock Input Oscillation Frequency (2)	V_{CC1}=3.0V to 5.5V	0		16	MHz
		V_{CC1}=2.7V to 3.0V	0		$20\times V_{CC1}-44$	MHz
f(XCIN)	Sub-Clock Oscillation Frequency			32.768	50	kHz
f(Ring)	On-chip Oscillation Frequency		0.5	1	2	MHz
f(PLL)	PLL Clock Oscillation Frequency (2)	V_{CC1}=3.0V to 5.5V	10		24	MHz
		V_{CC1}=2.7V to 3.0V	10		$46.67\times V_{CC1}-116$	MHz
f(BCLK)	CPU Operation Clock		0		24	MHz
t_{SU}(PLL)	PLL Frequency Synthesizer Stabilization Wait Time	V_{CC1}=5.5V			20	ms
		V_{CC1}=3.0V			50	ms

NOTES:
1. Referenced to V_{CC1} = V_{CC2} = 2.7 to 5.5V at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified.
2. Relationship between main clock oscillation frequency, and supply voltage.

Main clock input oscillation frequency



PLL clock oscillation frequency

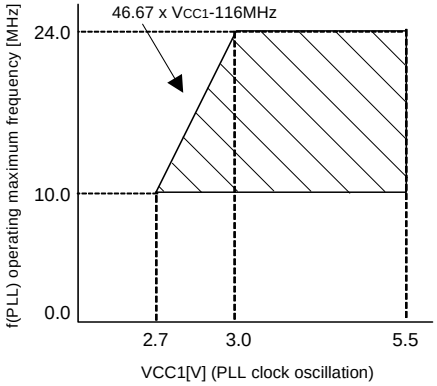


Table 5.4 A/D Conversion Characteristics (1)

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		$V_{REF}=V_{CC1}$				10	Bits
INL	Integral Non-Linearity Error	10bit	$V_{REF}=V_{CC1}=5V$	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±3	LSB
				External operation amp connection mode			±7	LSB
			$V_{REF}=V_{CC1}=3.3V$	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±5	LSB
				External operation amp connection mode			±7	LSB
		8bit	$V_{REF}=V_{CC1}$=5V, 3.3V				±2	LSB
–	Absolute Accuracy	10bit	$V_{REF}=V_{CC1}=5V$	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±3	LSB
				External operation amp connection mode			±7	LSB
			$V_{REF}=V_{CC1}=3.3V$	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input			±5	LSB
				External operation amp connection mode			±7	LSB
		8bit	$V_{REF}=V_{CC1}$=5V, 3.3V				±2	LSB
–	Tolerance Level Impedance					3		kΩ
DNL	Differential Non-Linearity Error						±1	LSB
–	Offset Error						±3	LSB
–	Gain Error						±3	LSB
R_{LADDER}	Ladder Resistance		$V_{REF}=V_{CC1}$		10		40	kΩ
t_{CONV}	10-bit Conversion Time, Sample & Hold Available		$V_{REF}=V_{CC1}$=5V, ϕAD=12MHz		2.75			µs
t_{CONV}	8-bit Conversion Time, Sample & Hold Available		$V_{REF}=V_{CC1}$=5V, ϕAD=12MHz		2.33			µs
t_{SAMP}	Sampling Time				0.25			µs
V_{REF}	Reference Voltage				2.0		V_{CC1}	V
V_{IA}	Analog Input Voltage				0		V_{REF}	V

NOTES:
1. Referenced to $V_{CC1}=AV_{CC}=V_{REF}$=3.3 to 5.5V, $V_{SS}=AV_{SS}$=0V at T_{opr} = −20 to 85°C / −40 to 85°C unless otherwise specified.
2. If $V_{CC1} > V_{CC2}$, do not use AN0_0 to AN0_7 and AN2_0 to AN2_7 as analog input pins.
3. ϕAD frequency must be 12 MHz or less. And divide the fAD if V_{CC1} is less than 4.0V, and ϕAD frequency into 10 MHz or less.
4. When sample & hold is disabled, ϕAD frequency must be 250 kHz or more, in addition to the limitation in Note 3.
   When sample & hold is enabled, ϕAD frequency must be 1MHz or more, in addition to the limitation in Note 3.

$V_{CC1}=V_{CC2}=5V$

Table 5.11 Electrical Characteristics (1) (1)

Symbol	Parameter			Measuring Condition	Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	HIGH Output Voltage (3)	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1		I_{OH}=−5mA	V_{CC1}−2.0		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		I_{OH}=−5mA (2)	V_{CC2}−2.0		V_{CC2}	
V_{OH}	HIGH Output Voltage (3)	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1		I_{OH}=−200μA	V_{CC1}−0.3		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		I_{OH}=−200μA (2)	V_{CC2}−0.3		V_{CC2}	
V_{OH}	HIGH Output Voltage XOUT		HIGHPOWER	I_{OH}=−1mA	V_{CC1}−2.0		V_{CC1}	V
			LOWPOWER	I_{OH}=−0.5mA	V_{CC1}−2.0		V_{CC1}	
	HIGH Output Voltage XCOUT		HIGHPOWER	With no load applied		2.5		V
			LOWPOWER	With no load applied		1.6		
V_{OL}	LOW Output Voltage (3)	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1		I_{OL}=5mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		I_{OL}=5mA (2)			2.0	
V_{OL}	LOW Output Voltage (3)	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1		I_{OL}=200μA			0.45	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		I_{OL}=200μA (2)			0.45	
V_{OL}	LOW Output Voltage XOUT		HIGHPOWER	I_{OL}=1mA			2.0	V
			LOWPOWER	I_{OL}=0.5mA			2.0	
	LOW Output Voltage XCOUT		HIGHPOWER	With no load applied		0		V
			LOWPOWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT5}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, CLK0 to CLK4, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD2, SCL0 to SCL2, SDA0 to SDA2, SIN3, SIN4			0.2		1.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$			0.2		2.5	V
I_{IH}	HIGH Input Current (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE		V_I=5V			5.0	μA
I_{IL}	LOW Input Current (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7,P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, $\overline{RESET}$, CNVSS, BYTE		V_I=0V			−5.0	μA
R_{PULLUP}	Pull-Up Resistance (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7,P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1		V_I=0V	30	50	170	kΩ
R_{fXIN}	Feedback Resistance XIN					1.5		MΩ
R_{fXCIN}	Feedback Resistance XCIN					15		MΩ
V_{RAM}	RAM Retention Voltage			At stop mode	2.0			V

NOTES:
1. Referenced to V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS} = 0V at T_{opr} = −20 to 85°C / −40 to 85°C, f(BCLK)=24MHz unless otherwise specified.
2. Where the product is used at V_{CC1} = 5 V and V_{CC2} = 3 V, refer to the 3 V version value for the pin specified value on V_{CC2} port side.
3. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.

$V_{CC1}=V_{CC2}=5V$

Timing Requirements
(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.13 External Clock Input (XIN input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	62.5		ns
$t_{w(H)}$	External Clock Input HIGH Pulse Width	25		ns
$t_{w(L)}$	External Clock Input LOW Pulse Width	25		ns
t_r	External Clock Rise Time		15	ns
t_f	External Clock Fall Time		15	ns

NOTES:
1. The condition is V_{CC1}=V_{CC2}=3.0 to 5.0V.

Table 5.14 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (for setting with no wait)		(NOTE 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (for setting with wait)		(NOTE 2)	ns
$t_{ac3(RD-DB)}$	Data Input Access Time (when accessing multiplex bus area)		(NOTE 3)	ns
$t_{su(DB-RD)}$	Data Input Setup Time	40		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ Input Setup Time	30		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ Input Setup Time	40		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ Input Hold Time	0		ns

NOTES:
1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 45[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 45[ns]$$ n is ”2” for 1-wait setting, “3” for 2-wait setting and “4” for 3-wait setting.

3. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 45[ns]$$ n is “2” for 2-wait setting, “3” for 3-wait setting.

$V_{CC1}=V_{CC2}=5V$

Timing Requirements
(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.15 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	40		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	40		ns

Table 5.16 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	200		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	200		ns

Table 5.17 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	100		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	100		ns

Table 5.18 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	100		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	100		ns

Table 5.19 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAiOUT Input HIGH Pulse Width	1000		ns
$t_{w(UPL)}$	TAiOUT Input LOW Pulse Width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

Table 5.20 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT Input Setup Time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN Input Setup Time	200		ns

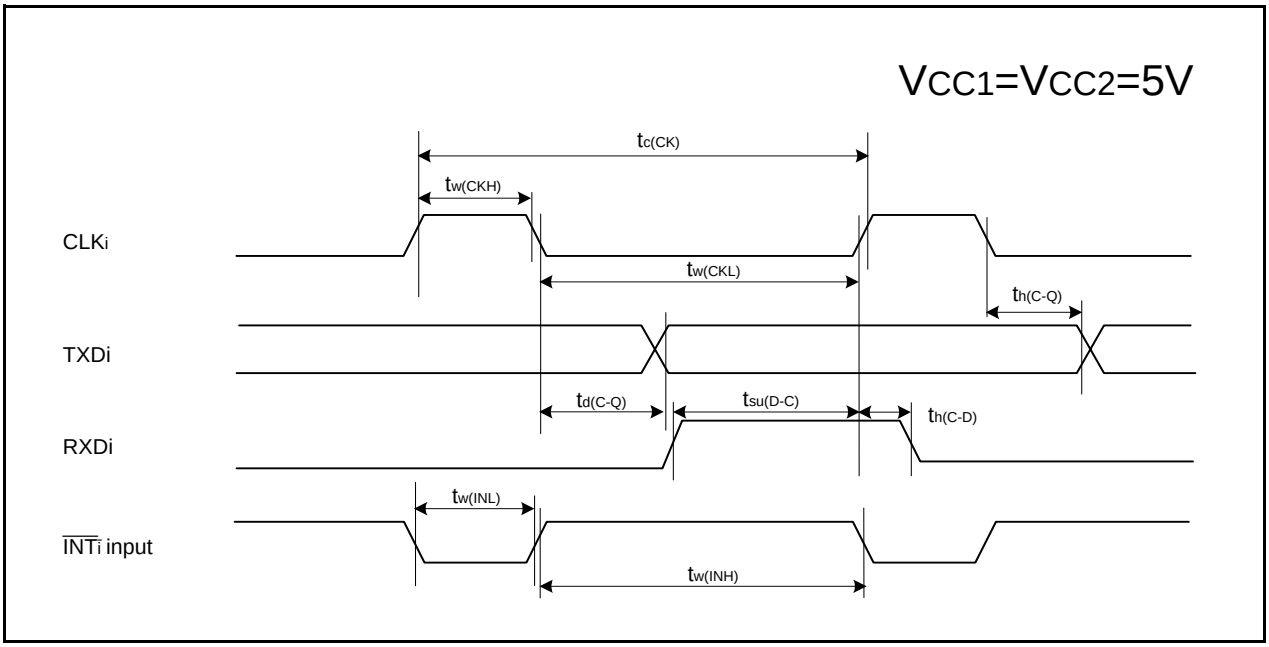
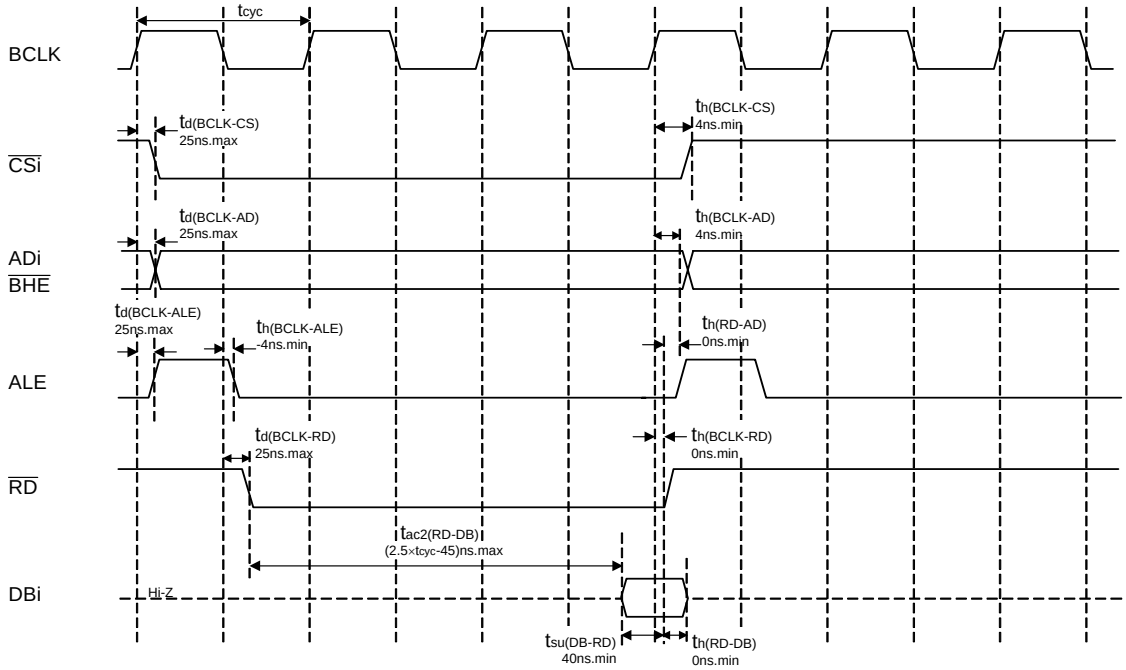


Figure 5.4 Timing Diagram (2)

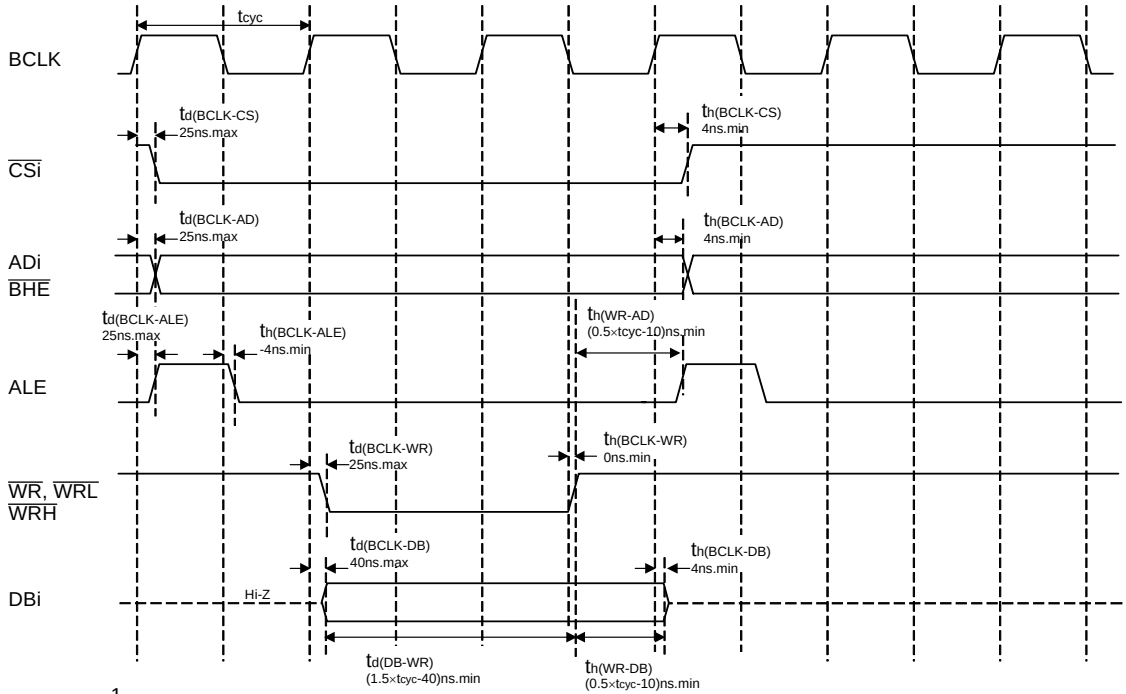
$V_{CC1}=V_{CC2}=5V$

Memory Expansion Mode, Microprocessor Mode
(for 2-wait setting and external area access**)**

Read timing



Write timing



$$T_{cyc}=\frac{1}{f(BCLK)}$$

Measuring conditions
· $V_{CC1}=V_{CC2}=5V$
· Input timing voltage : $V_{IL}=0.8V$, $V_{IH}=2.0V$
· Output timing voltage : $V_{OL}=0.4V$, $V_{OH}=2.4V$

Figure 5.8 Timing Diagram (6)

$V_{CC1}=V_{CC2}=3V$

Timing Requirements
(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at T_{opr} = –20 to 85°C / –40 to 85°C unless otherwise specified)

Table 5.34 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	150		ns
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	60		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	60		ns

Table 5.35 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	600		ns
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	300		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	300		ns

Table 5.36 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	300		ns
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	150		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	150		ns

Table 5.37 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	150		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	150		ns

Table 5.38 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT Input Cycle Time	3000		ns
$t_{w(UPH)}$	TAiOUT Input HIGH Pulse Width	1500		ns
$t_{w(UPL)}$	TAiOUT Input LOW Pulse Width	1500		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	600		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	600		ns

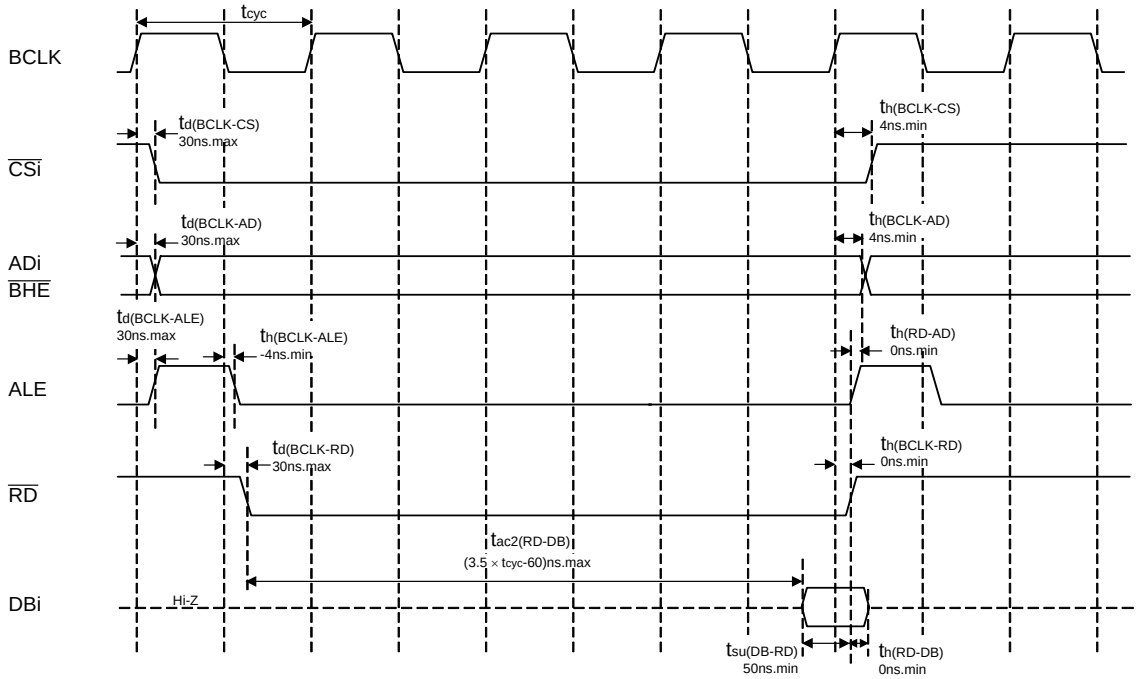
Table 5.39 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	2		µs
$t_{su(TAIN-TAOUT)}$	TAiOUT Input Setup Time	500		ns
$t_{su(TAOUT-TAIN)}$	TAiIN Input Setup Time	500		ns

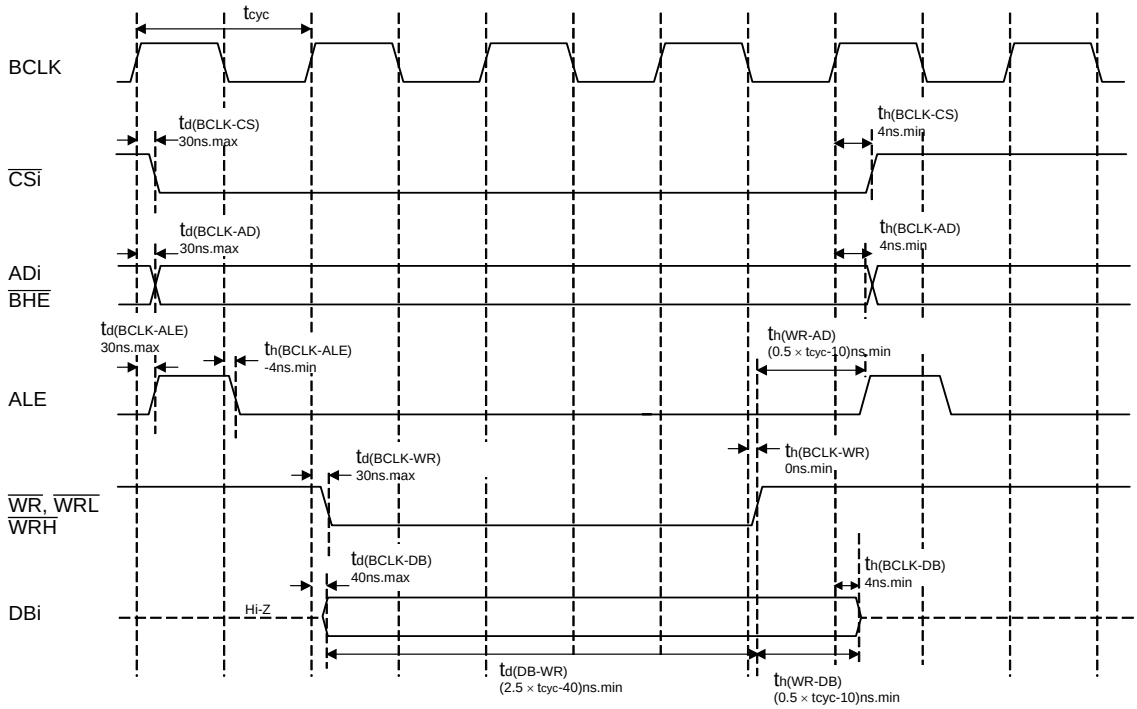
$V_{CC1} = V_{CC2} = 3V$

Memory Expansion Mode, Microprocessor Mode
(for 3-wait setting and external area access**)**

Read timing



Write timing



$$t_{cyc} = \frac{1}{f(BCLK)}$$

Measuring conditions
· V_{CC1}=V_{CC2}=3V
· Input timing voltage : V_{IL}=0.6V, V_{IH}=2.4V
· Output timing voltage : V_{OL}=1.5V, V_{OH}=1.5V

Figure 5.19 Timing Diagram (7)

5.2 Electrical Characteristics (M16C/62PT)

Table 5.49 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC1}, V_{CC2}	Supply Voltage		V_{CC1}=V_{CC2}=AVcc	–0.3 to 6.5	V
AVcc	Analog Supply Voltage		V_{CC1}=V_{CC2}=AVcc	–0.3 to 6.5	V
V_I	Input Voltage	$\overline{\text{RESET}}$, CNVSS, BYTE, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, VREF, XIN		–0.3 to V_{CC1}+0.3 (1)	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		–0.3 to V_{CC2}+0.3 (1)	V
		P7_0, P7_1		–0.3 to 6.5	V
V_O	Output Voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P14_0, P14_1, XOUT		–0.3 to V_{CC1}+0.3 (1)	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P12_0 to P12_7, P13_0 to P13_7		–0.3 to V_{CC2}+0.3 (1)	V
		P7_0, P7_1		–0.3 to 6.5	V
P_d	Power Dissipation		–40°C<T_{opr}≤85°C	300	mW
			85°C<T_{opr}≤125°C	200	
T_{opr}	Operating Ambient Temperature	When the Microcomputer is Operating		–40 to 85 / –40 to 125 (2)	°C
		Flash Program Erase		0 to 60	
T_{stg}	Storage Temperature			–65 to 150	°C

NOTES:
1. There is no external connections for port P1_0 to P1_7, P4_4 to P4_7, P7_2 to P7_5 and P9_1 in 80-pin version.
2. T version = –40 to 85 °C, V version= –40 to 125 °C.

V_{CC1}=V_{CC2}=5V

Timing Requirements
(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –40 to 85°C (T version) / –40 to 125°C (V version) unless otherwise specified)

Table 5.60 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	40		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	40		ns

Table 5.61 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	200		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	200		ns

Table 5.62 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	100		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	100		ns

Table 5.63 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	100		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	100		ns

Table 5.64 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAiOUT Input HIGH Pulse Width	1000		ns
$t_{w(UPL)}$	TAiOUT Input LOW Pulse Width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

Table 5.65 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT Input Setup Time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN Input Setup Time	200		ns

V_{CC1}=V_{CC2}=5V

Timing Requirements
(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at T_{opr} = –40 to 85°C (T version) / –40 to 125°C (V version) unless otherwise specified)

Table 5.66 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on both edges)	80		ns

Table 5.67 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	200		ns

Table 5.68 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	200		ns

Table 5.69 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{\text{ADTRG}}$ Input Cycle Time	1000		ns
$t_{w(ADL)}$	$\overline{\text{ADTRG}}$ input LOW Pulse Width	125		ns

Table 5.70 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input HIGH Pulse Width	100		ns
$t_{w(CKL)}$	CLKi Input LOW Pulse Width	100		ns
$t_{d(C-Q)}$	TXDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TXDi Hold Time	0		ns
$t_{su(D-C)}$	RXDi Input Setup Time	70		ns
$t_{h(C-D)}$	RXDi Input Hold Time	90		ns

Table 5.71 External Interrupt $\overline{\text{INTi}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{\text{INTi}}$ Input HIGH Pulse Width	250		ns
$t_{w(INL)}$	$\overline{\text{INTi}}$ Input LOW Pulse Width	250		ns