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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	M16C/60
Core Size	16-Bit
Speed	24MHz
Connectivity	I ² C, IEBus, UART/USART
Peripherals	DMA, WDT
Number of I/O	50
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30620spfp-u3c

Table 1.2 Performance Outline of M16C/62P Group (M16C/62P, M16C/62PT)(100-pin version)

	Item	Performance	
		M16C/62P	M16C/62PT ⁽⁴⁾
CPU	Number of Basic Instructions	91 instructions	
	Minimum Instruction Execution Time	41.7ns(f(BCLK)=24MHz, VCC1=3.3 to 5.5V) 100ns(f(BCLK)=10MHz, VCC1=2.7 to 5.5V)	41.7ns(f(BCLK)=24MHz, VCC1=4.0 to 5.5V)
	Operating Mode	Single-chip, memory expansion and microprocessor mode	Single-chip
	Address Space	1 Mbyte (Available to 4 Mbytes by memory space expansion function)	1 Mbyte
	Memory Capacity	See Table 1.4 to 1.7 Product List	
Peripheral Function	Port	Input/Output : 87 pins, Input : 1 pin	
	Multifunction Timer	Timer A : 16 bits x 5 channels, Timer B : 16 bits x 6 channels, Three phase motor control circuit	
	Serial Interface	3 channels Clock synchronous, UART, I ² C bus ⁽¹⁾ , IEBus ⁽²⁾ 2 channels Clock synchronous	
	A/D Converter	10-bit A/D converter: 1 circuit, 26 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	2 channels	
	CRC Calculation Circuit	CCITT-CRC	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	Internal: 29 sources, External: 8 sources, Software: 4 sources, Priority level: 7 levels	
	Clock Generation Circuit	4 circuits Main clock generation circuit (*), Subclock generation circuit (*), On-chip oscillator, PLL synthesizer (*)Equipped with a built-in feedback resistor.	
	Oscillation Stop Detection Function	Stop detection of main clock oscillation, re-oscillation detection function	
	Voltage Detection Circuit	Available (option ⁽⁵⁾)	Absent
Electric Characteristics	Supply Voltage	VCC1=3.0 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK)=24MHz) VCC1=2.7 to 5.5 V, VCC2=2.7V to VCC1 (f(BCLK)=10MHz)	VCC1=VCC2=4.0 to 5.5V (f(BCLK)=24MHz)
	Power Consumption	14 mA (VCC1=VCC2=5V, f(BCLK)=24MHz) 8 mA (VCC1=VCC2=3V, f(BCLK)=10MHz) 1.8μA (VCC1=VCC2=3V, f(XCIN)=32kHz, wait mode) 0.7μA (VCC1=VCC2=3V, stop mode)	14 mA (VCC1=VCC2=5V, f(BCLK)=24MHz) 2.0μA (VCC1=VCC2=5V, f(XCIN)=32kHz, wait mode) 0.8μA (VCC1=VCC2=5V, stop mode)
Flash memory version	Program/Erase Supply Voltage	3.3±0.3 V or 5.0±0.5 V	5.0±0.5 V
	Program and Erase Endurance	100 times (all area) or 1,000 times (user ROM area without block A and block 1) / 10,000 times (block A, block 1) ⁽³⁾	
Operating Ambient Temperature		-20 to 85°C, -40 to 85°C ⁽³⁾	T version : -40 to 85°C V version : -40 to 125°C
Package		100-pin plastic mold QFP, LQFP	

NOTES:

1. I²C bus is a registered trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a registered trademark of NEC Electronics Corporation.
3. See **Table 1.8 and 1.9 Product Code** for the program and erase endurance, and operating ambient temperature.
In addition 1,000 times/10,000 times are under development as of Jul., 2005. Please inquire about a release schedule.
4. Use the M16C/62PT on VCC1=VCC2
5. All options are on request basis.

1.5 Pin Configuration

Figures 1.6 to 1.9 show the Pin Configuration (Top View).

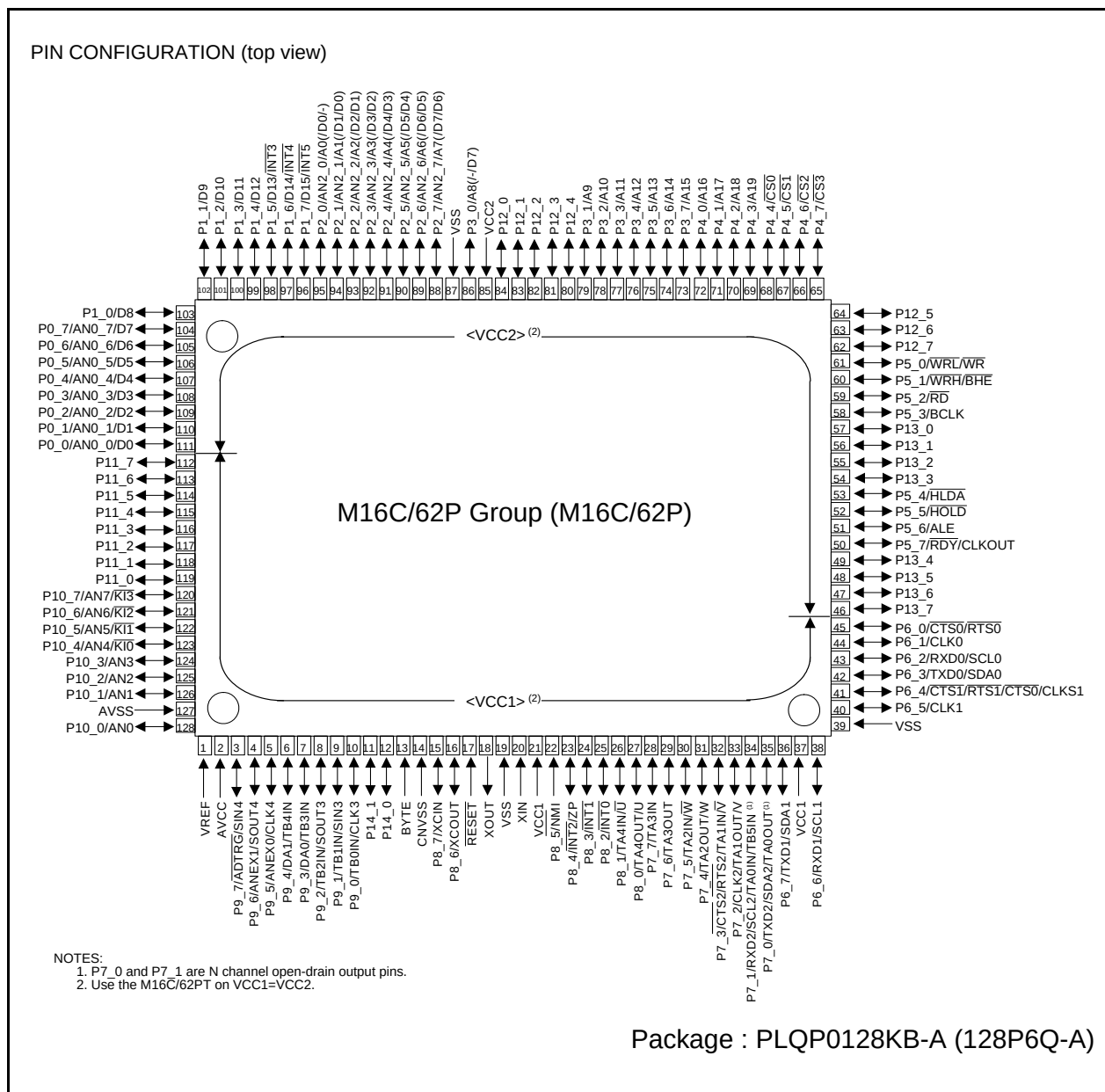


Figure 1.6 Pin Configuration (Top View)

Table 1.11 Pin Characteristics for 128-Pin Package (2)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
51		P5_6					ALE
52		P5_5					$\overline{\text{HOLD}}$
53		P5_4					$\overline{\text{HLDA}}$
54		P13_3					
55		P13_2					
56		P13_1					
57		P13_0					
58		P5_3					BCLK
59		P5_2					$\overline{\text{RD}}$
60		P5_1					$\overline{\text{WRH/BHE}}$
61		P5_0					$\overline{\text{WRL/WR}}$
62		P12_7					
63		P12_6					
64		P12_5					
65		P4_7					$\overline{\text{CS3}}$
66		P4_6					$\overline{\text{CS2}}$
67		P4_5					$\overline{\text{CS1}}$
68		P4_4					$\overline{\text{CS0}}$
69		P4_3					A19
70		P4_2					A18
71		P4_1					A17
72		P4_0					A16
73		P3_7					A15
74		P3_6					A14
75		P3_5					A13
76		P3_4					A12
77		P3_3					A11
78		P3_2					A10
79		P3_1					A9
80		P12_4					
81		P12_3					
82		P12_2					
83		P12_1					
84		P12_0					
85	VCC2						
86		P3_0					A8(/D7)
87	VSS						
88		P2_7				AN2_7	A7(/D7/D6)
89		P2_6				AN2_6	A6(/D6/D5)
90		P2_5				AN2_5	A5(/D5/D4)
91		P2_4				AN2_4	A4(/D4/D3)
92		P2_3				AN2_3	A3(/D3/D2)
93		P2_2				AN2_2	A2(/D2/D1)
94		P2_1				AN2_1	A1(/D1/D0)
95		P2_0				AN2_0	A0(/D0/-)
96		P1_7	$\overline{\text{INT5}}$				D15
97		P1_6	$\overline{\text{INT4}}$				D14
98		P1_5	$\overline{\text{INT3}}$				D13
99		P1_4					D12
100		P1_3					D11

Table 1.12 Pin Characteristics for 128-Pin Package (3)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin	Bus Control Pin
101		P1_2					D10
102		P1_1					D9
103		P1_0					D8
104		P0_7				AN0_7	D7
105		P0_6				AN0_6	D6
106		P0_5				AN0_5	D5
107		P0_4				AN0_4	D4
108		P0_3				AN0_3	D3
109		P0_2				AN0_2	D2
110		P0_1				AN0_1	D1
111		P0_0				AN0_0	D0
112		P11_7					
113		P11_6					
114		P11_5					
115		P11_4					
116		P11_3					
117		P11_2					
118		P11_1					
119		P11_0					
120		P10_7	$\overline{\text{KI3}}$			AN7	
121		P10_6	$\overline{\text{KI2}}$			AN6	
122		P10_5	$\overline{\text{KI1}}$			AN5	
123		P10_4	$\overline{\text{KI0}}$			AN4	
124		P10_3				AN3	
125		P10_2				AN2	
126		P10_1				AN1	
127	AVSS						
128		P10_0				AN0	

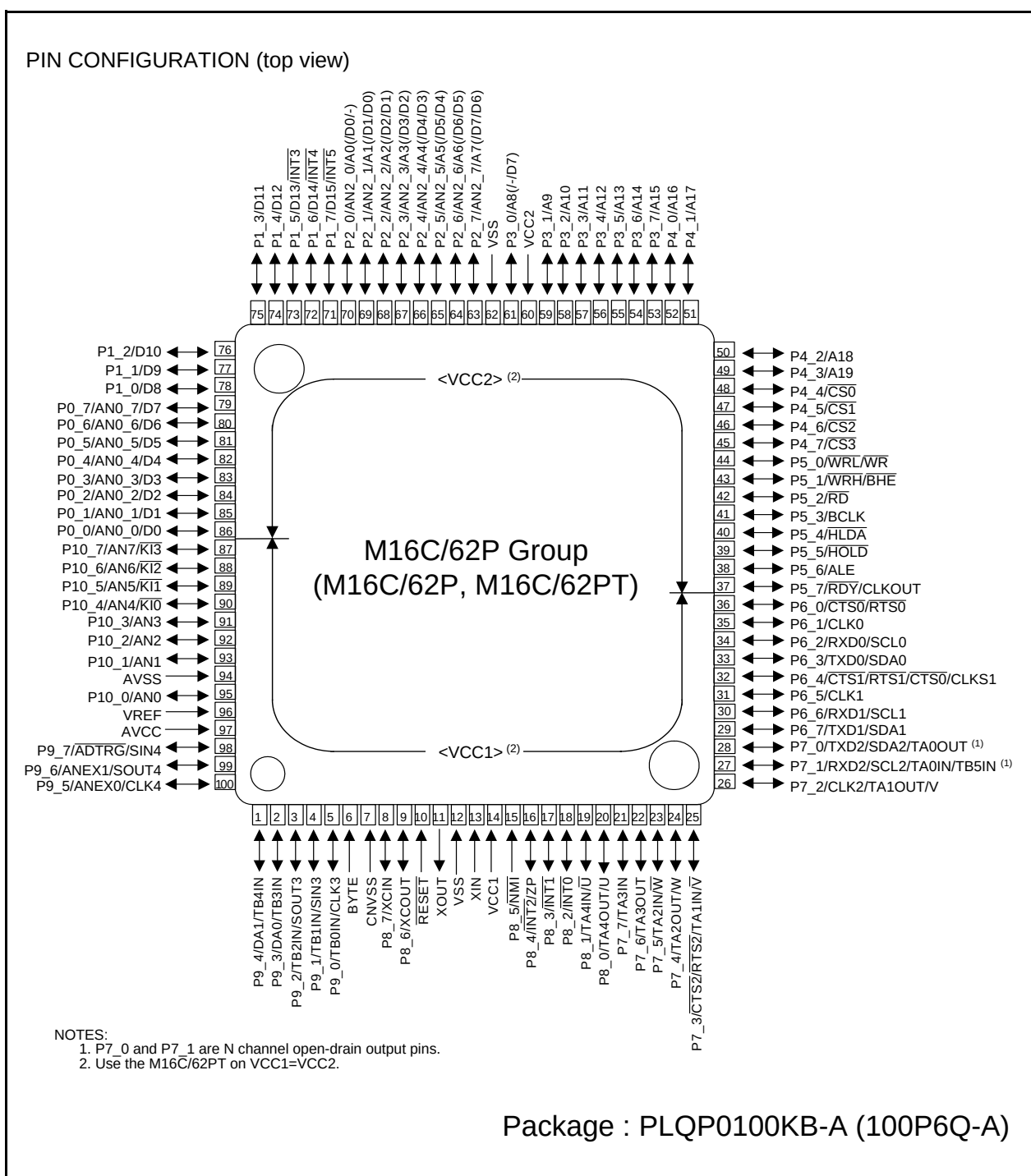


Figure 1.8 Pin Configuration (Top View)

Table 1.20 Pin Description (80-pin Version) (1)

Signal Name	Pin Name	I/O Type	Power Supply	Description
Power supply input	VCC1, VSS	I	–	Apply 2.7 to 5.5 V to the VCC1 pin and 0 V to the VSS pin. (1, 2)
Analog power supply input	AVCC AVSS	I	VCC1	Applies the power supply for the A/D converter. Connect the AVCC pin to VCC1. Connect the AVSS pin to VSS.
Reset input	RESET	I	VCC1	The microcomputer is in a reset state when applying “L” to the this pin.
CNVSS	CNVSS (BYTE)	I	VCC1	Switches processor mode. Connect this pin to VSS to when after a reset to start up in single-chip mode. Connect this pin to VCC1 to start up in microprocessor mode. As for the BYTE pin of the 80-pin versions, pull-up processing is performed within the microcomputer.
Main clock input	XIN	I	VCC1	I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT (3). To use the external clock, input the clock from XIN and leave XOUT open.
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT (3). To use the external clock, input the clock from XCIN and leave XCOUT open.
Sub clock output	XCOUT	O	VCC1	
Clock output	CLKOUT	O	VCC2	The clock of the same cycle as fC, f8, or f32 is outputted.
INT interrupt input	INT0 to INT2	I	VCC1	Input pins for the INT interrupt.
NMI interrupt input	NMI	I	VCC1	Input pin for the NMI interrupt.
Key input interrupt input	KI0 to KI3	I	VCC1	Input pins for the key input interrupt.
Timer A	TA0OUT, TA3OUT, TA4OUT	I/O	VCC1	These are Timer A0, Timer A3 and Timer A4 I/O pins. (however, output of TA0OUT for the N-channel open drain output.)
	TA0IN, TA3IN, TA4IN	I	VCC1	These are Timer A0, Timer A3 and Timer A4 input pins.
	ZP	I	VCC1	Input pin for the Z-phase.
Timer B	TB0IN, TB2IN to TB5IN	I	VCC1	These are Timer B0, Timer B2 to Timer B5 input pins.
Serial interface	CTS0 to CTS1	I	VCC1	These are send control input pins.
	RTS0 to RTS1	O	VCC1	These are receive control output pins.
	CLK0, CLK1, CLK3, CLK4	I/O	VCC1	These are transfer clock I/O pins.
	RXD0 to RXD2	I	VCC1	These are serial data input pins.
	SIN4	I	VCC1	This is serial data input pin.
	TXD0 to TXD2	O	VCC1	These are serial data output pins. (however, output of TXD2 for the N-channel open drain output.)
	SOUT3, SOUT4	O	VCC1	These are serial data output pins.
	CLKS1	O	VCC1	This is output pin for transfer clock output from multiple pins function.
I ² C mode	SDA0 to SDA2	I/O	VCC1	These are serial data I/O pins. (however, output of SDA2 for the N-channel open drain output.)
	SCL0 to SCL2	I/O	VCC1	These are transfer clock I/O pins. (however, output of SCL2 for the N-channel open drain output.)

I : Input O : Output I/O : Input and output

NOTES:

1. In this manual, hereafter, VCC refers to VCC1 unless otherwise noted.
2. In M16C/62PT, apply 4.0 to 5.5 V to the VCC1 pin.
3. Ask the oscillator maker the oscillation characteristic.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

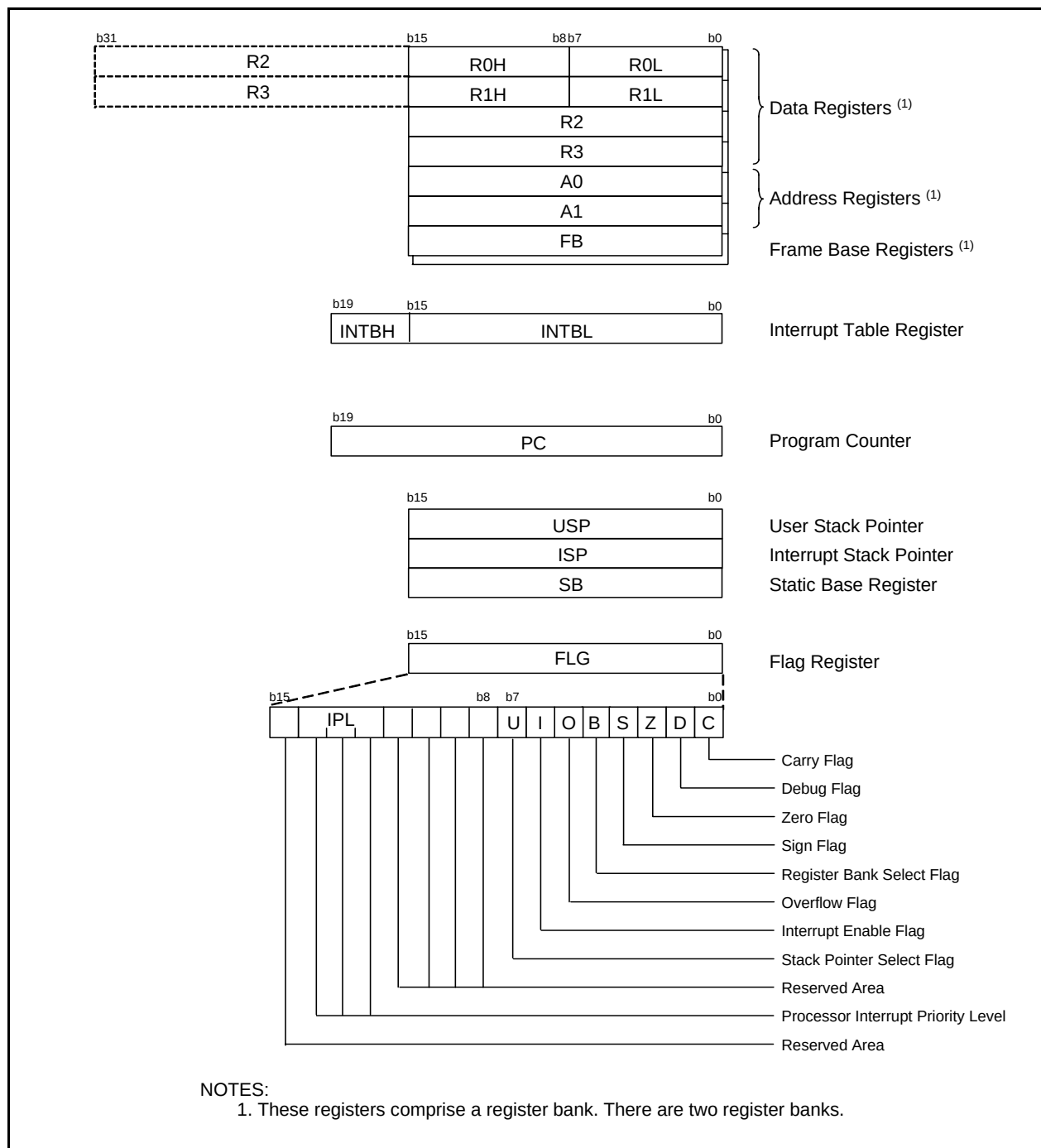


Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers.

R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

Table 4.2 SFR Information (2) ⁽¹⁾

Address	Register	Symbol	After Reset
0040h			
0041h			
0042h			
0043h			
0044h	INT3 Interrupt Control Register	INT3IC	XX00X000b
0045h	Timer B5 Interrupt Control Register	TB5IC	XXXXX000b
0046h	Timer B4 Interrupt Control Register, UART1 BUS Collision Detection Interrupt Control Register	TB4IC, U1BCNIC	XXXXX000b
0047h	Timer B3 Interrupt Control Register, UART0 BUS Collision Detection Interrupt Control Register	TB3IC, U0BCNIC	XXXXX000b
0048h	SI/O4 Interrupt Control Register, INT5 Interrupt Control Register	S4IC, INT5IC	XX00X000b
0049h	SI/O3 Interrupt Control Register, INT4 Interrupt Control Register	S3IC, INT4IC	XX00X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	XXXXX000b
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXXX000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXXX000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXXX000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXXX000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXXX000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXXX000b
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXXX000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXXX000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Fh	INT2 Interrupt Control Register	INT2IC	XX00X000b
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

NOTES:

- The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Table 5.9 Low Voltage Detection Circuit Electrical Characteristics

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det4}	Low Voltage Detection Voltage ⁽¹⁾	V _{CC1} =0.8V to 5.5V	3.3	3.8	4.4	V
V _{det3}	Reset Level Detection Voltage ^(1, 2)		2.2	2.8	3.6	V
V _{det4} -V _{det3}	Electric potential difference of Low Voltage Detection and Reset Level Detection		0.3			V
V _{det3s}	Low Voltage Reset Retention Voltage				0.8	V
V _{det3r}	Low Voltage Reset Release Voltage ⁽³⁾		2.2	2.9	4.0	V

NOTES:

1. V_{det4} > V_{det3}.
2. Where reset level detection voltage is less than 2.7 V, if the supply power voltage is greater than the reset level detection voltage, the microcomputer operates with f(BCLK) ≤ 10MHz.
3. V_{det3r} > V_{det3} is not guaranteed.
4. The voltage detection circuit is designed to use when V_{CC1} is set to 5V.

Table 5.10 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
t _d (P-R)	Time for Internal Power Supply Stabilization During Powering-On	V _{CC1} =2.7V to 5.5V			2	ms
t _d (R-S)	STOP Release Time				150	μs
t _d (W-S)	Low Power Dissipation Mode Wait Mode Release Time				150	μs
t _d (S-R)	Brown-out Detection Reset (Hardware Reset 2) Release Wait Time	V _{CC1} =V _{det3r} to 5.5V		6 ⁽¹⁾	20	ms
t _d (E-A)	Low Voltage Detection Circuit Operation Start Time	V _{CC1} =2.7V to 5.5V			20	μs

NOTES:

1. When V_{CC1} = 5V.

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.15 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	40		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	40		ns

Table 5.16 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	200		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	200		ns

Table 5.17 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	100		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	100		ns

Table 5.18 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN Input HIGH Pulse Width	100		ns
$t_{w(TAL)}$	TAiIN Input LOW Pulse Width	100		ns

Table 5.19 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAiOUT Input HIGH Pulse Width	1000		ns
$t_{w(UPL)}$	TAiOUT Input LOW Pulse Width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

Table 5.20 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT Input Setup Time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN Input Setup Time	200		ns

$$V_{CC1}=V_{CC2}=5V$$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.28 Memory Expansion and Microprocessor Modes (for 1- to 3-wait setting and external area access)

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_d(BCLK-AD)$	Address Output Delay Time	See Figure 5.2		25	ns
$t_h(BCLK-AD)$	Address Output Hold Time (in relation to BCLK)		4		ns
$t_h(RD-AD)$	Address Output Hold Time (in relation to RD)		0		ns
$t_h(WR-AD)$	Address Output Hold Time (in relation to WR)		(NOTE 2)		ns
$t_d(BCLK-CS)$	Chip Select Output Delay Time			25	ns
$t_h(BCLK-CS)$	Chip Select Output Hold Time (in relation to BCLK)		4		ns
$t_d(BCLK-ALE)$	ALE Signal Output Delay Time			15	ns
$t_h(BCLK-ALE)$	ALE Signal Output Hold Time		-4		ns
$t_d(BCLK-RD)$	RD Signal Output Delay Time			25	ns
$t_h(BCLK-RD)$	RD Signal Output Hold Time		0		ns
$t_d(BCLK-WR)$	WR Signal Output Delay Time			25	ns
$t_h(BCLK-WR)$	WR Signal Output Hold Time		0		ns
$t_d(BCLK-DB)$	Data Output Delay Time (in relation to BCLK)			40	ns
$t_h(BCLK-DB)$	Data Output Hold Time (in relation to BCLK) ⁽³⁾		4		ns
$t_d(DB-WR)$	Data Output Delay Time (in relation to WR)		(NOTE 1)		ns
$t_h(WR-DB)$	Data Output Hold Time (in relation to WR) ⁽³⁾		(NOTE 2)		ns
$t_d(BCLK-HLDA)$	HLDA Output Delay Time			40	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 40[ns]$$

n is "1" for 1-wait setting, "2" for 2-wait setting and "3" for 3-wait setting.
(BCLK) is 12.5MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10[ns]$$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.

Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

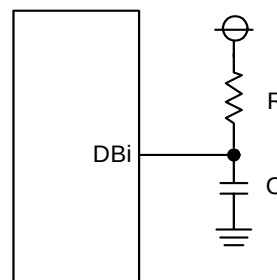
$$t = -CR \times \ln(1 - V_{OL} / V_{CC2})$$

by a circuit of the right figure.

For example, when $V_{OL} = 0.2V_{CC2}$, $C = 30pF$, $R = 1k\Omega$, hold time of output "L" level is

$$t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2})$$

$$= 6.7ns.$$



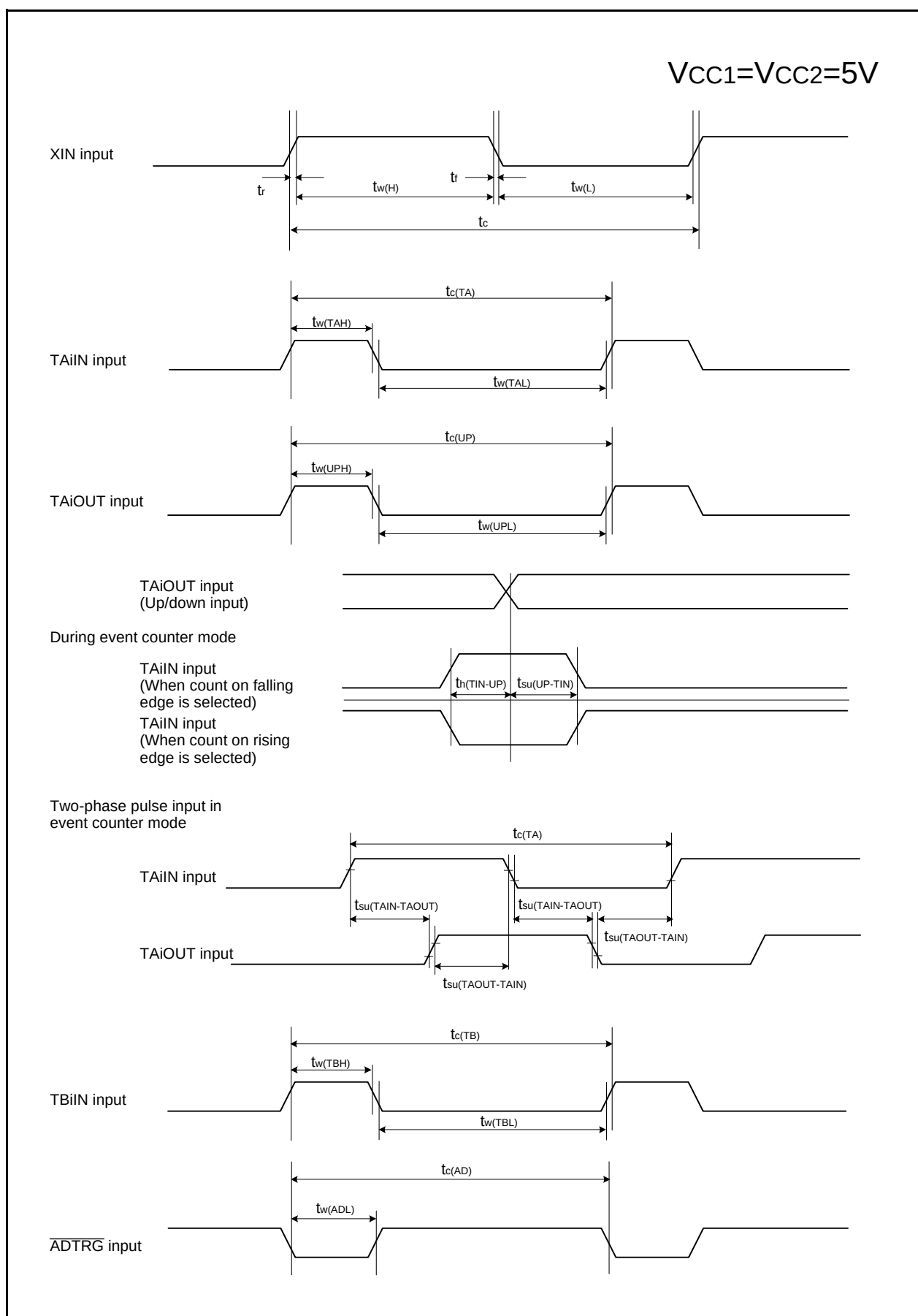


Figure 5.3 Timing Diagram (1)

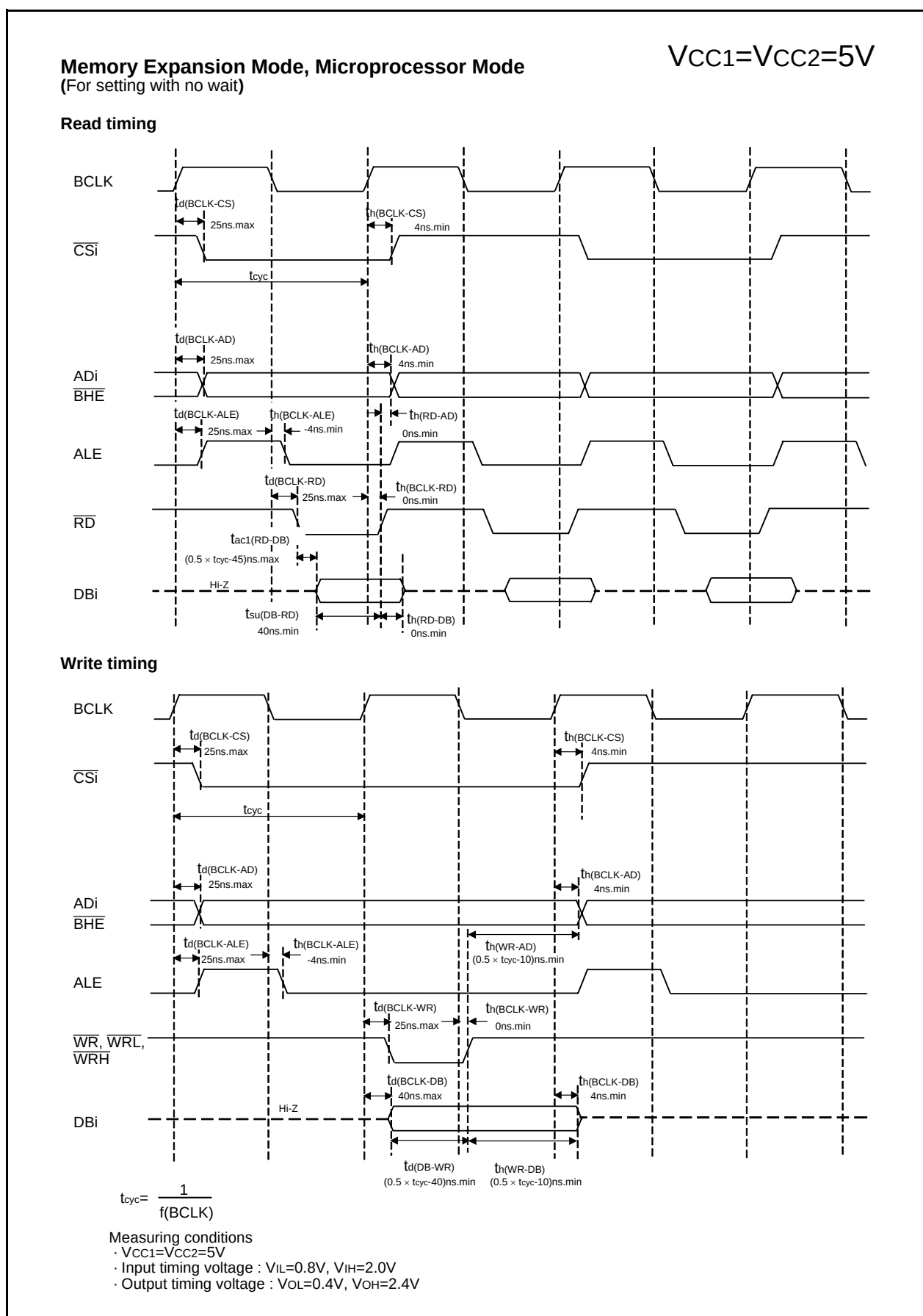


Figure 5.6 Timing Diagram (4)

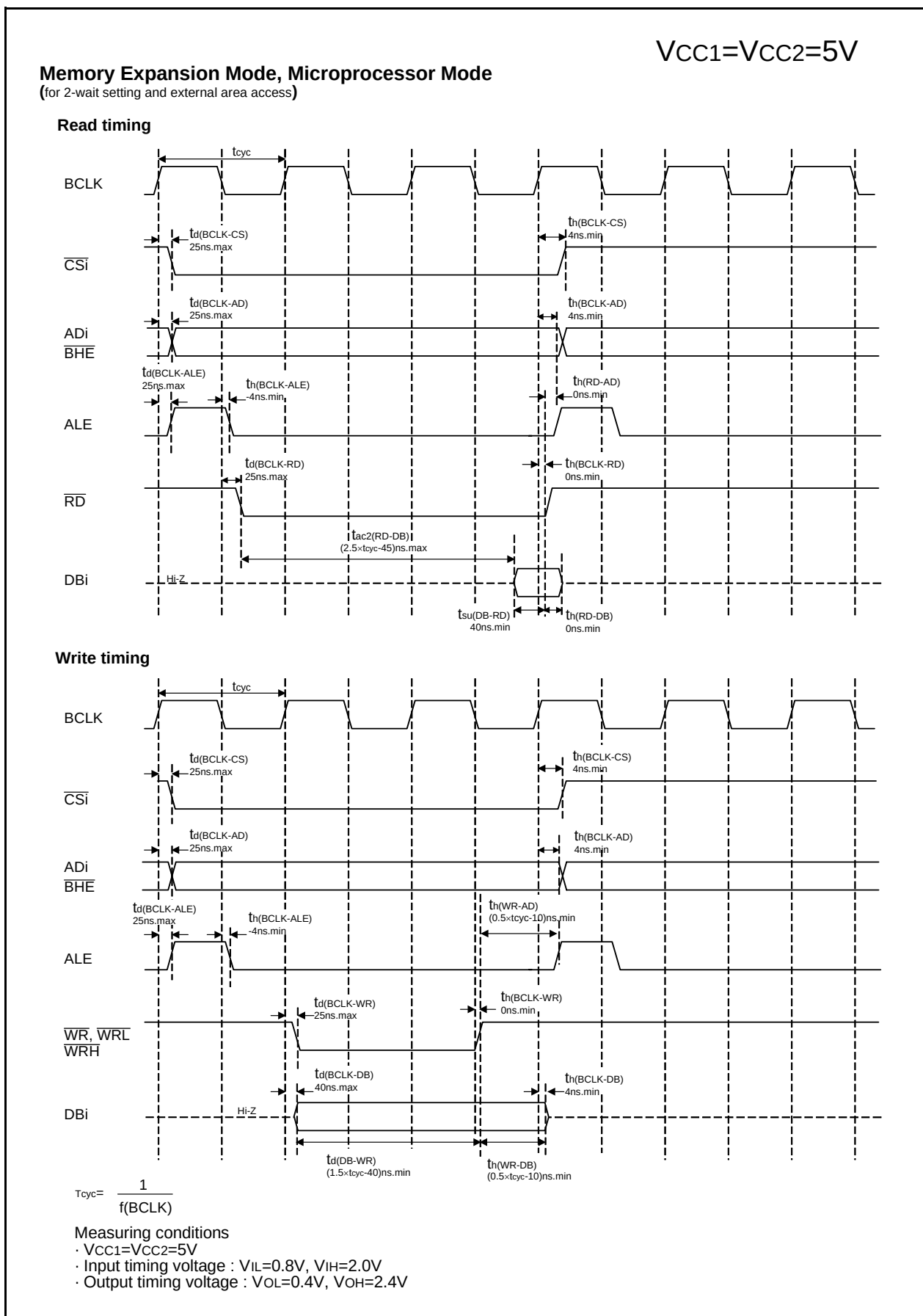


Figure 5.8 Timing Diagram (6)

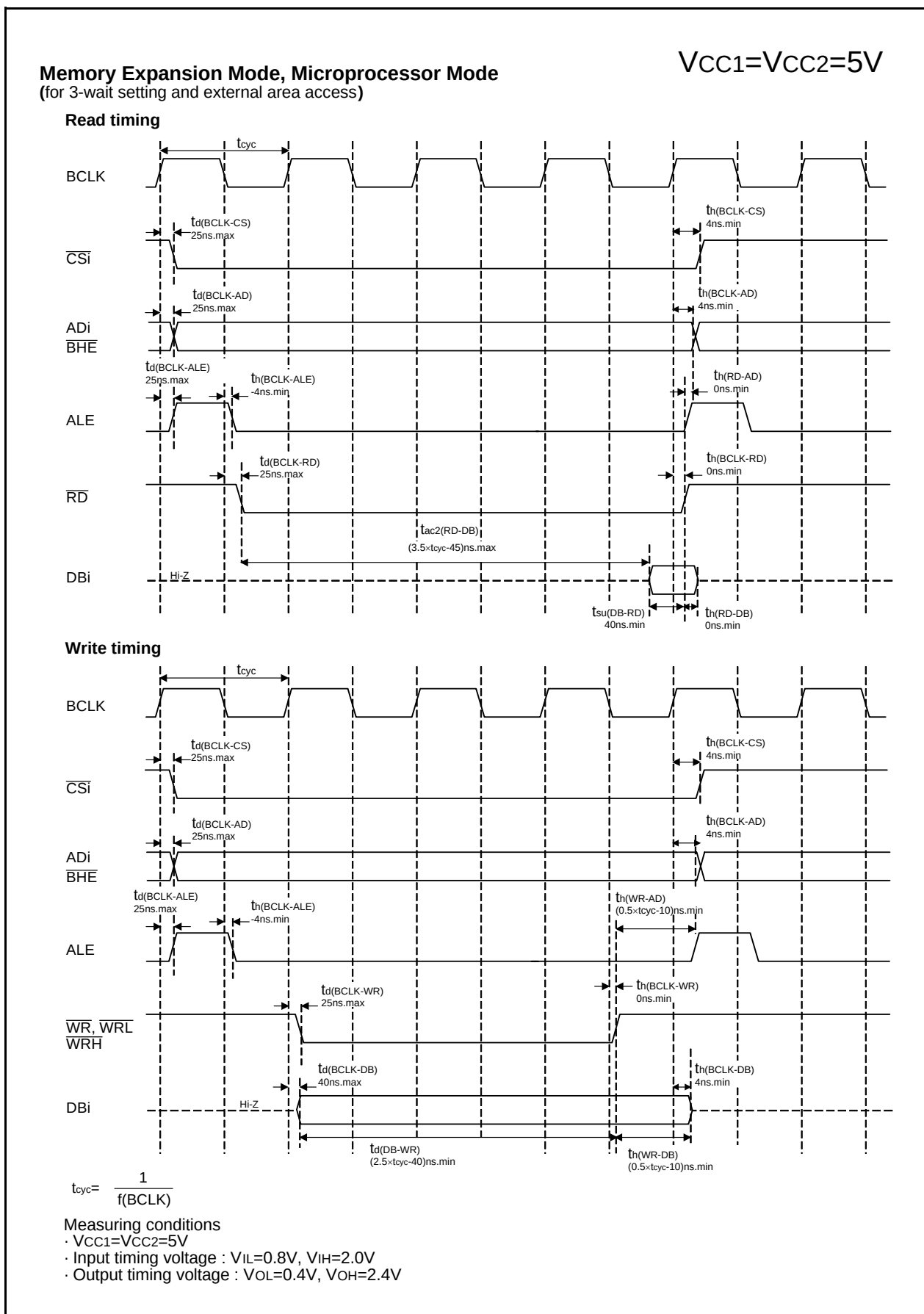


Figure 5.9 Timing Diagram (7)

$$V_{CC1}=V_{CC2}=3V$$

Timing Requirements

($V_{CC1} = V_{CC2} = 3V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.40 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on both edges)	120		ns

Table 5.41 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	600		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	300		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	300		ns

Table 5.42 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	600		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	300		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	300		ns

Table 5.43 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time	1500		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ Input LOW Pulse Width	200		ns

Table 5.44 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	300		ns
$t_{w(CKH)}$	CLKi Input HIGH Pulse Width	150		ns
$t_{w(CKL)}$	CLKi Input LOW Pulse Width	150		ns
$t_{d(C-Q)}$	TXDi Output Delay Time		160	ns
$t_h(C-Q)$	TXDi Hold Time	0		ns
$t_{su(D-C)}$	RXDi Input Setup Time	100		ns
$t_h(C-D)$	RXDi Input Hold Time	90		ns

Table 5.45 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input HIGH Pulse Width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ Input LOW Pulse Width	380		ns

$$V_{CC1}=V_{CC2}=3V$$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5V$, $V_{SS} = 0V$, at $T_{opr} = -20$ to $85^{\circ}C$ / -40 to $85^{\circ}C$ unless otherwise specified)

Table 5.48 Memory Expansion and Microprocessor Modes (for 2- to 3-wait setting, external area access and multiplex bus selection)

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_d(BCLK-AD)$	Address Output Delay Time	See Figure 5.12		50	ns
$t_h(BCLK-AD)$	Address Output Hold Time (in relation to BCLK)		4		ns
$t_h(RD-AD)$	Address Output Hold Time (in relation to RD)		(NOTE 1)		ns
$t_h(WR-AD)$	Address Output Hold Time (in relation to WR)		(NOTE 1)		ns
$t_d(BCLK-CS)$	Chip Select Output Delay Time			50	ns
$t_h(BCLK-CS)$	Chip Select Output Hold Time (in relation to BCLK)		4		ns
$t_h(RD-CS)$	Chip Select Output Hold Time (in relation to RD)		(NOTE 1)		ns
$t_h(WR-CS)$	Chip Select Output Hold Time (in relation to WR)		(NOTE 1)		ns
$t_d(BCLK-RD)$	RD Signal Output Delay Time			40	ns
$t_h(BCLK-RD)$	RD Signal Output Hold Time		0		ns
$t_d(BCLK-WR)$	WR Signal Output Delay Time			40	ns
$t_h(BCLK-WR)$	WR Signal Output Hold Time		0		ns
$t_d(BCLK-DB)$	Data Output Delay Time (in relation to BCLK)			50	ns
$t_h(BCLK-DB)$	Data Output Hold Time (in relation to BCLK)		4		ns
$t_d(DB-WR)$	Data Output Delay Time (in relation to WR)		(NOTE 2)		ns
$t_h(WR-DB)$	Data Output Hold Time (in relation to WR)		(NOTE 1)		ns
$t_d(BCLK-HLDA)$	HLDA Output Delay Time			40	ns
$t_d(BCLK-ALE)$	ALE Signal Output Delay Time (in relation to BCLK)			25	ns
$t_h(BCLK-ALE)$	ALE Signal Output Hold Time (in relation to BCLK)		-4		ns
$t_d(AD-ALE)$	ALE Signal Output Delay Time (in relation to Address)		(NOTE 3)		ns
$t_h(AD-ALE)$	ALE Signal Output Hold Time (in relation to Address)		(NOTE 4)		ns
$t_d(AD-RD)$	RD Signal Output Delay From the End of Address		0		ns
$t_d(AD-WR)$	WR Signal Output Delay From the End of Address		0		ns
$t_{dz}(RD-AD)$	Address Output Floating Start Time			8	ns

NOTES:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 [ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 50 [ns] \quad n \text{ is "2" for 2-wait setting, "3" for 3-wait setting.}$$

3. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 40 [ns]$$

4. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 15 [ns]$$

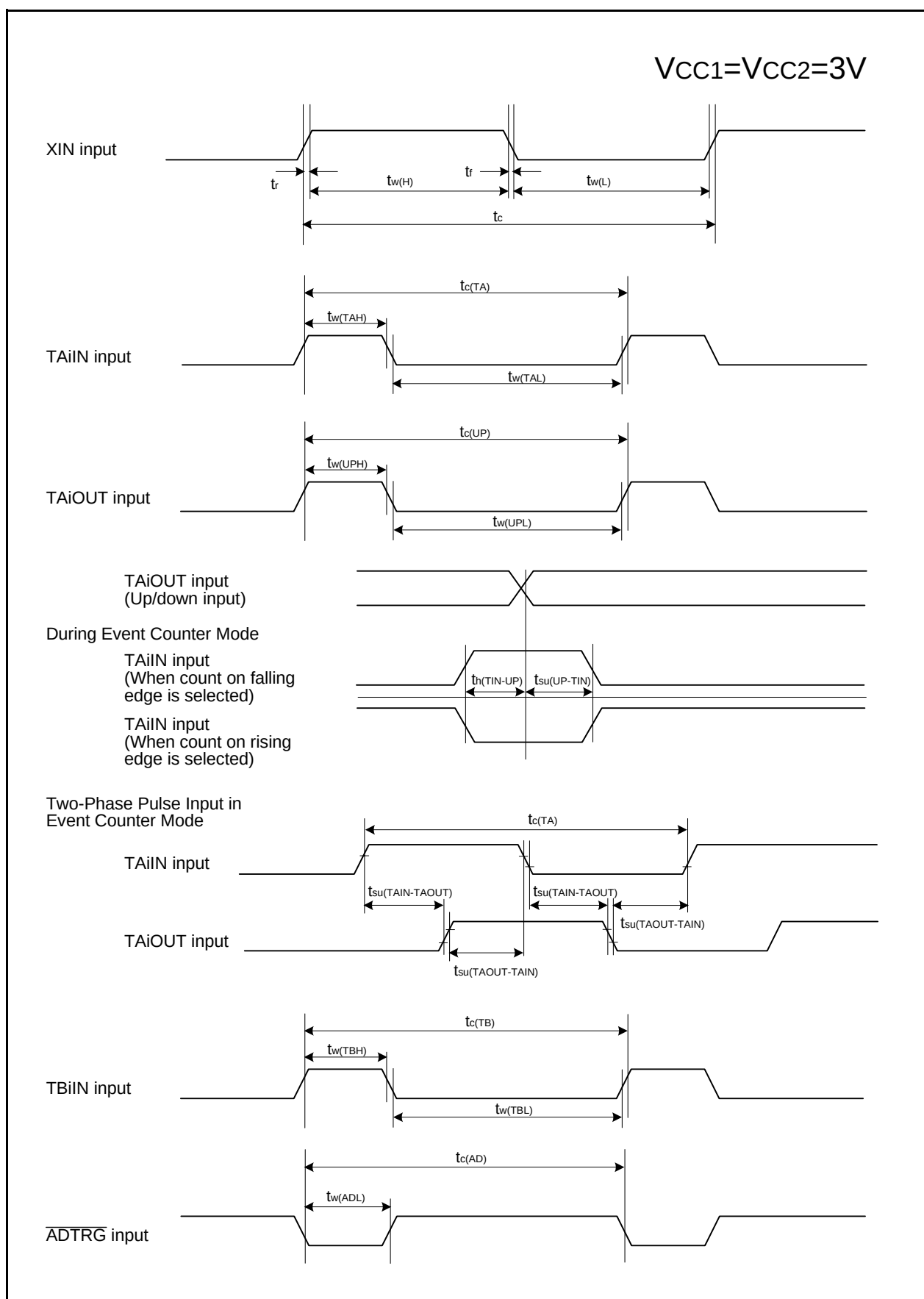


Figure 5.13 Timing Diagram (1)

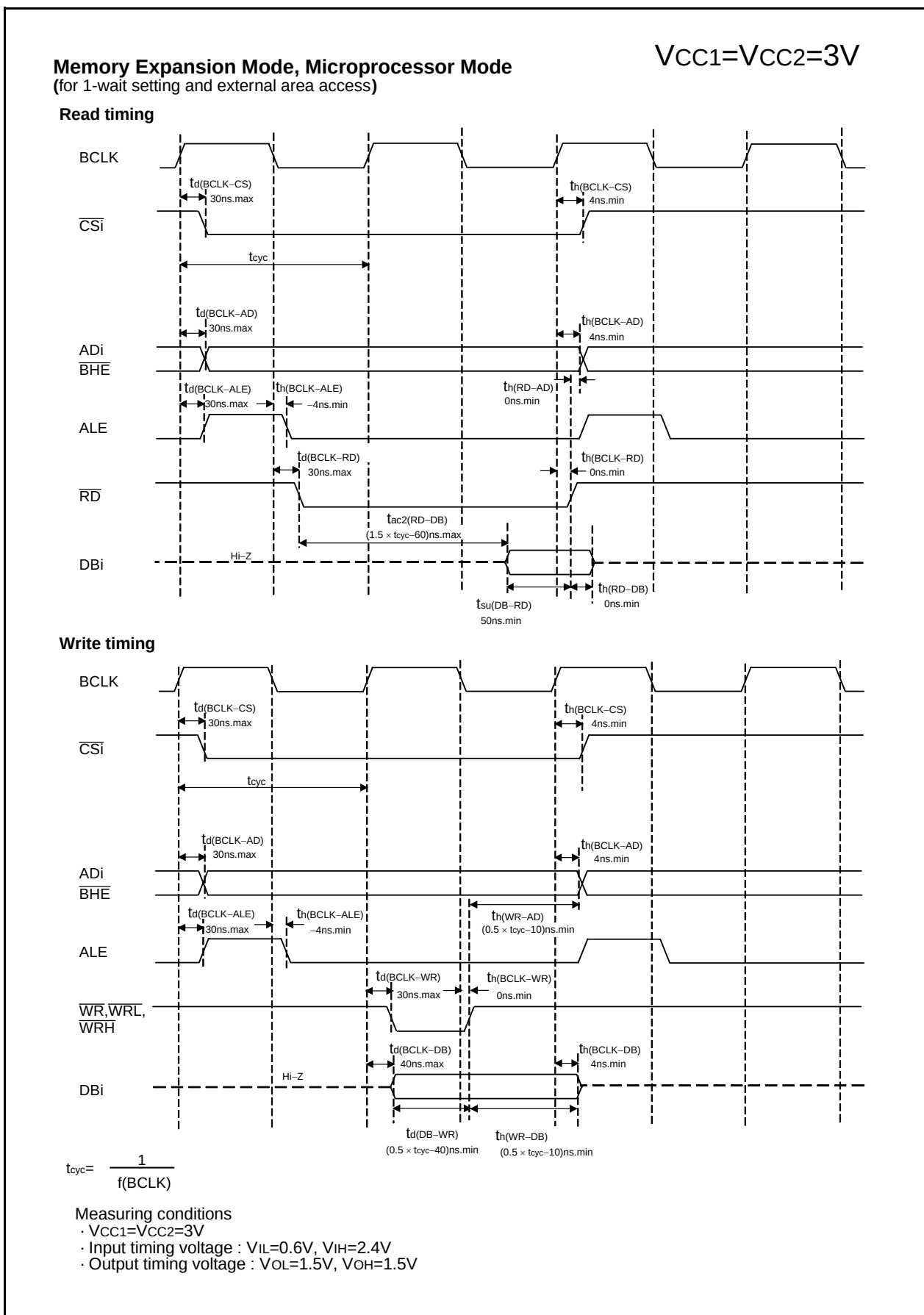


Figure 5.17 Timing Diagram (5)

Appendix 1.Package Dimensions

